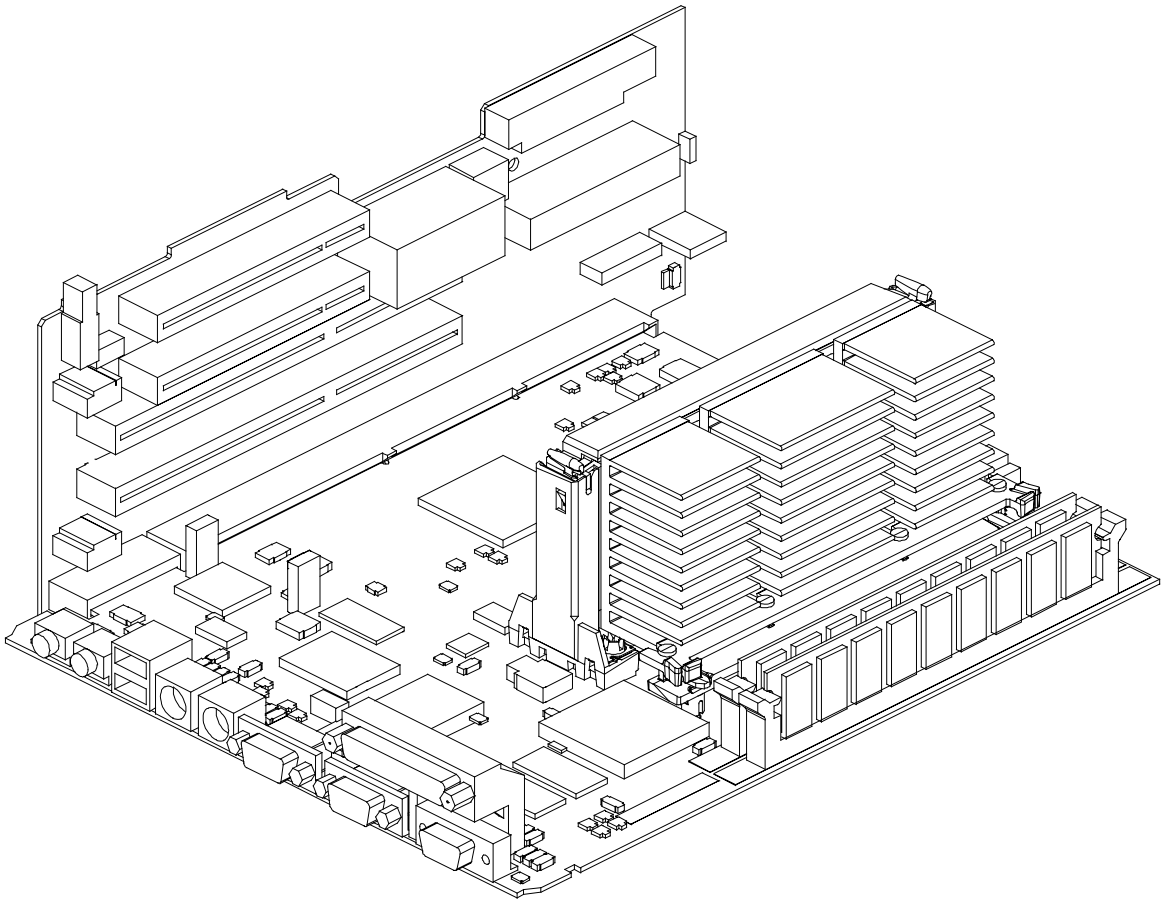
NLX Motherboard Specification

Release 1.8



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Version 1.8, April 1999

Revision History, Current

Revision 1.2 to 1.8 (for previous revision history, see Section 8 in this specification)

General: Preliminary Version 1.61 had a limited external distribution; Preliminary Version 1.7 had internal distribution only. These versions addressed a proposed form-factor addition that was subsequently dropped. We have incremented to Version 1.8 for this public release of the specification because of the number of electrical changes that have incremented since Version 1.2; see the details below. We made various editorial changes for clarity and consistency.

- Title page: substituted a detailed example drawing.
- Incorporated all approved, published Engineering Change Requests (ECRs) to date.
- Listed figures in the Contents. Updated all figure numbers to be consecutive throughout the document and omitted the section numbers from the figure numbers. For the equivalent old/new numbers, see Table 18 in Section 8.
- Listed tables in the Contents. Updated all table numbers to be consecutive throughout the document and omitted the section numbers from the table numbers. For the equivalent old/new numbers, see Table 19 in Section 8.
- Renamed Appendix A to be Section 6 and Appendix B to be Section 7 to enable use of automatic paragraph numbering.
- Section 2, Figure 1 (was Fig. 2.1): repeated the example drawing from the title page.
- Figure 5 (was Fig. 3.4): corrected mounting hole size to 0.156 inches from 0.140 inches.
- Figure 8 (was Fig. 3.7): the correct measurement from zone A to zone B (2.5”[63.5mm]) is from the bottom of zone B, not from the top of zone B.
- Inserted Figures 12, 13, and 14 in place of Figures 3.9, 3.10, and 3.11; see the notes below each figure.
- Section 3.3.3: added text and Figure 15 (was Fig. 3.11.1 in ECR# P16) to specify the recommended connector tilts for the axes of the NLX riser board card edge connector.
- Section 3.6: clarified the text that describes the optional keepout zone C.
- Section 3.8.1: clarified the text that describes the maximum component height at the far left primary side of the motherboard, distinguishing between boards that either do or do not accept AGP add-in cards. Provided two separate figures instead of just one (do or do not accept AGP cards).
- Section 3.8.4: clarified the text that describes the optional keepout zone C.
- Section 3.9.1: added text to clarify the allowable area for motherboard connectors to protrude from the I/O aperture.
- Figure 21 (was Fig. 3.17): corrected the corners for the I/O aperture and clarified the allowable I/O connector area.

Continued

Revision History, Current (continued)

- Section 3.9.2: added text to clarify the intent of the contact surface for the I/O aperture (location of the end surface flange in the I/O aperture). Modified the explanation of the flat surface on the flange to match Figures 21 and 22.
- Figure 22 callouts (was Fig. 3.18): clarified the wording about the flanges on the I/O aperture to help ensure that a standard NLX I/O shield can be used with the specified flanges. Changed callout "maximum top flange" to "maximum top flange gap"; changed callout "minimum lower flange" to "minimum lower flange gap."
- Table 5 (was Table 4.3), deleted the two pins used for IEEE-1394 power, and added the 3.3Vaux (3.3VSB) signal. Changed total signals to 68.
- Table 9 (was Table 4.7), changed the number of reserved pins to four. Changed total signals to 30.
- Table 12 (was Table 4.10):
  - Pin A135 was redefined to carry 3.3V Standby (3.3Vaux) on the NLX riser to comply with PCI 2.2 (PM 1.1); previously, this pin was reserved. Added footnote to table.
  - Pins A157, A158, A160, and A161: a footnote was added to clarify the location of USB pulldown and series termination.
  - Pins A168, B167, B168, and B169 were redefined to implement 1394-1995 IEEE standards in NLX. The four pins (previously reserved) are now assigned for the differential pairs.
  - Pins A167 and B166 were changed to Reserved; there is no longer a need to carry isolated 1394 power on these two pins.
- Table 13 (was Table 4.11):
  - Corrected the description of Serial bus signals SDA and SCL to be Open Drain, not TTL. The change allows compatibility with SM bus implementations.
  - Corrected the description of Serial bus signal SCL to show the correct reserved EEPROM address as 1010111.
  - Removed pins A168, B167, B168, and B169 from the section listing Reserved pins and added them to the section listing IEEE 1394 signals.
  - Removed pin A135 from the section listing Reserved pins and added it to the section listing Power.
  - Removed pins A167 and B166 from the section listing IEEE 1394 pins and added them to the section listing Reserved pins.
  - Added a footnote about speed requirements and a pointer to the IEEE standard.
- Added Figure 25 to support Table 13 information about IEEE 1394 signals.

Revision History, Current (continued)

- Table 16 (was Table A.3): corrected two recommended voltage tolerances. Current industry-standard power supplies support ±10% tolerance on negative rails and ±5% on the +3.3V rail. Motherboards and option cards do not require tighter tolerance. This correction was made in the *NLX Power Supply Recommendations* and is being made here to match that change.
- Figure 32 (was Fig. B.2) and Figure 33 (was Fig. B.3): the measurement from the key on the NLX riser connector to pin 1 on the connector was corrected to be 75.50 [2.972], not 77.44 [3.049].
- Table 17 (was Table B.1):
  - Pin X5, corrected the description of FP_SPKR_EN (Front Panel Speaker Enable); this signal is pulled low through a pulldown on the motherboard, not pulled high.
  - Pin Y5, corrected the description of FP_MIC_EN (Front Panel Microphone Enable); this signal is high when the microphone is plugged in and low when it is not.
  - Pin Y13, corrected the MODEM_SPKR signal to input to the motherboard, not output.
  - Pins X9, X10, X11, formerly reserved, now carry AC ’97 input signals to the motherboard.
  - Pin Y8 previously supported an AC ’97 device; its name has been modified from AC_SD_IN to AC_SD_IN0 to indicate that it now carries input signal 0 of 4.

Contents

Figures

Tables

1. Executive Summary

NLX is a new low profile motherboard form factor designed to improve upon today's low profile form factors and to adapt to new market trends and PC technologies. NLX does the following:

- Supports current and future processor technologies
- Supports new Accelerated Graphics Port (AGP) high performance graphics solutions
- Supports tall memory modules and DIMM technology
- Provides more flexibility for system-level design and integration; for example, the new design flexibility allows system designers to implement a motherboard that can be installed quickly, in most cases without using screws, thus lowering the PC's total cost of ownership.

Several major PC vendors world-wide worked jointly to define the NLX form factor and to incorporate flexibility to accommodate the best designs for current and future PCs. NLX is a public specification intended for widespread use in many types of systems. The specification and other information on NLX are available through the public Web site *http://www.teleport.com/~nlx* or *http://www.teleport.com/~ffsupprt/*.

1.1 Technology Influences

New physical size and thermal characteristics: Today's low profile form factors are not well suited for the physical size and thermal characteristics of the next generation of microprocessors. New processors will dissipate more heat and will use more physical space in the system. These new processors, combined with new high powered graphics solutions, such as the Accelerated Graphics Port (AGP), and DIMM technology, can cause designs like LPX to have limitations such as restricted use of these technologies. Dual processor technology will also increase the thermal and mechanical needs of today's designs.

Multimedia drives new form factor requirements: Video-playback, enhanced graphics, and extended audio connectivity are becoming the standard hardware building blocks to support multimedia. To achieve cost savings, the features are being integrated onto the motherboard. To achieve this integration, most multimedia features must have connectors on the motherboard. However, with today's form factors, it is a challenge to bring more I/O connectivity out of the chassis. Some designers bring audio and video I/O out of the chassis with small passive daughter cards or cables connecting motherboard components to connectors mounted on spare expansion slots on the chassis. While this reduces cost compared to a full add-in card solution, it is still substantially more costly than placing I/O connectors on the motherboard. The NLX form factor addresses this need by providing more connector space at the back of the chassis and by allowing connectors to be placed out the front of the chassis through the use of the riser. The NLX design also provides other

features, such as less cable clutter and fewer connections, thus reducing cost and improving the quality of the system.

The introduction of new technologies—processor, memory, and graphics—requires a new motherboard form factor to take full advantage of these powerful new components. NLX supports these technologies with its form factor design.

1.2 Other Technical Documents

For information about the following areas, see the series of NLX design guidelines and suggestions that can be downloaded from the NLX public Web site at *http://www.teleport.com/~nlx*:

- *NLX Board Gauge User Manual*
- *NLX Chassis Design Suggestions*
- *NLX Electrical Design Suggestions* (V1.21)
- *NLX EMC Design Suggestions*
- *NLX Generic Riser Card Design Overview* (updated)
- *NLX Ground Clip Design Suggestions*
- *NLX I/O Shield Design Suggestions* (updated)
- *NLX Power Supply Recommendations* (V1.1)
- *NLX Rail Design Suggestions*
- *NLX Thermal Design Suggestions*
- *NLX Chassis Gauge User Manual*

For information about signal requirements for a high-speed serial bus, see the IEEE Standard for a High Performance Serial Bus, 1394-1995; refer to the IEEE World Wide Web site at

http://standards.ieee.org/

For detailed information about the Accelerated Graphics Port (AGP) specification, see the World Wide Web site at

http://www.agpforum.org/

2. NLX Form Factor Overview

Figure 1 shows an example of an NLX board and riser.

- The add-in card riser is located at the left edge of the motherboard (as viewed from the back).
- Tall components such as the processor and memory are typically located on the opposite side from the I/O slots. This allows full length add-in cards in many system configurations.
- The back I/O connectors are stacked single- and double-high to support more connectors.

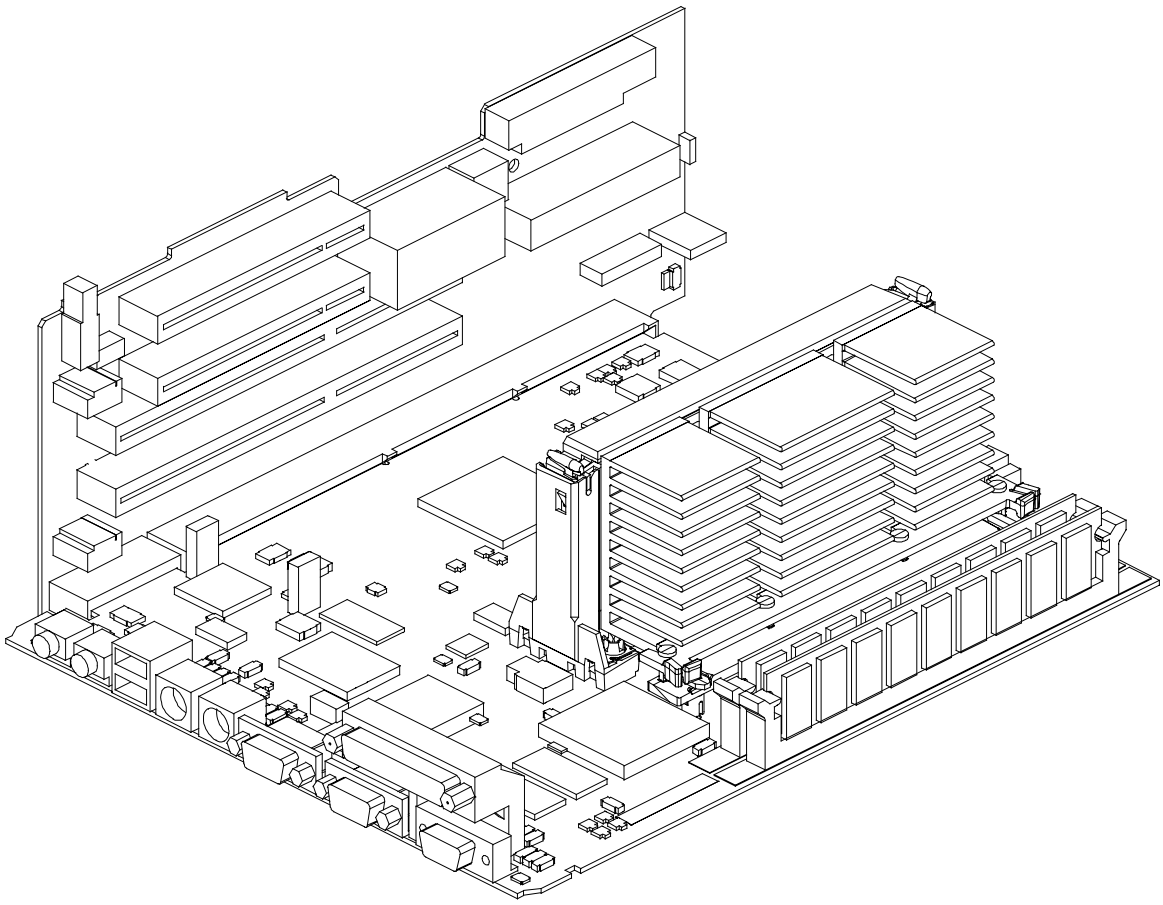

Figure 1. NLX Board and Riser Example

(8.25 x 10 inch board as example)

2.1 NLX System Configuration Example

Figure 2 shows an NLX motherboard in a system layout that highlights NLX form factor features for a low profile design. Note that this specification offers many possible system configurations.

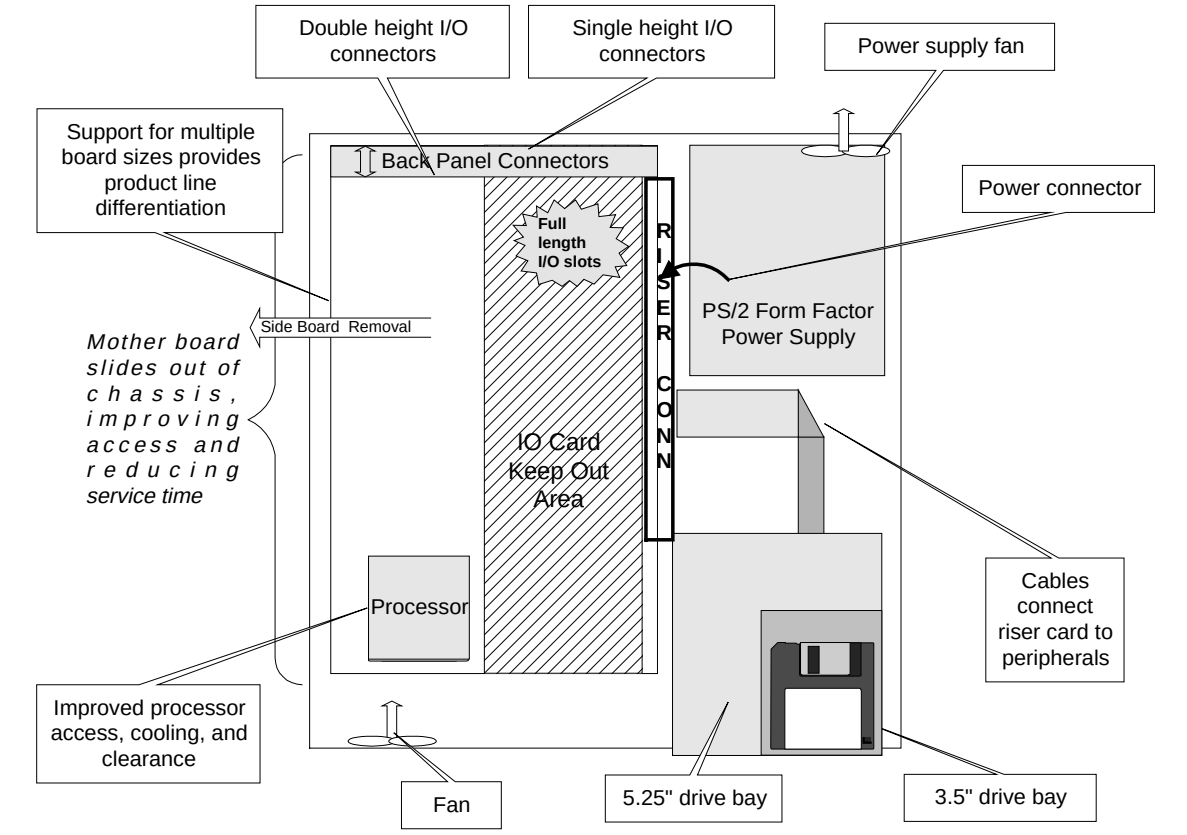

Figure 2. NLX System Layout Example

Summary of features shown in Figure 2:

- Use of double-high connectors across half the back I/O area and single-high across the whole 9-inch maximum board width
- Power supply harness that connects directly to the NLX riser, not to NLX boards
- Floppy and IDE-based peripheral signal cables that attach to the riser card
- Drive bays that can all fit to one side of the riser in a convenient 17.5-inch wide low profile system form factor
- Processor located toward the front of the system, close to the fan, for optimum cooling
- Dockable motherboard that slides into the system and docks with the riser card

2.1.1 NLX Riser Card

Riser design: NLX has extended the traditional basic riser card functionality to define an extended pinout for the riser card connection. The NLX pinout defines pins for the PCI bus, ISA bus, power, IDE, floppy, serial bus, and other I/O signals, which allows the following:

- Most cables that would normally attach to the motherboard can now be attached to the riser, enabling high motherboard serviceability.
- The system designer can optionally place devices and connectors on the riser, improving options for product differentiation for the PC OEM.

2.2 Benefits for OEMs

The NLX design provides improved design flexibility for product features, total lower cost of ownership, improved manufacturability, and quality.

Features and Benefits:

- PC system manufacturers can increase their manufacturing and inventory flexibility by stocking fewer motherboards and using several different riser cards, each with active features such as audio or I/O logic (i.e., 1394) on the riser card instead of the motherboard.
- NLX boards can be used in a minitower chassis by vertically orienting the motherboard. Using a single motherboard design for both the low profile and minitower offerings provides inventory management benefits to many PC manufacturers.
- The NLX form factor, with its riser card configuration, is a versatile design because it can be used in a wide range of system configurations, including low profile, desktop, modular, minitower, and servers.
- The specification is written such that the same form factor and chassis can be used for single and dual processor systems.

3. NLX Mechanical Specifications

The following sections describe the mechanical dimensions of the NLX form-factor motherboard, including physical size, mounting hole placement, back panel I/O shield opening, card-edge connector placement, and component height constraints. Table 1 defines the terms used in the mechanical diagrams in this document.

3.1 NLX Motherboard Dimensions

3.1.1 Definition of Terms Used in Mechanical Diagrams

Table 1. Definition of Terms Used in the Mechanical Diagrams

Term/phrase	Definition
Tolerances	All dimensions are mm/inches unless otherwise specified. +/- tolerances are: Sheet metal / chassis = +/- 0.010 inches board mounting hole to edge = +/- 0.010 inches board hole to hole = +/- 0.005 inches board hole size = + 0.003 inches -0.001 inches plastic = +/- 0.005 inches
Motherboard thickness	A nominal motherboard thickness of 0.062 inches is used throughout the specification to calculate dimensions. Any deviation from this nominal value will affect most of the dimensions and must be considered.
Keepout areas for EMI clips, required	The EMI clip location area is reserved for EMI clips. The chassis must provide keepout areas in the EMI clip location areas to provide an electrical contact to the chassis. The EMI clips protrude from the secondary side of the motherboard in these areas. ***Required.***
Keepout areas for mounting holes, required	Primary side areas of the motherboard with no traces and components, to assure the motherboard can accommodate the attachment of rail support. ***Required.***
Keepout zones, recommended	Secondary side zones of the motherboard with no protruding pins from primary side components, and no secondary side SMT components, to assure that the motherboard can slide into the chassis and be mounted without rails. Recommended.

3.1.2 NLX Board Size

The NLX specification supports motherboards with overall dimensions of 9.0 inches x 13.6 inches (maximum) to 8.0 inches x 10.0 inches (minimum). An NLX-compatible chassis must be able to accommodate motherboards with these two extreme dimensions, and all sizes in between. The specification defines the maximum motherboard width as 9.0 inches, so an NLX chassis must be designed to accept boards up to 9.0 inches wide. The minimum motherboard width is 8.0 inches; an NLX chassis can support board widths down to 8.0 inches because of the way the NLX mounting holes are placed. The specification defines motherboard lengths from 10.0 inches to 13.6 inches. To accommodate these board sizes,

the chassis must allow for a maximum length board of 13.6 inches and must include all three sets of mounting holes.

Motherboard dimensions with keepout areas are illustrated in Figures 3 to 8. The figures show the primary and secondary sizes of 8.0 inch-9.0 inch board widths, in lengths of 10.0 inches, 11.2 inches, and 13.6 inches.

Section 3.3, "NLX Card Edge Connector," describes the location of the card edge gold fingers.

3.1.3 Mounting Hole Placement

As detailed in the section above, the NLX specification supports motherboards with overall dimensions of 9.0 inches x13.6 inches (maximum) to 8.0 inches x 10.0 inches (minimum), and any size in between.

To simplify the design of both motherboards and chassis, the specification details three sets of mounting holes, which are located to allow motherboard size optimization. **Any given motherboard needs to have only one set of four mounting holes, whereas the chassis is required to support all three sets.** The chassis designer must determine how the motherboard is mounted to the chassis with the specified set of mounting holes.

The exact method of how the chassis uses these holes to mount the motherboard is left to the system designer. The chassis designer must adhere to all requirements and keepout area details of this specification for the chassis to be NLX-compliant.

The motherboard can be mounted with any set of the mounting holes provided but must support the four holes in the defined set. The chassis needs to support only one set of four holes at a time. Three sets of holes are defined to support the most common motherboard sizes, as listed in Table 2 with hole sets and locations.

Table 2. Mounting Hole Placement

Hole set and board length	Position of hole along length dimension (inches)	Position of hole along width dimension (inches)
Hole set A:	13.400	7.800
13.6 inch board length	13.400	4.400
	7.175	7.800
	7.175	4.400
Hole set B:	11.000	7.800
Less than 13.6 inches to a minimum board length of 11.2 inches	11.000	4.400
	4.775	7.800
	4.775	4.400
Hole set C:	9.800	7.800
Less than 11.2 inches to a minimum board length of 10.0 inches	9.800	4.400
	3.575	7.800
	3.575	4.400

3.1.4 NLX Board Complete Keepout Specification

- Primary side: ***Required,*** four keepout areas; these are 0.390 inches in diameter and centered around the four mounting holes (plated and grounded, Mounting Hole Required "keepout area A").
- Secondary side: ***Required,*** six keepout zones; these are 0.400 inches square, centered around the four mounting holes (plated, required "keepout zone A"), and the two additional keepout areas (required "keepout zone B") for rail bumpers. No traces, through-holes devices, or SMT devices are allowed within "keepout zone A." No through-holes devices or SMT devices are allowed within required "keepout zone B."

The NLX specification encourages motherboard manufacturers not to use through-hole and secondary side SMT devices along the suggested "keepout zones B" (see Figures 3 to 8 for notes on zones). If these zones are kept free, the user has the option of sliding the motherboard in directly and mounting it to the chassis without rails. For this situation, board traces are allowed along the recommended keepout zones, but system assemblers are required to ensure that the motherboard traces are not damaged during the motherboard slide in/out process.

Note

See section 3.8.5 for additional secondary side component height constraints.

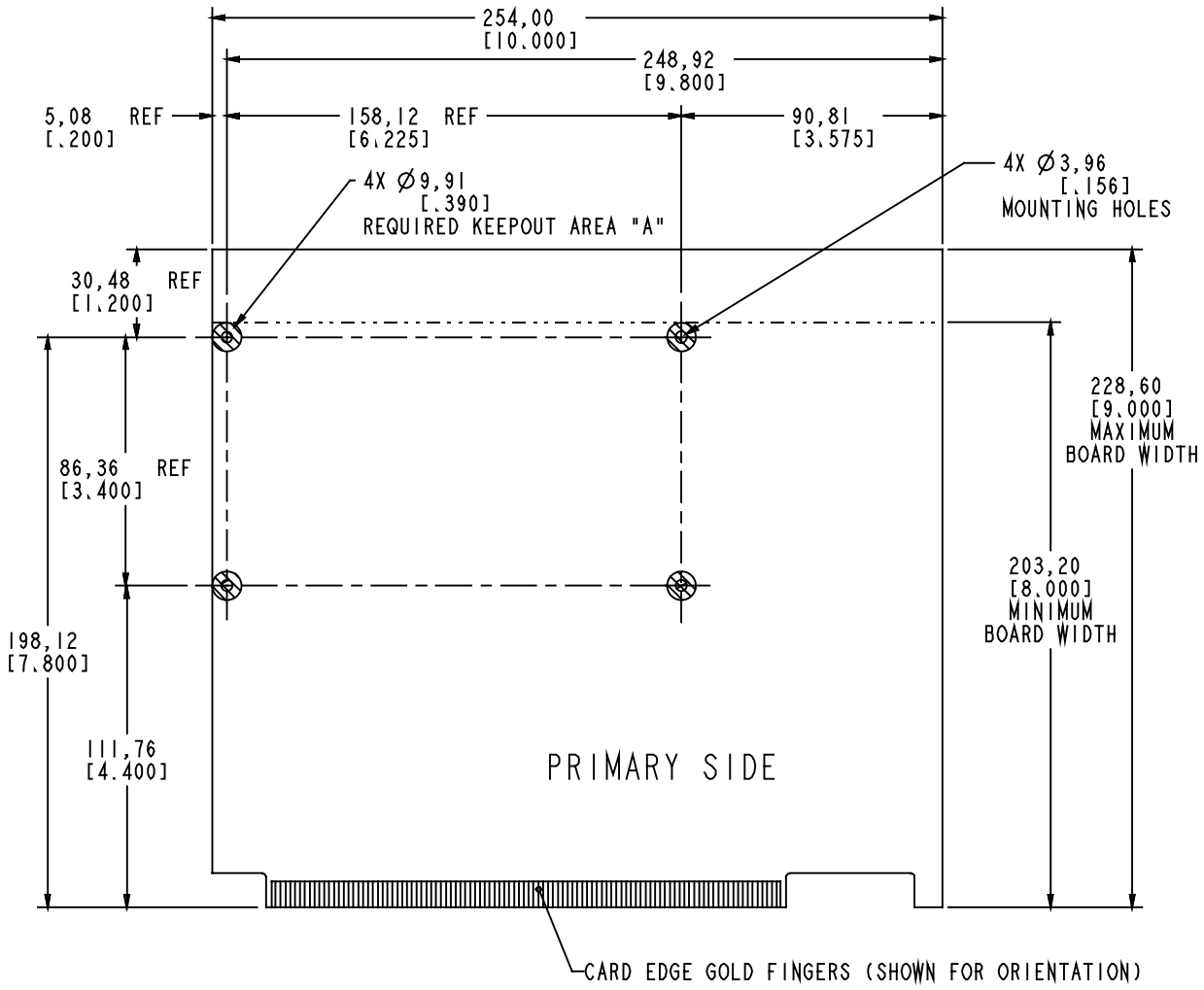

Figure 3. NLX Motherboard Dimensions—10.0 Inches Primary Side

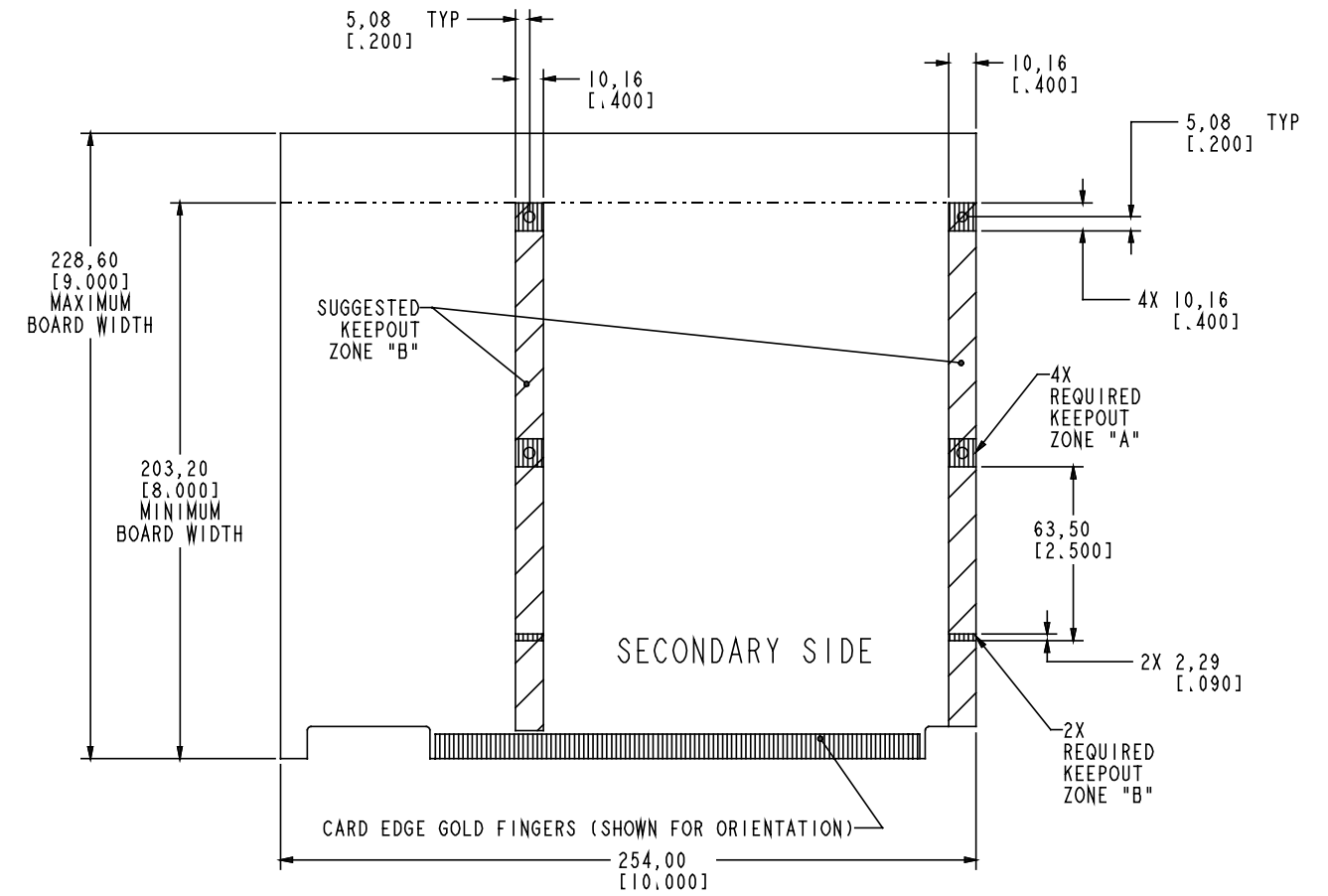

Figure 4. NLX Motherboard Dimensions—10.0 Inches Secondary Side

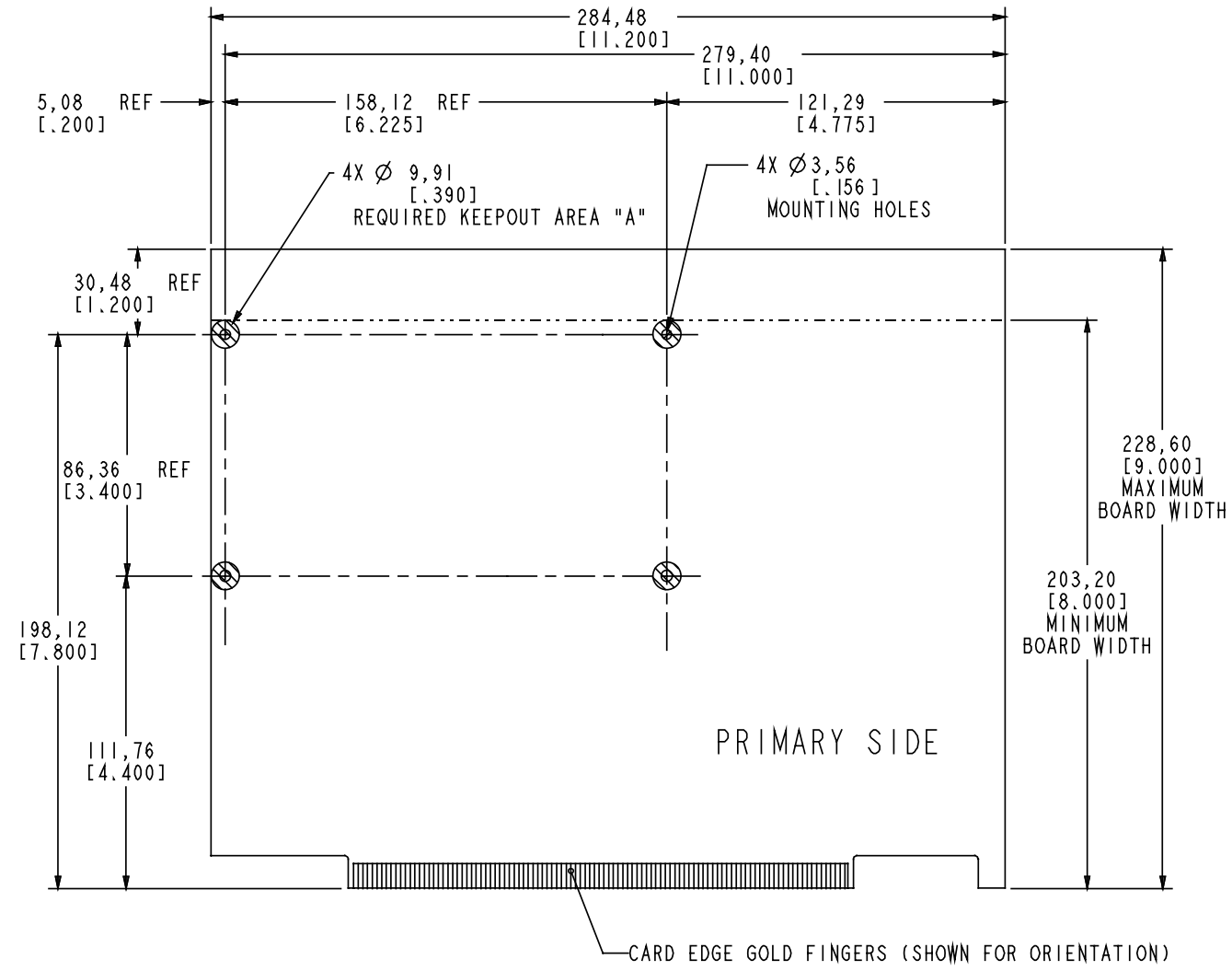

Figure 5. NLX Motherboard Dimensions—11.2 Inches Primary Side

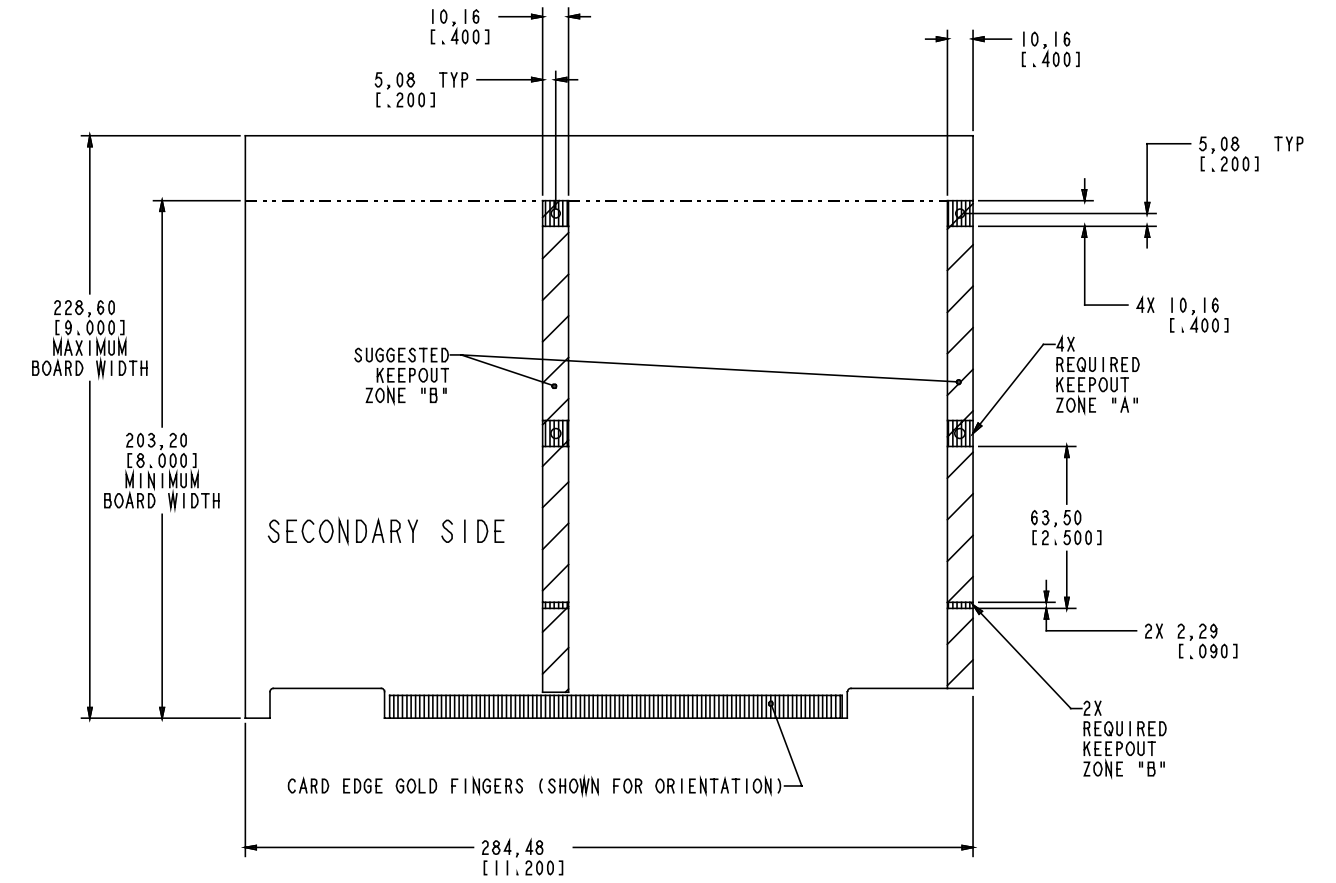

Figure 6. NLX Motherboard Dimensions—11.2 Inches Secondary Side

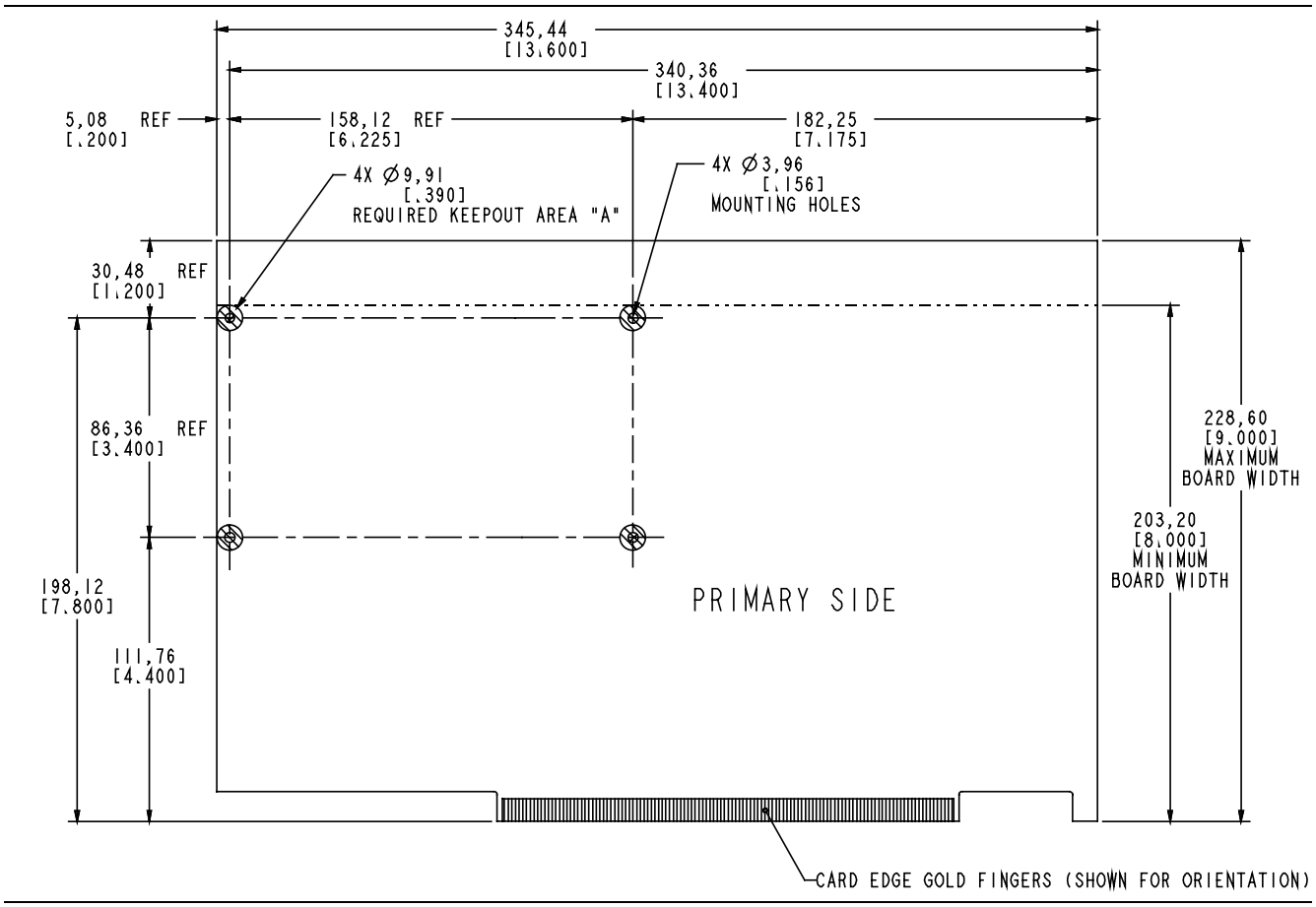

Figure 7. NLX Motherboard Dimensions—13.6 Inches Primary Side

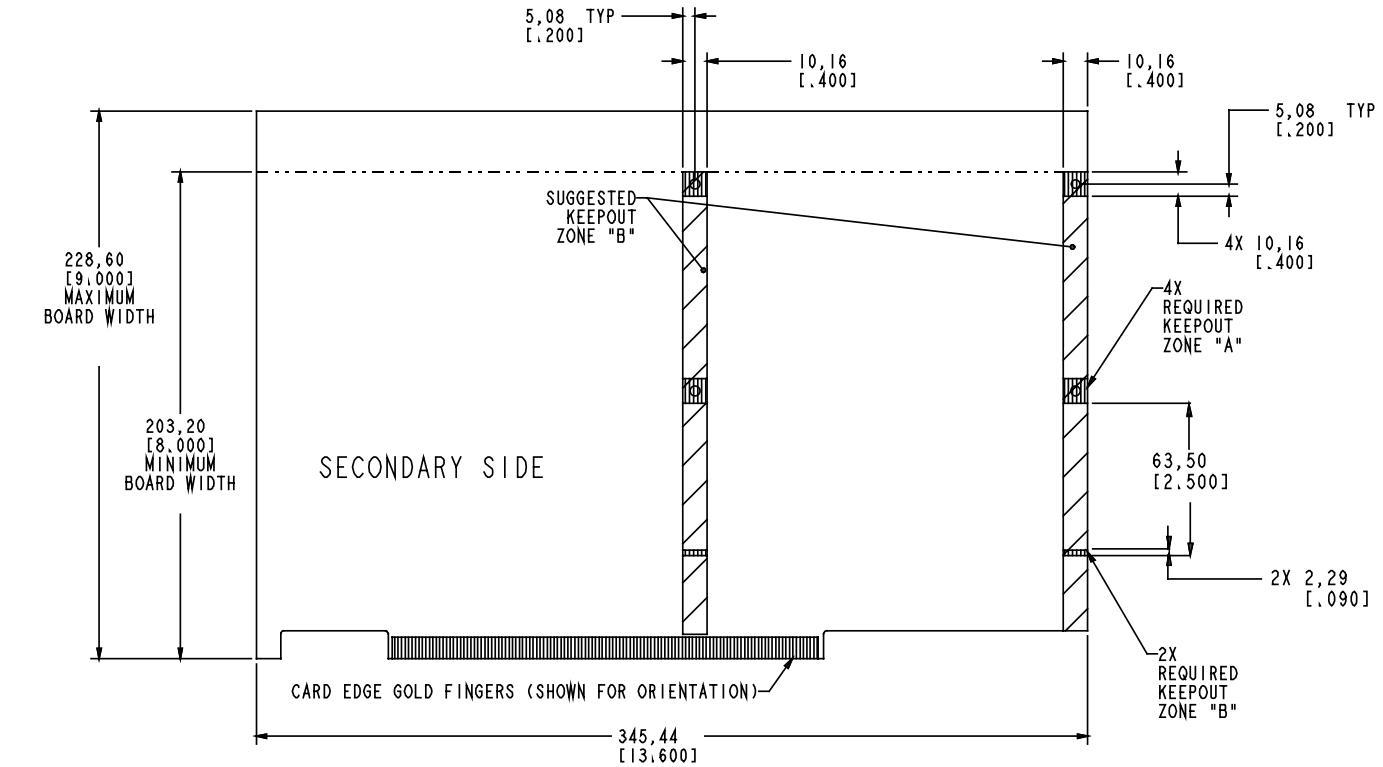

Figure 8. NLX Motherboard Dimensions—13.6 Inches Secondary Side

3.2 Motherboard EMI Clip Locations with Chassis Keepouts

The specification defines EMI clip location areas and chassis keepout areas for motherboard designs that require multipoint grounding solutions. A flat, electrically conductive, clean surface must be provided in these keepout areas. The optional clips provide a ground contact between the motherboard and chassis, replacing the electrical functionality of screws used in previous chassis designs. Figure 9 shows chassis keepout areas and motherboard EMI clip location areas for all three motherboard lengths.

The EMI clips protrude through the secondary side of the motherboard in the clip location areas. Figure 9 shows the areas of a motherboard where a board designer can place EMI clips to make electrical contact to the chassis. The chassis manufacturer must design the chassis with the required keepout areas to allow a motherboard with EMI clips to slide into the chassis without interference. The primary surface of the riser card is defined as the side that the 340-pin connector is mounted on.

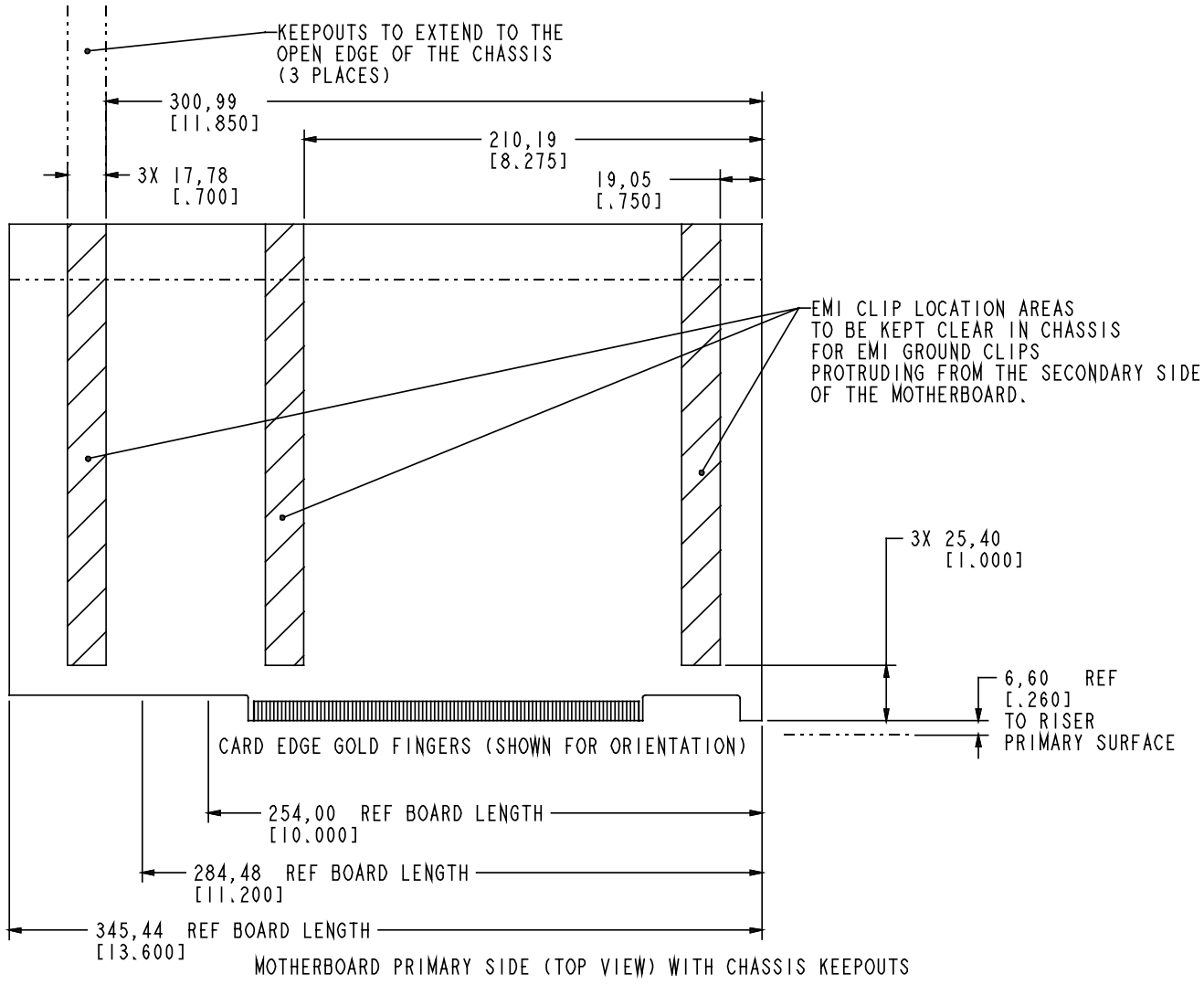

Figure 9. Chassis Keepout Areas and Motherboard EMI Clip Location Areas

3.2.1 EMI Grounding Using Motherboard Rails

To allow for grounding of the motherboard to the chassis through the rails, a required ground path has been specified. The four hatched areas shown in Figure 10 are dimensioned from the motherboard mounting holes as defined by board size. Rails with ground clips attached will contact the motherboard grounding pads, extend through the mounting rails, and rest on the pads shown in Figures 10 and 11. This will increase the grounding options provided on an NLX board to improve EMI characteristics if required. The cross sectional view in Figure 11 shows the standard rail clip design with the 0.313 inches required pad height to ensure contact with the rail mounted EMI clips. If a chassis design is such that the board height is greater than 0.313 inches, then an emboss or additional detail should be provided to ensure ground contact with a standard rail clip design.

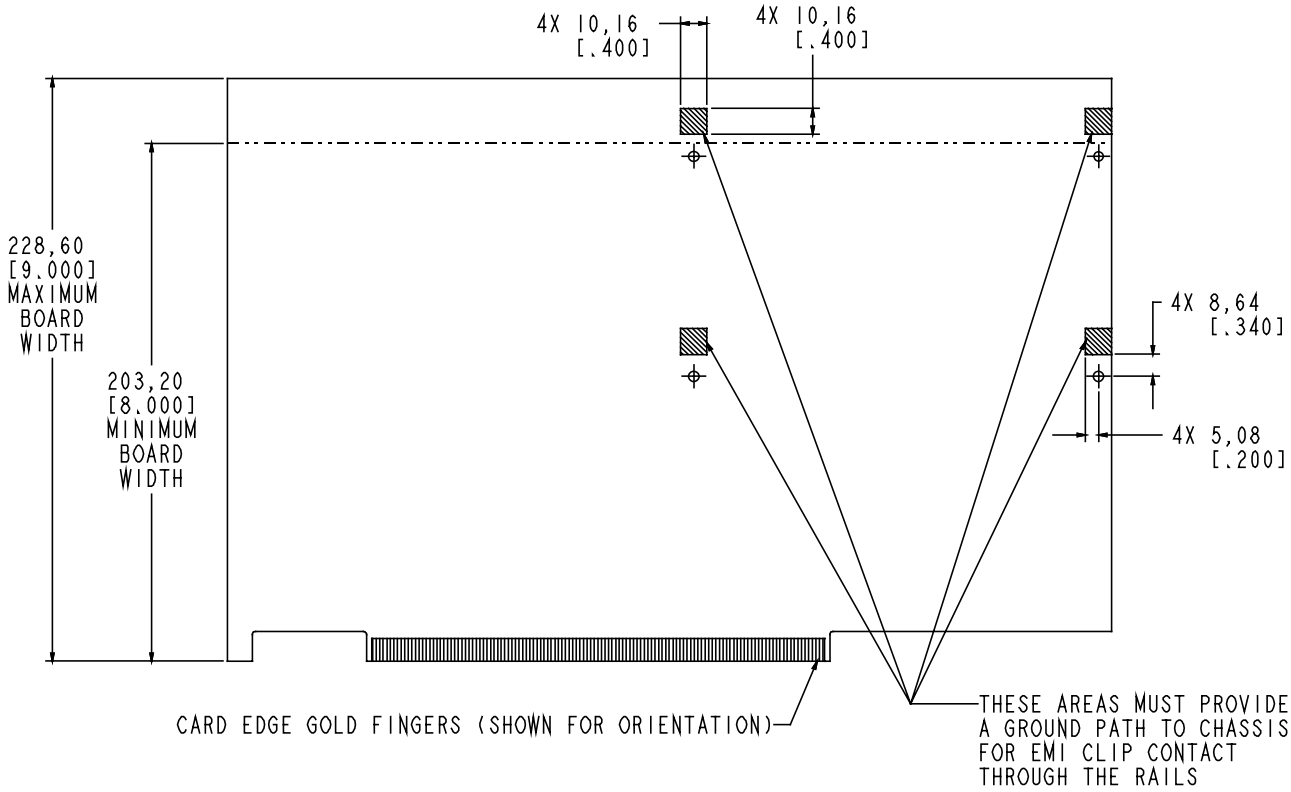

Figure 10. Ground Pad Detail on Chassis for EMI Clips on Rails (secondary side shown)

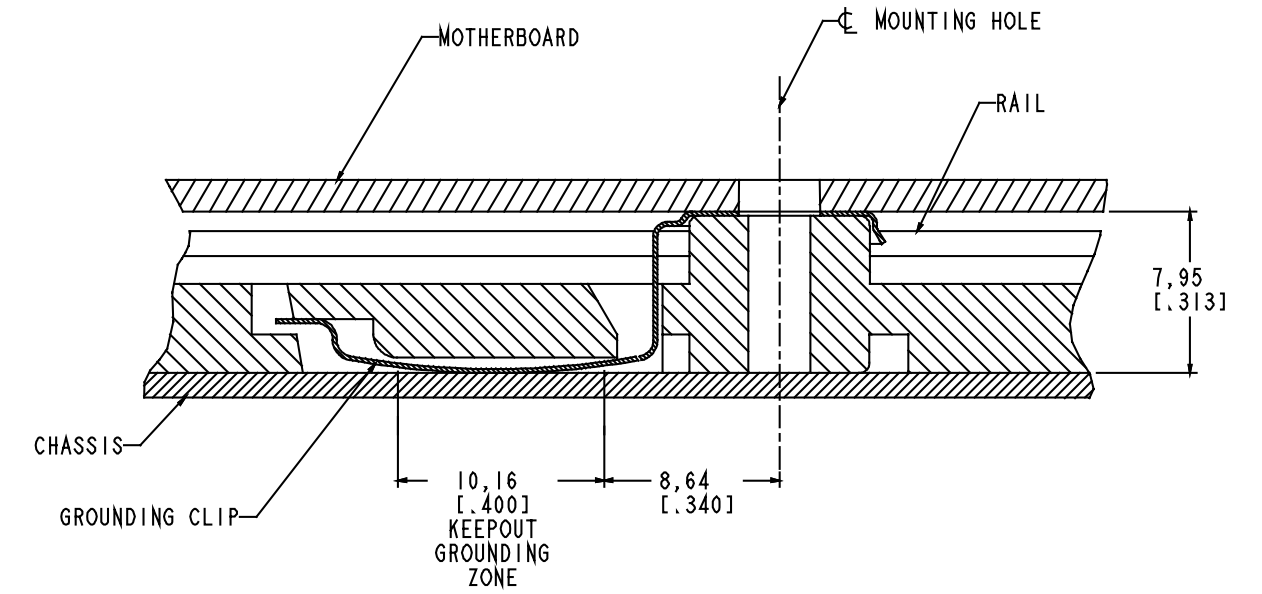

Figure 11. Rail Section View of Ground Pad

3.3 NLX Card Edge Connectors

The primary NLX card edge connector on the motherboard consists of a 340 (2x170) position gold finger contact (1.00mm pitch). The first gold finger center location begins 2.787 inches from the back of the motherboard and is detailed in Figures 12, 13, and 14. The mating connector for this card edge connector is Molex # 71796-0003, AMP # 145275-1, or equivalent.

An optional supplemental connector, is also defined. If the motherboard designer is not implementing the supplemental connector, then this area must be notched to a depth of 0.460 inches. The NLX riser card must not contain components that interfere with the motherboard, or components on the motherboard. For details on the supplemental connector signals, refer to Section 7.7, “NLX Riser with Supplemental Connector Example.”

The seating depth of an NLX motherboard into the NLX card edge connector is defined to be the distance from the riser board primary surface to the edge of the NLX motherboard when fully inserted into the connector. This distance is .260 inches. The gold finger connector must have a minimum contact backout wipe within the connector for the upper and lower contacts of 0.99mm (.039 inches).

The total available mechanical lead-in, front to back, for both the connector and the card edge is 5.38mm [.211 inches]. If the motherboard is off-center from the connector by more than 2.69mm [.106 inches], a mechanical interference will occur.

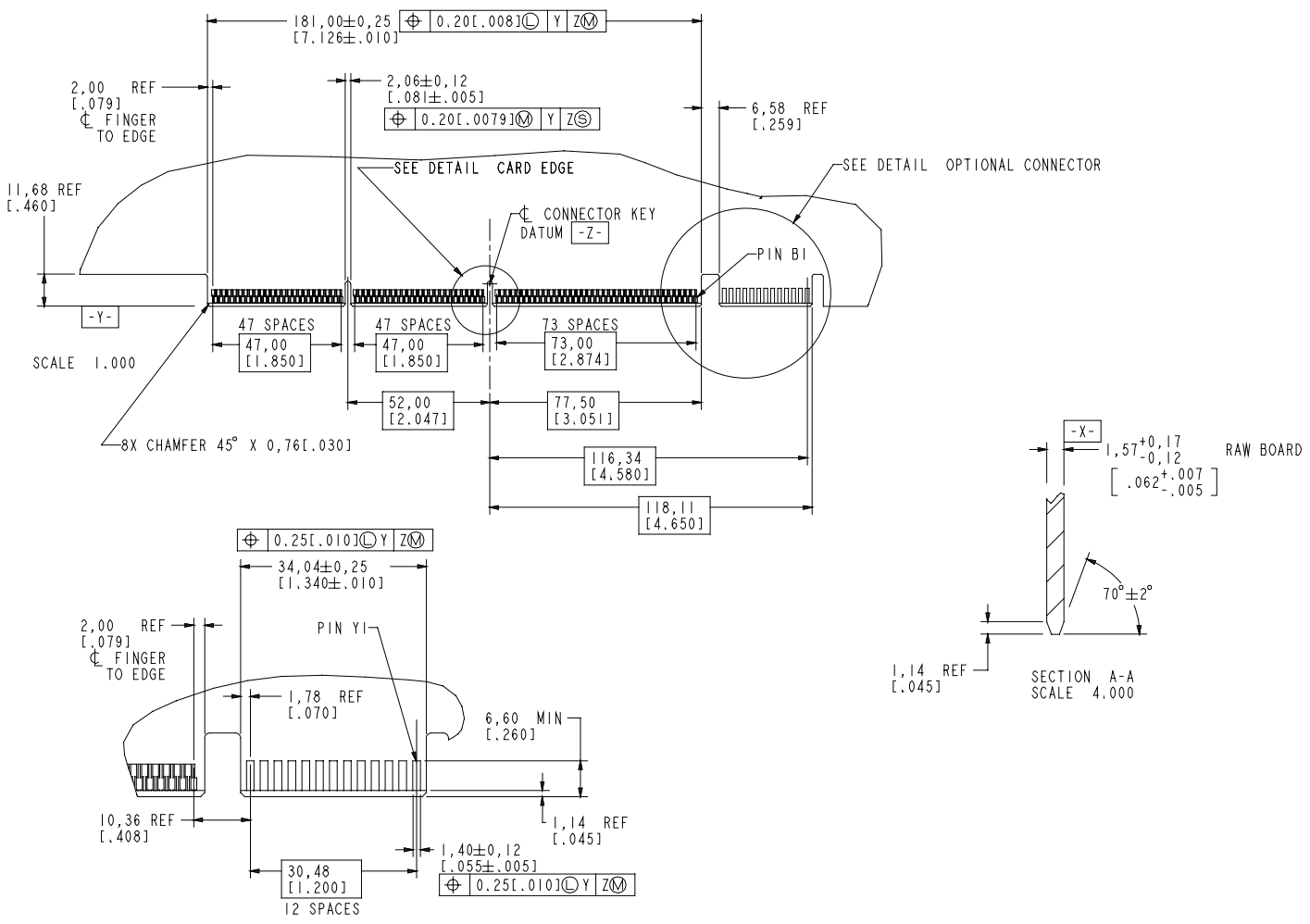

Figure 12. NLX Card Edge Detail, Primary (Top) Side

Notes:

1. Dimensioned with GDT (Geometric Dimensions and Tolerances) per ANSI Y14.5M.
2. See Figure 14 for pin location details.
3. Optional connector detail was changed to .260 Minimum from .300.
4. Sect A:-A: .045 Dimension was changed to REF.
5. The secondary key slot size was changed to 2.06 from 1.88 to prevent any insertion problems if the connector keys are the same size.

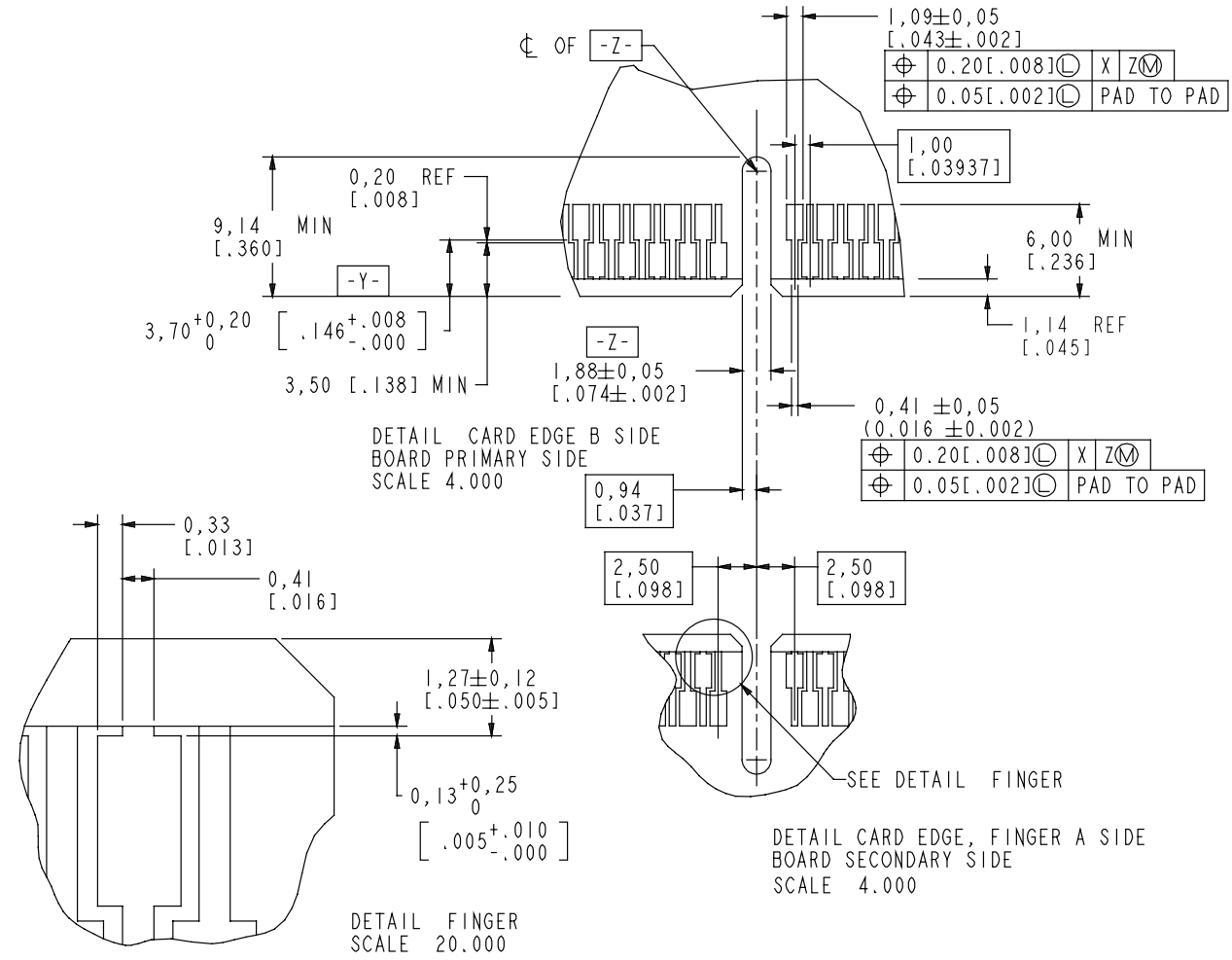

Figure 13. NLX Card Edge Detail

Notes:

1. Dimensioned with GDT (Geometric Dimensions and Tolerances) per ANSI Y14.5M.
2. See Figure 14 for pin location details.
3. Added detail view “Finger” with configuration to eliminate swipe while cutting chamfer.
4. Added key slot tolerance under Z.

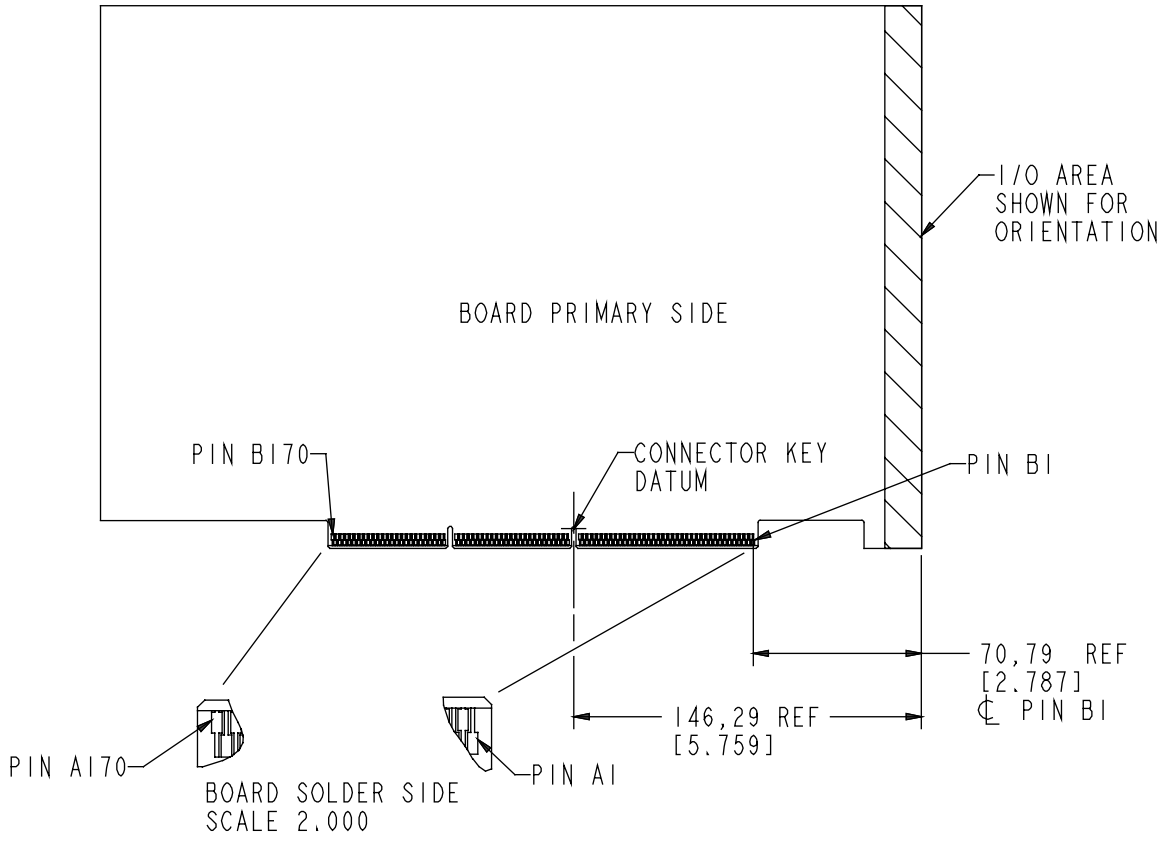

Figure 14. NLX Card Edge, Board View

Notes:

1. Picture update shows chamfer.
2. Pin number and location reference details are included.

3.3.1 I/O Signals Routed to the NLX Riser Card

To reduce the number of cables to the motherboard, NLX defines a comprehensive set of pins on the riser for I/O signals. Section 7 shows an example method to implement front panel features.

3.3.2 Disk I/O to the NLX Riser Card

The IDE and floppy disk drive connectors are supported on the NLX riser card. The IDE interface has two distinct sets of data, address, and control lines for the primary and secondary IDE connectors. This interface supports all IDE modes.

3.3.3 NLX Riser Card Design Considerations

Riser Mechanical Support: Validation testing has shown that the riser card must have adequate support directly behind the card edge connector to eliminate any torque of the riser card during motherboard insertion/extraction.

Connector and Card Edge Alignment: The system designer should ensure that there exists enough clearance in the system rails so the motherboard can align properly with the connector. If the guide holds the rail too tightly, the motherboard card edge may not easily guide into the riser card connector.

Alignment of the 340-pin Connector and the Supplemental Connector: Riser card designers should consider the tilt and alignment of the two independent connectors that mate with the motherboard. If these connectors tilt excessively, and in opposite directions, the resulting interference could cause board insertion difficulties.

Note

The maximum allowed connector tilt is 0.010 inches from the plane of the riser card for both the short and long axes (see Figure 15). Excessive tilts could cause board insertion difficulties and damages. Figure 15 shows tilts on both short and long axes.

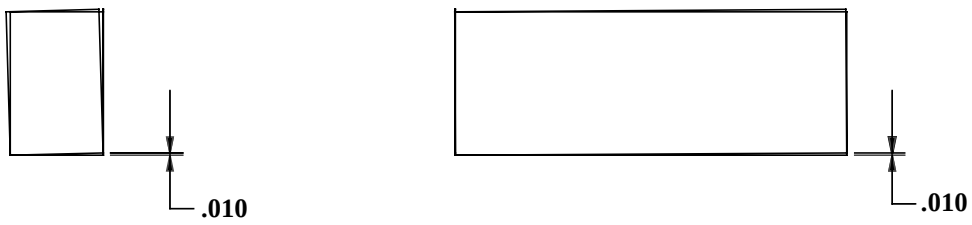

Figure 15. Maximum Recommended Connector Tilts for Riser Board Card Edge Connectors

(2X13-pin connector and 340-pin connector)

3.3.4 Reserved Space for Workstation/Server Performance Connector Definition

Standard NLX boards must have a reserved space at the front of the motherboard in line with, and in front of, the 340-pin connector. This space is shown in Figure 16. A future revision to the NLX specification will define a set of pins and a connector for use in this space by workstations and servers. Standard boards should not enter this space for ANY function, and designers should keep this area free of board fiberglass, components, and connectors.

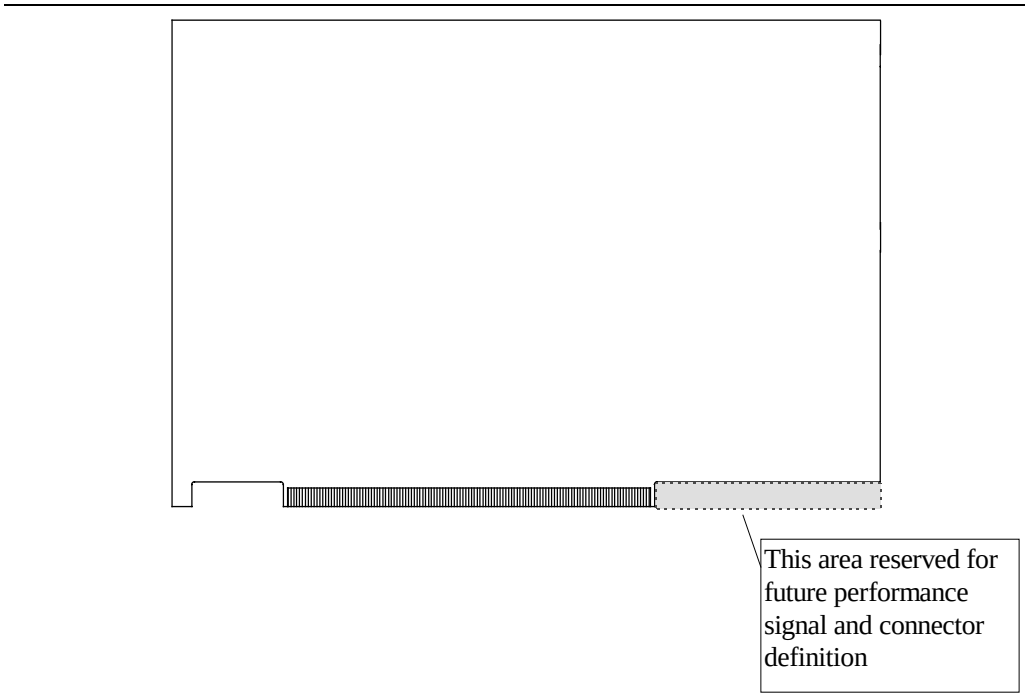

Figure 16. Reserved Space for Workstation/Server Performance Connector

3.4 PCI and ISA Card Support

Support for full length PCI and full length ISA cards is dependent on each vendor's chassis implementation, including their placement of the peripheral bays and power supply. The NLX specification allows for support of full length PCI and full length ISA cards.

The NLX specification supports standard XT card height (4.20 inches). Taller AT cards may be supported in the NLX chassis that has expansion slots above the 2.8-inch keepout area.

3.5 Memory Sockets

The exact location of the memory sockets (SIMM, DIMM, or other type of connector) is not specified. Ideally, the sockets should be located to the left of the I/O cards, to eliminate component height restrictions. This location should also simplify memory upgrades through better user accessibility. The exact locations will be dictated by the processor and core logic placement requirements.

3.6 Processor

The exact location of the processor is not specified. Ideally, the processor should be located to the left of the I/O cards and toward the front of the motherboard. The exact location will be dictated by the core logic placement requirements. For the system to support full-length add-in cards, the maximum component height should be .700 inches in this area. Refer to Figures 18 and 19 and Section 3.8 to determine proper placement based on motherboard height restrictions.

3.7 AGP Support

The Accelerated Graphics Port (AGP) is a high performance, component-level interconnect targeted at 3D graphical display applications; the interconnect is based on a set of performance enhancements to the Peripheral Component Interconnect (PCI). Detailed information regarding the AGP specification can be found on the World Wide Web site at *www.agpforum.org*.

Supporting video down takes no special effort to comply with the NLX specification. To support an AGP expansion slot, the connector location and chassis opening must be specified for compatibility between the motherboards and chassis.

An "NLX-notched" AGP card with a reduced total height, from top surface of motherboard to top edge of card, has been defined in the AGP specification. This smaller AGP card is defined to fit in a low profile chassis. Some AGP cards may require special cooling requirements. It is recommended that the chassis designer refer to the AGP specification for more details and design implications.

Note

An NLX motherboard solution with an AGP connector must be a 9.00-inch wide board to fit into an NLX-compliant chassis. Motherboards without an AGP connector can vary in width from 8.00 inches to 9.00 inches. Figure 17 shows the required position of the AGP connector on the NLX motherboard.

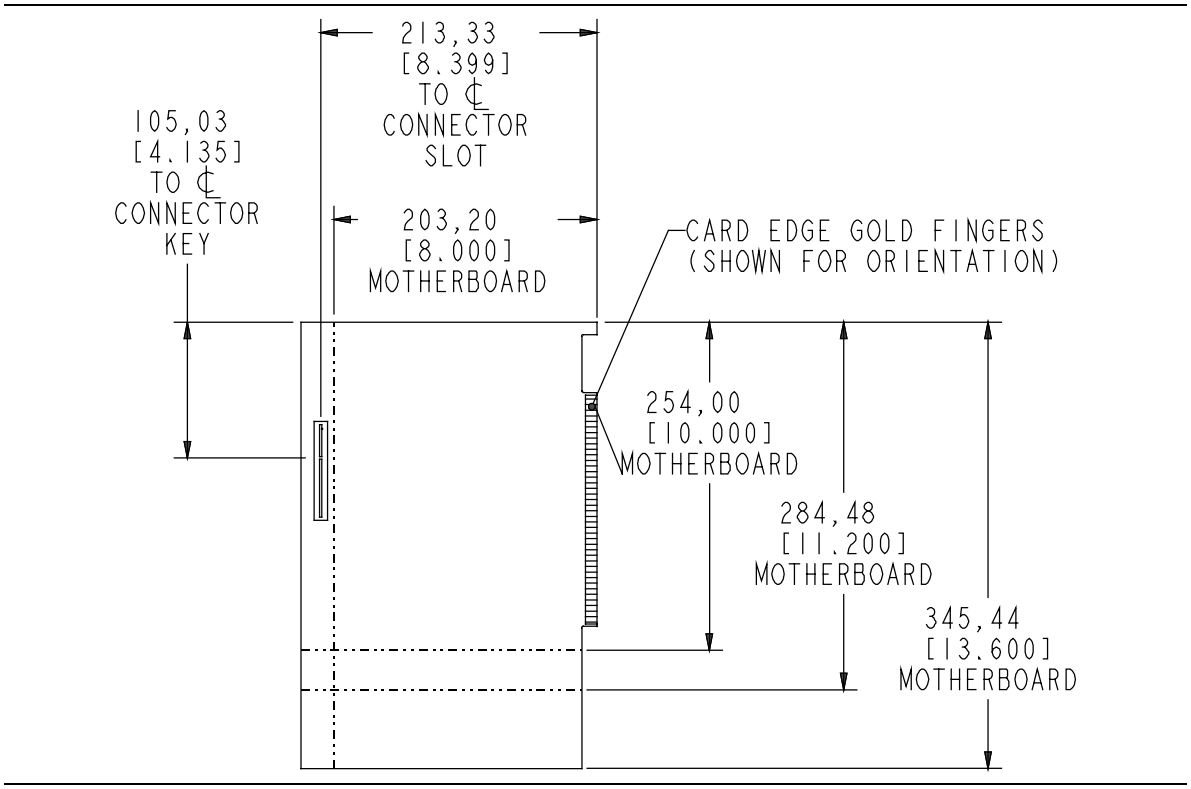

Figure 17. AGP Connector Pin 1 Location

Note: The AGP connector can be placed only on 9-inch wide motherboards.

3.8 Motherboard Component Height Constraints, Primary and Secondary Sides

Three figures show maximum height restrictions; the terms “left” and “right” in the text below refer to the orientation of the board in the following figures:

- Figure 18, motherboard primary side; design that supports AGP add-in card
- Figure 19, motherboard primary side; design that does not support AGP add-in card
- Figure 20, motherboard secondary side

The chassis designer should dimension the chassis with sufficient margin to accommodate dynamic excursions (vibration movements) of taller components.

3.8.1 Component Height, Motherboard Primary Side, Far Left

The far left side of the motherboard accepts a maximum component height of up to .600 inches [15.24 mm] in the area where an NLX AGP “notched” card would be present if an AGP connector is provided on a 9.000-inch wide motherboard. To support AGP, the NLX motherboard designer should not place any component taller than .600 inches [15.24 mm] in that area. The NLX chassis designer should refer to the AGP specification to determine how to support an AGP add-in card. Figure 18 shows the height restrictions for boards that support AGP cards.

For boards that do not support an NLX AGP “notched” card or are less than 9.000 inches wide, the maximum component height in this area is 2.800 inches [71.12 mm] and 1.750 inches [44.45 mm]. Figure 19 shows the height restrictions for boards that do not support AGP cards.

For detailed information about the Accelerated Graphics Port (AGP) specification and compliance, see the World Wide Web site at *www.agpforum.org*.

3.8.2 Component Height, Motherboard Primary Side, Mid Left

The front of the mid-left side of the motherboard accepts a component height of up to 2.80 inches, supporting placement of tall components such as processor modules and heat sinks. Care must be taken to ensure that placement of tall components does not block airflow past the processor heat sink.

The middle of the mid-left side of the motherboard accepts a component height of up to 1.75 inches, supporting placement of tall components, such as DIMM/SIMMs. This area of the board is not intended to support tall processor modules and heat sinks.

The back of the mid-left side of the motherboard accepts double-height stacked I/O connectors of up to 1.400 inches. The keepout zone is 1.430 inches, which leaves .030 inches clearance for the connectors.

3.8.3 Component Height, Motherboard Primary Side, Right Side Mid to Back

The right side mid-to-back section of the motherboard has a 0.70-inch height restriction, which allows the use of half-length add-in cards in all of the NLX expansion slots.

3.8.4 Component Height, Motherboard Primary Side, Right Side Mid to Front

Chassis/system designers should assume that a height keep-out restriction of 2.800 inches exists in the right side mid-to-front section of the motherboard (zone C). Motherboard designers should assume that a height keep-in restriction of .700 inches exists for components placed in this area. This restriction includes processors and associated retention mechanisms. It is not an absolute restriction, although encroachment into this area by either motherboard components or chassis/system features would restrict the bottom two expansion slots to half-length add-in cards.

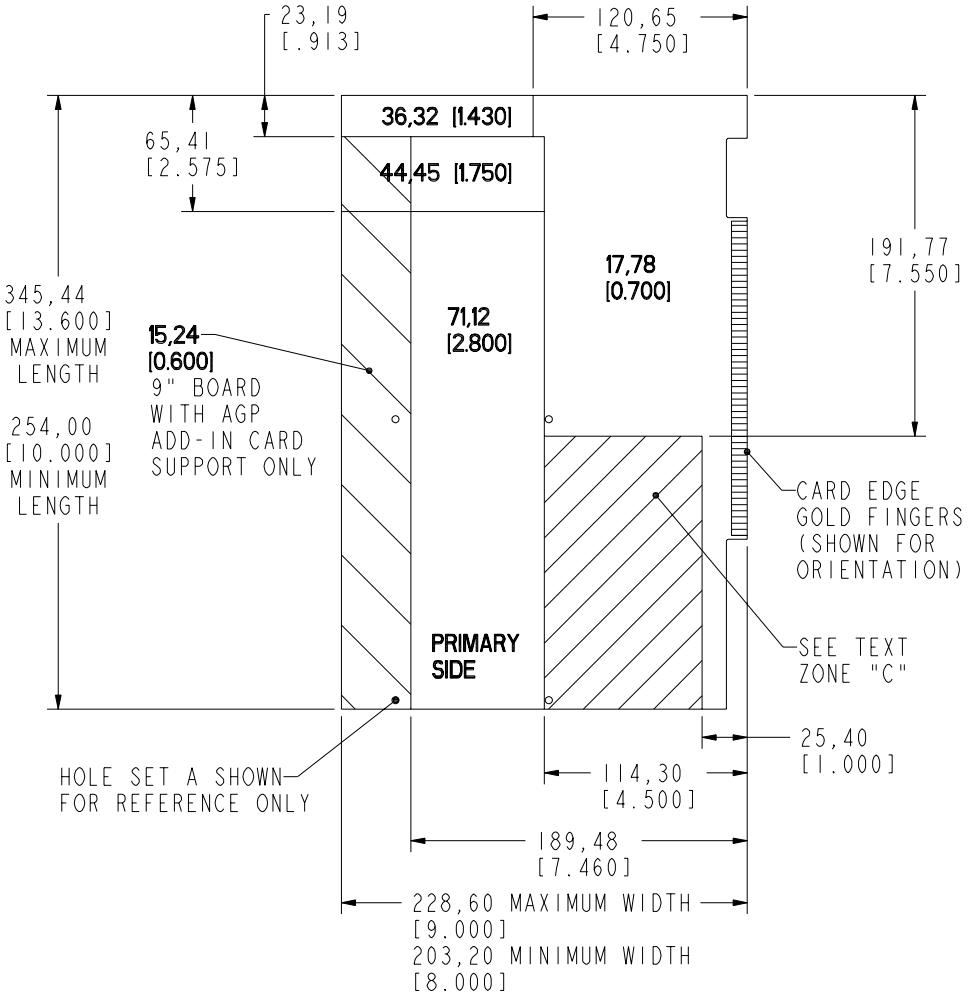

Figure 18. NLX Motherboard Primary Side Height Restrictions for a Design That Supports AGP Add-in Cards

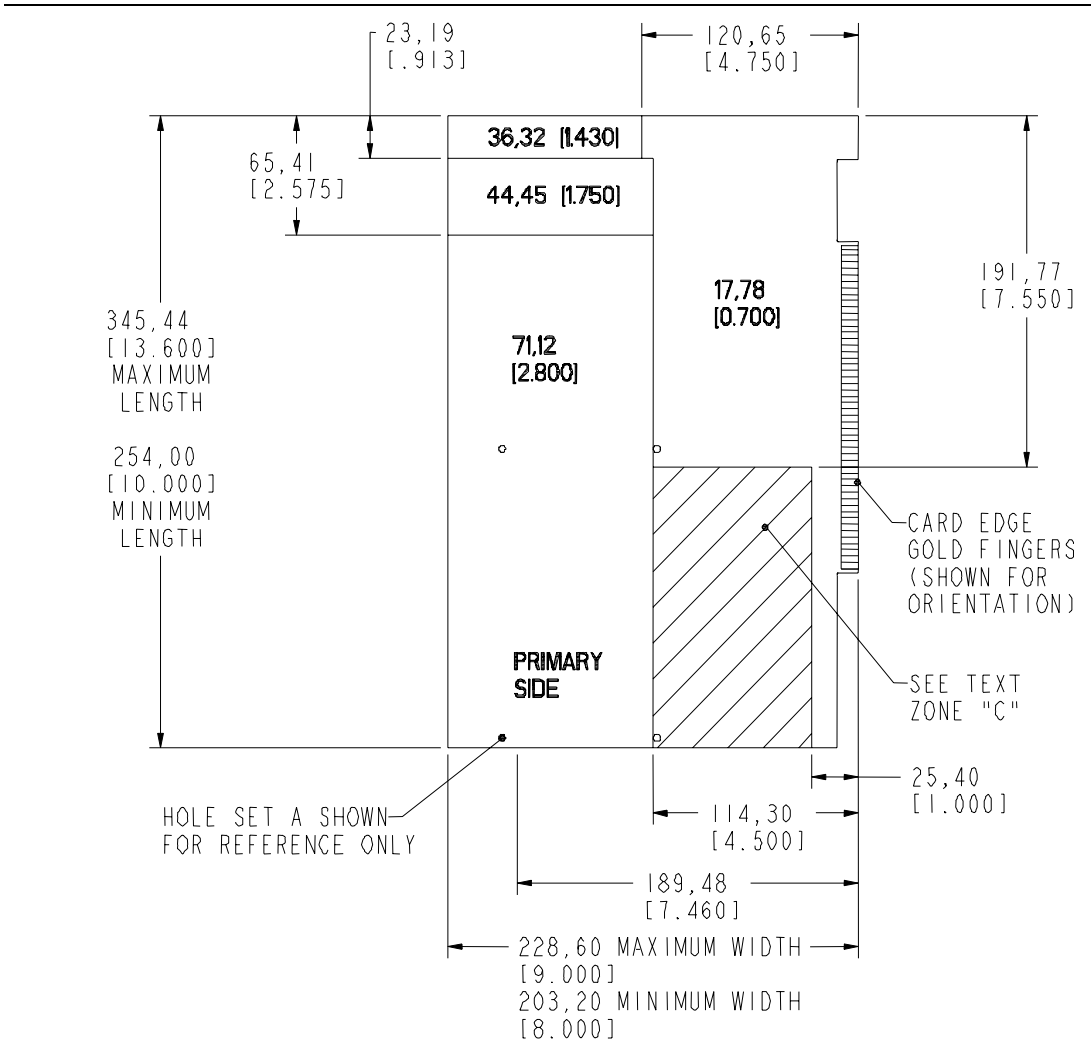

Figure 19. NLX Motherboard Primary Side Height Restrictions for a Design That Does Not Support AGP Add-in Cards

3.8.5 Motherboard Secondary Side

Figure 20 shows the maximum component height specification on the motherboard secondary side. Restricted zones D are highlighted (crosshatched).

Overall, the motherboard has a secondary side height restriction of 0.150 inches except in the restricted areas D, where the secondary side component height is limited to 0.120 inches (see Section 6.5, motherboard rails, for more details). The restricted zones D allow sufficient board-to-chassis clearances to allow for chassis features such as rail guides to be built directly into the chassis. (See Sections 6 and 7 for more information.)

To assure compliance with UL Enclosure requirements, it is highly recommended that the motherboard manufacturer not place secondary side components (active or passive) within the restricted D zones, shown in Figure 20.

For each motherboard dimension (and hence each set of motherboard mounting holes), the motherboard designer MUST also adhere to the secondary keepout zones as detailed in Section 3.1.4, "NLX Board Complete Keepout Specification."

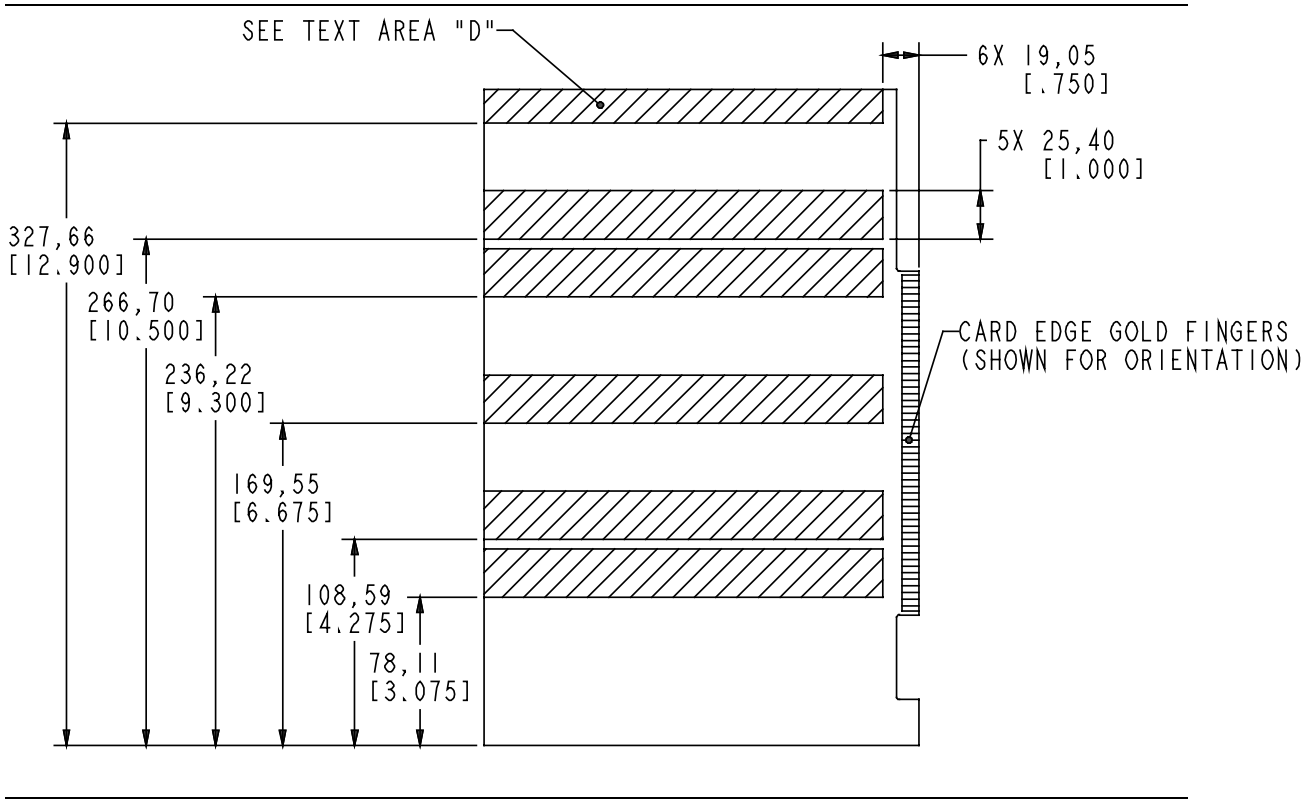

Figure 20. NLX Motherboard Secondary Side Component Height Restrictions

3.9 Back Panel I/O Shield

The NLX chassis must use the specified I/O shield opening to ensure that any NLX board will fit into any NLX chassis. The I/O shield opening is fully defined so the designer can define an I/O shield to fit into the standard NLX shield opening. The shield location relative to the motherboard is fully defined to ensure compatibility between board and chassis.

It is the responsibility of the system or board designer to provide mechanical support for the motherboard with the I/O shield.

3.9.1 Back Panel I/O Shield Opening Dimensions

The I/O shield opening is defined in Figure 21. The specification does not define the location of individual I/O connectors. However, it does limit the allowable area for motherboard connectors to protrude from the aperture. This area is defined in order to provide sufficient clearance between the connectors and the chassis opening for the I/O shield structure to make proper contact.

However, this specification does limit placement of the I/O connector to this extent: The motherboard supplier must ensure that there is sufficient clearance between the I/O connector, the connector housing, and the chassis to allow sufficient material in the I/O shield to make proper contact.

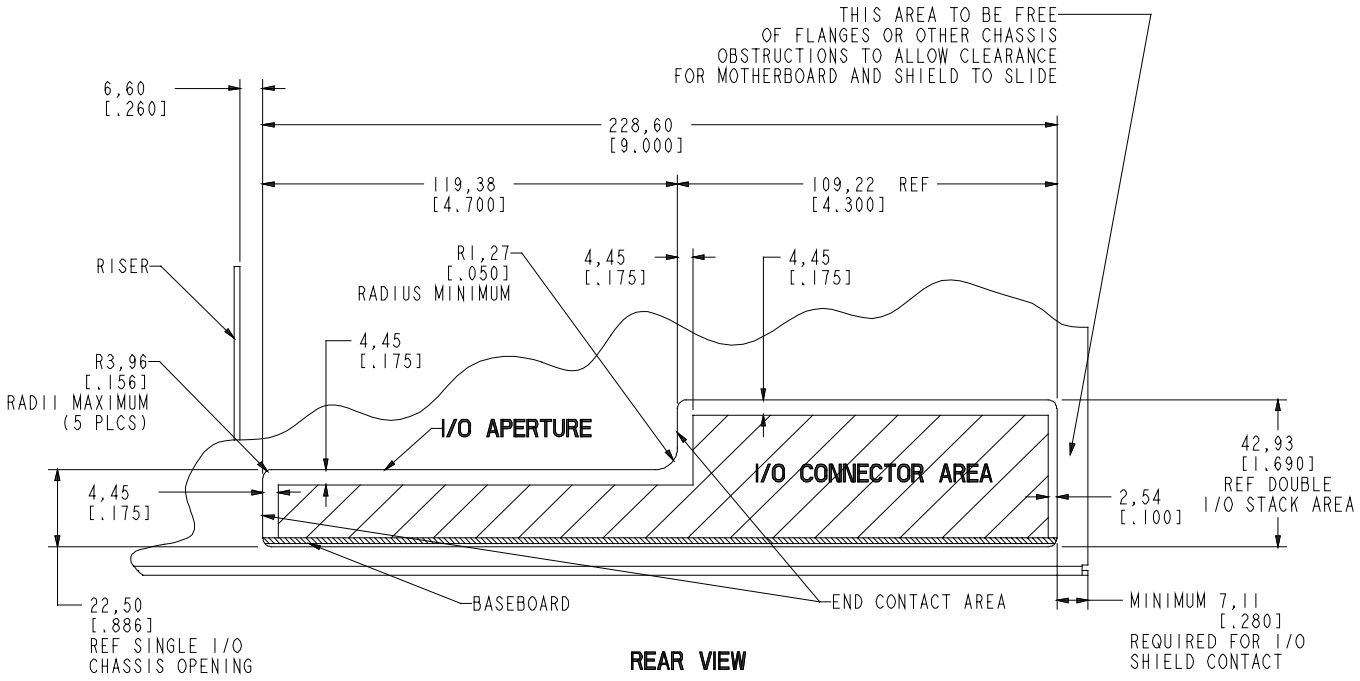

Figure 21. Chassis Back Panel I/O Shield Opening

3.9.2 Back Panel I/O Shield Side View

The NLX I/O shield side view is illustrated in Figures 22 through 24.

The I/O shield is surrounded by a flange used to provide EMI containment. EMI containment is discussed in more detail in the next section. The top of the I/O shield mates with a flat surface provided by the chassis back panel opening. The bottom of the I/O shield mates with the base of the chassis.

A flat surface on the chassis is required for all surfaces of the I/O shield. This chassis surface must be ***flat*** over the maximum top flange dimension; outside of this dimension, the chassis designer is free to implement any guide or alignment features desired. The surface of the chassis flange at the top of the I/O opening must be flat from the inside surface of the chassis to the beginning of the minimum top flange gap area. If it is desired to implement a guide or alignment feature for the I/O shield in this top flange, the chassis designer should ensure that any such feature does not interfere with the I/O shield where it meets the flange. The I/O shield will generally require a flat surface on the flange extending to the outer edge of the motherboard.

The areas used for end contact of the I/O shield are specified by surface size only, and the specific location of these contact surfaces is left to the designer. A good design will keep this area at a maximum and centered in the opening to the extent possible. To standardize a shield design, the dimensions flagged with an asterisk must be used. Also required is the minimum motherboard location dimension of 7.62mm[.300 inches]. A standard shield must fit between the back of the chassis and the board mounted connectors at the MINIMUM MOTHERBOARD LOCATION. This will limit the standard SHIELD FLANGE LENGTH to a maximum of 5.84mm[.230 inches] plus tolerance. Any deviation from the above mentioned dimensions may require the use of a chassis-specific shield.

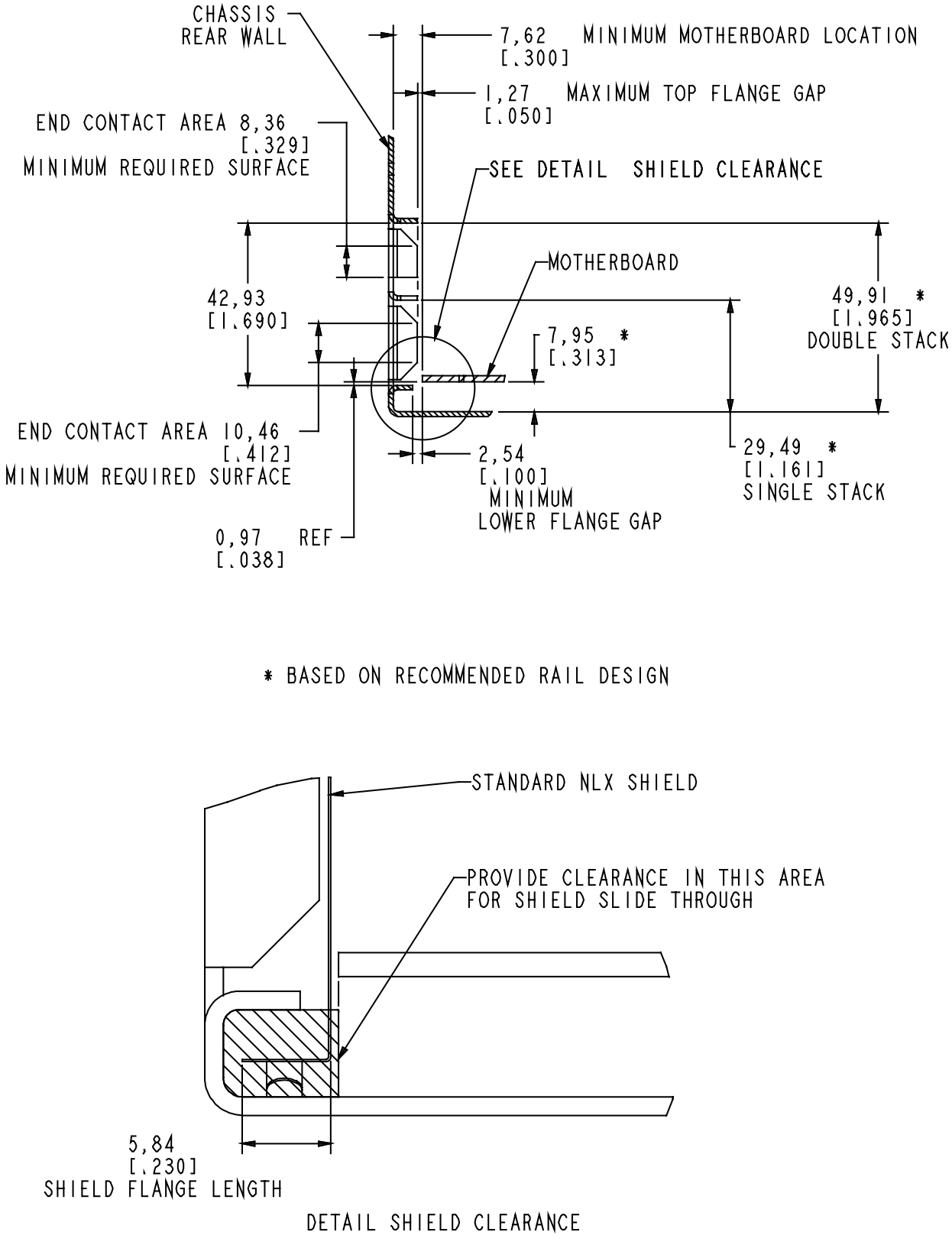

Figure 22. Side View of Back Panel Double High I/O Shield Opening Dimensions

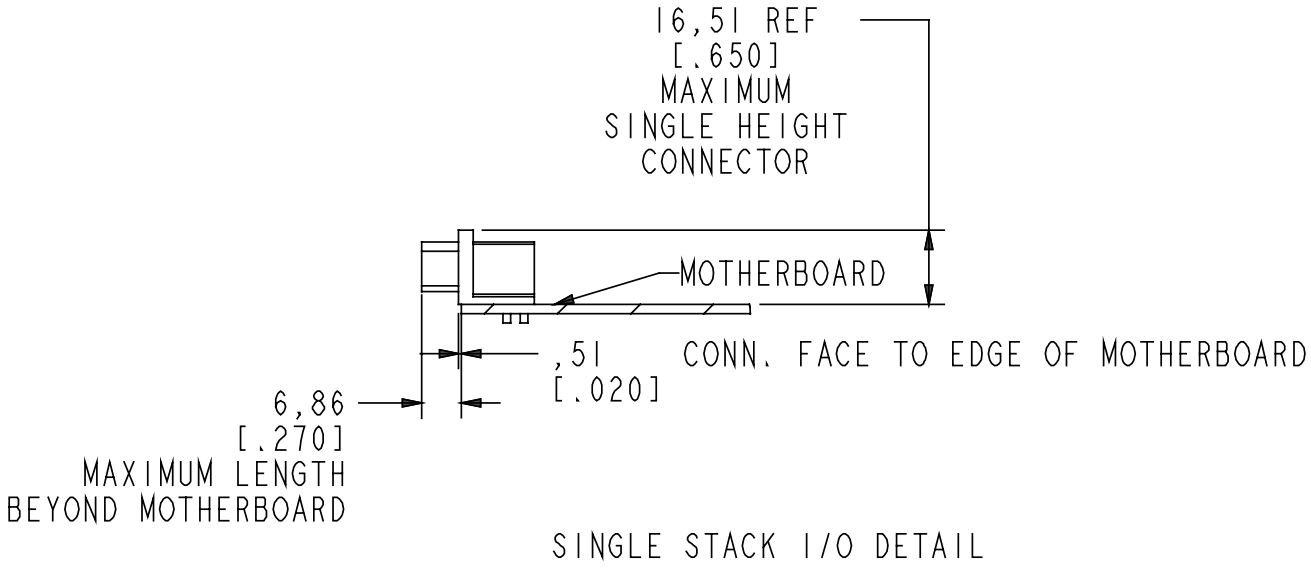

Figure 23. Side View of Single High I/O Shield Opening Dimensions

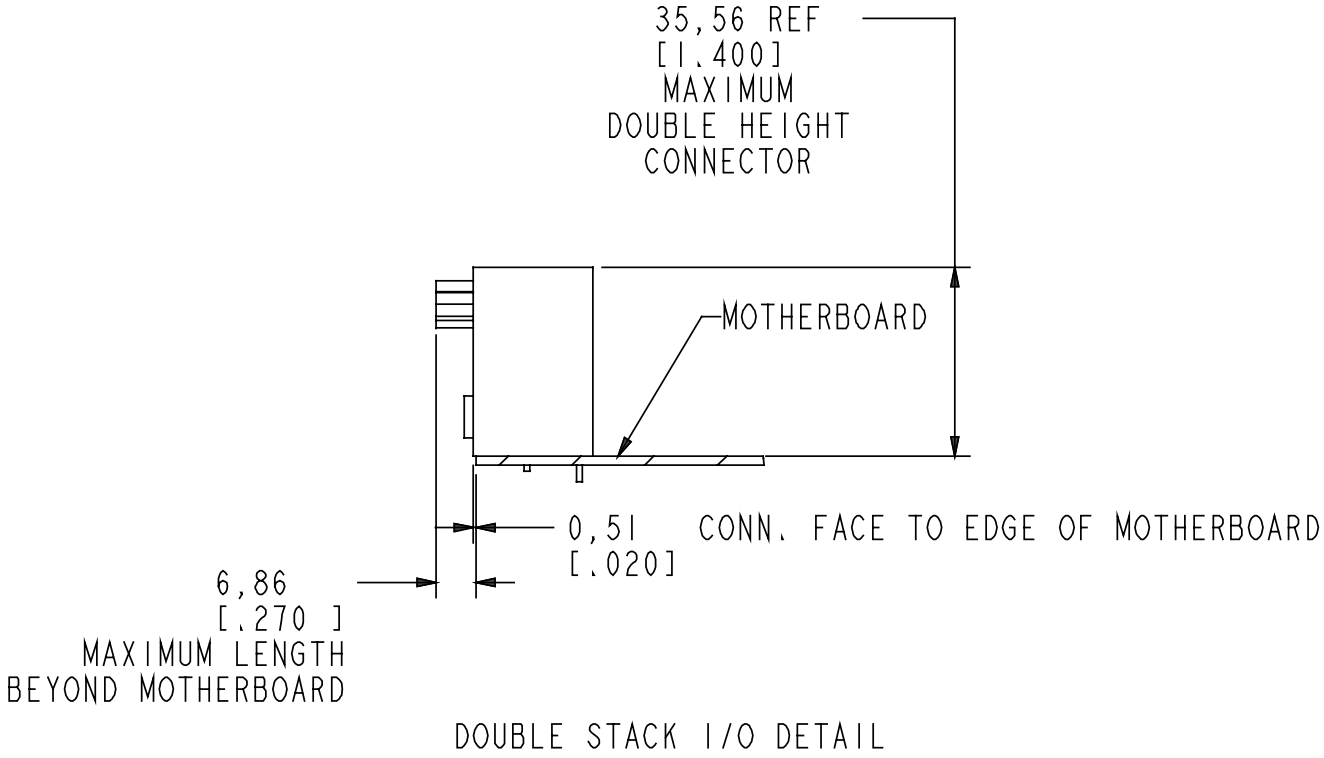

Figure 24. Side View of Double Stack I/O Shield Opening Dimensions

3.9.3 I/O Shield EMI Containment Contacts

The specific EMI containment implementation is left to the vendor.

The perimeter of the I/O shield should provide EMI containment by contacting the chassis. An NLX chassis will provide a flat surface that contacts the I/O shield. A flat, electrically conductive, clean surface must be provided for all six sides of the chassis I/O opening to be compliant with the NLX specification. These surfaces are:

- Top of the stacked area
- Top of the single height area
- Bottom contact area of the I/O shield
- Left end of the contact area of the I/O shield
- Back inside of the chassis at the double stack end of the I/O shield
- Side between the stacked and single height connector area

The method of contact between the I/O shield and the chassis is not specified. Spacing between the EMI contacts varies with the frequencies present inside the chassis. An EMI shield ***example*** is illustrated in Section 7.6. Note that this is only an example. The EMI shield design is left entirely up to the motherboard designer or system designer.

4. Riser Card Pinouts and Edge Connector Specifications

The NLX riser card has the IDE, floppy, and front panel connectors on the riser card, removing most cables from the motherboard.

The NLX riser card can support up to five PCI clocks and five PCI REQ/GNT# pairs. The number of ISA slots supported is not specified; it is determined by the system designer.

4.1 NLX Card Edge Connector

The NLX motherboard connects to the riser with a 340 pin (2x170) pin, 1mm pitch, card edge connector. The pinouts for the riser interconnect are listed in the tables in Section 4.1.1. The "A" side is the bottom (secondary) side of the motherboard, and the "B" side is the top (primary) side of the motherboard. Pin 1 is toward the back of the motherboard (back panel I/O connectors). See Figures 8 and 13 for connector placement relative to the motherboard.

4.1.1 NLX Card Edge Connector Pin Definitions

The tables in this section associate the NLX specification pin names with their functions and proper location on the card edge connector. The tables also describe front panel and miscellaneous signals.

⇒ **Note**

Support for all of the signals defined in the NLX riser definition is determined by each particular motherboard implementation. All motherboard functions are not necessarily supported by the riser, and likewise, all riser functions are not necessarily supported on the motherboard. An example of this is the NLX riser supporting two USB ports, whereas the motherboard may not support these ports across the NLX riser.

Requirements:

- PCI, ISA, Power, two IDE channels, one floppy, serial bus, and miscellaneous front panel signals
- Riser to supply up to 100 W of 5VDC power [1]
- Riser to supply up to 60 W of 3.3VDC power 1

[1] Additional motherboard power requirements are supported with additional power connectors on the motherboard.

Table 3. Audio Signals, Total of 2

Signal Group	Number of Signals
PC Speaker	2

Table 4. PCI Signals, Total of 69

Signal Group	Number of Signals
PCIINT0-3#	4
PCICLK	5
REQ/GNT0-4#	10
AD(0-31)	32
CBE(3-0)#	4
PCI MISC	14

Table 5. Power Pins/Signals, Total of 68

Signal Group	Number of Signals
5VDC	13
3.3VDC	13
SENSE3.3	1
-5V	1
-12V	1
+12V	3
Ground	31
Power Supply On/Off	1
Soft On/Off	1
Powergood	1
5VSB	1
3.3Vaux	1

Table 6. ISA Signals, Total of 88

Signal Group	Number of Signals
IRQ /DMA	26
ISA MISC	19
SD(0-15)	16
SA(0-19)	20
LA(17-23)	7

Table 7. IDE Signals, Total of 30 x 2 = 60

Signal Group	Number of Signals
ADDR, DATA	19
CONTROL	11

Table 8. Floppy Signals, Total of 19

Signal Group	Number of Signals
LOGIC/CONTROL	19

Table 9. Miscellaneous and Front Panel Signals, Total of 30

Signal Group	Number of Signals
Reserved	4
Infra-Red	5
Power LED	1
Front Panel Sleep	1
Modem Wake Up	1
LAN Wake Up	1
LAN Activity	1
Front Panel Reset	1
USB	6
Fan Control	4
Tamper Detection	1
VBAT	1
Message Waiting	1
Serial bus	2

Requirements:

Any required components such as pullup resistors must be placed on the riser unless otherwise stated in the miscellaneous and front panel signal descriptions (Section 4.1.2).

4.1.1.1 Riser Interconnect Pinout

Table 10. PCI Segment, Riser Interconnect Pinout

Pin	Signal Name	Type	I/O	Termination	Pin	Signal Name	Type	I/O	Termination
A1	-12V	PWR	NA	NA	B1	PCSPKR_RT	AUDIO	O	NA
A2	REQ4#	PCI	I	RIS	B2	+12V	PWR	NA	NA
A3	+12V	PWR	NA	NA	B3	PCSPKR_LFT	AUDIO	O	NA
A4	GNT4#	PCI	O	RIS	B4	+12V	PWR	NA	NA
A5	3.3VDC	PWR	NA	NA	B5	PCICLK0	PCI	O	MB
A6	PCIINT3#	PCI	I	RIS	B6	GND	PWR	NA	NA
A7	3.3VDC	PWR	NA	NA	B7	PCICLK1	PCI	O	MB
A8	PCIINT0#	PCI	I	RIS	B8	SER_IRQ	MISC	I/O	MB
A9	PCIINT1#	PCI	I	RIS	B9	PCIINT2#	PCI	I	RIS
A10	PCICLK2	PCI	O	MB	B10	3.3VDC	PWR	NA	NA
A11	3.3VDC	PWR	NA	NA	B11	PCICLK3	PCI	O	MB
A12	PCI_RST#	PCI	O	MB	B12	GND	PWR	NA	NA
A13	GNT0#	PCI	O	RIS	B13	GNT3#	PCI	O	RIS
A14	PCICLK4	PCI	O	MB	B14	3.3VDC	PWR	NA	NA
A15	GND	PWR	NA	NA	B15	GNT2#	PCI	O	RIS
A16	GNT1#	PCI	O	RIS	B16	AD[31]	PCI	I/O	RIS
A17	3.3VDC	PWR	NA	NA	B17	REQ0#	PCI	I	RIS
A18	REQ2#	PCI	I	RIS	B18	GND	PWR	NA	NA
A19	REQ3#	PCI	I	RIS	B19	AD[29]	PCI	I/O	RIS
A20	AD[30]	PCI	I/O	RIS	B20	AD[28]	PCI	I/O	RIS
A21	GND	PWR	NA	NA	B21	AD[26]	PCI	I/O	RIS
A22	AD[25]	PCI	I/O	RIS	B22	3.3VDC	PWR	NA	NA
A23	REQ1#	PCI	I	RIS	B23	AD[24]	PCI	I/O	RIS
A24	AD[27]	PCI	I/O	RIS	B24	C/BE[3]#	PCI	I/O	RIS
A25	3.3VDC	PWR	NA	NA	B25	AD[22]	PCI	I/O	RIS
A26	AD[23]	PCI	I/O	RIS	B26	GND	PWR	NA	NA
A27	AD[20]	PCI	I/O	RIS	B27	AD[21]	PCI	I/O	RIS
A28	AD[18]	PCI	I/O	RIS	B28	AD[19]	PCI	I/O	RIS
A29	GND	PWR	NA	NA	B29	AD[16]	PCI	I/O	RIS
A30	AD[17]	PCI	I/O	RIS	B30	3.3VDC	PWR	NA	NA
A31	IRDY#	PCI	I/O	RIS	B31	C/BE[2]#	PCI	I/O	RIS
A32	DEVSEL#	PCI	I/O	RIS	B32	FRAME#	PCI	I/O	RIS
A33	3.3VDC	PWR	NA	NA	B33	TRDY#	PCI	I/O	RIS
A34	STOP#	PCI	I/O	RIS	B34	GND	PWR	NA	NA

I/O column definitions relative to motherboard: O = Output from motherboard to riser
I = Input from riser to motherboard

Termination column definitions: MB = Termination/pullup/pulldown/debounce is on motherboard
RIS = Termination/pullup/pulldown is on riser card

NA = Not on motherboard or riser

Continued

Table 10, continued. PCI Segment, Riser Interconnect Pinout

Pin	Signal Name	Type	I/O	Termination	Pin	Signal Name	Type	I/O	Termination
A35	PERR#	PCI	I/O	RIS	B35	SDONE	PCI	I/O	RIS
A36	SERR#	PCI	I/O	RIS	B36	LOCK#	PCI	I/O	RIS
A37	GND	PWR	NA	NA	B37	SBO#	PCI	I/O	RIS
A38	C/BE[1]#	PCI	I/O	RIS	B38	3.3VDC	PWR	NA	NA
A39	AD[13]	PCI‘	I/O	RIS	B39	AD[15]	PCI	I/O	RIS
A40	AD[10]	PCI	I/O	RIS	B40	PAR	PCI	I/O	RIS
A41	GND	PWR	NA	NA	B41	AD[14]	PCI	I/O	RIS
A42	C/BE[0]#	PCI	I/O	RIS	B42	GND	PWR	NA	NA
A43	AD[00]	PCI	I/O	RIS	B43	AD[11]	PCI	I/O	RIS
A44	AD[06]	PCI	I/O	RIS	B44	AD[12]	PCI	I/O	RIS
A45	3.3VDC	PWR	NA	NA	B45	AD[09]	PCI	I/O	RIS
A46	AD[05]	PCI	I/O	RIS	B46	3.3VDC	PWR	NA	NA
A47	AD[01]	PCI	I/O	RIS	B47	AD[08]	PCI	I/O	RIS
A48	AD[03]	PCI	I/O	RIS	B48	AD[07]	PCI	I/O	RIS
A49	GND	PWR	NA	NA	B49	AD[04]	PCI	I/O	RIS
A50	AD[02]	PCI	I/O	RIS	B50	GND	PWR	NA	NA
A51	5VDC	PWR	NA	NA	B51	PCI_PM#	PCI	I/O	MB

I/O column definitions relative to motherboard: O = Output from motherboard to riser
I = Input from riser to motherboard

Termination column definitions: MB = Termination/pullup/pulldown/debounce is on motherboard
RIS = Termination/pullup/pulldown is on riser card

NA = Not on motherboard or riser

Table 11. ISA Segment, Riser Interconnect Pinout

Pin	Signal Name	Type	I/O	Termination	Pin	Signal Name	Type	I/O	Termination
A52	RSTDRV	ISA	O	MB	B52	5VDC	PWR	NA	NA
A53	IOCHK#	ISA	I	MB	B53	IRQ9	ISA	O	MB
A54	SD[6]	ISA	I/O	MB	B54	DRQ2	ISA	I	MB
A55	SD[7]	ISA	I/O	MB	B55	SD[3]	ISA	I/O	MB
A56	SD[4]	ISA	I/O	MB	B56	0WS#	ISA	I	MB
A57	5VDC	PWR	NA	NA	B57	SD[1]	ISA	I/O	MB
A58	SD[2]	ISA	I/O	MB	B58	AEN	ISA	O	MB
A59	SD[5]	ISA	I/O	MB	B59	IOCHRDY	ISA	I	MB
A60	SD[0]	ISA	I/O	MB	B60	SA[18]	ISA	I/O	MB
A61	SMEMW#	ISA	O	MB	B61	SMEMR#	ISA	O	MB
A62	SA[19]	ISA	I/O	MB	B62	SA[16]	ISA	I/O	MB
A63	IOW#	ISA	I/O	MB	B63	IOR#	ISA	I/O	MB
A64	SA[17]	ISA	I/O	MB	B64	DRQ3	ISA	I	MB
A65	GND	PWR	NA	NA	B65	SA[15]	ISA	I/O	MB
A66	DACK#3	ISA	O	MB	B66	GND	PWR	NA	NA
A67	SA[14]	ISA	I/O	MB	B67	SA[13]	ISA	I/O	MB
A68	DACK1#	ISA	O	MB	B68	5VDC	PWR	NA	NA
A69	DRQ1	ISA	I	MB	B69	REFRESH#	ISA	I/O	MB
A70	SA[12]	ISA	I/O	MB	B70	SA[11]	ISA	I/O	MB
A71	SYSCLK	ISA	O	MB	B71	SA[10]	ISA	I/O	MB
A72	SA[9]	ISA	I/O	MB	B72	IRQ7	ISA	I	MB
A73	5VDC	PWR	NA	NA	B73	IRQ6	ISA	I	MB
A74	IRQ5	ISA	I	MB	B74	SA[8]	ISA	I/O	MB
A75	SA[7]	ISA	I/O	MB	B75	SA[6]	ISA	I/O	MB
A76	IRQ3	ISA	I	MB	B76	DACK2#	ISA	O	MB
A77	IRQ4	ISA	I	MB	B77	SA[4]	ISA	I/O	MB
A78	SA[5]	ISA	I/O	MB	B78	GND	PWR	NA	NA
A79	TC	ISA	O	MB	B79	SA[3]	ISA	I/O	MB
A80	BALE	ISA	O	MB	B80	SA[2]	ISA	I/O	MB
A81	GND	PWR	NA	NA	B81	SA[1]	ISA	I/O	MB
A82	OSC	ISA	O	MB	B82	SA[0]	ISA	I/O	MB
A83	IOCS16#	ISA	I	MB	B83	SBHE#	ISA	I/O	MB
A84	MEMCS16#	ISA	I	MB	B84	LA[23]	ISA	I/O	MB
A85	IRQ11	ISA	I	MB	B85	LA[22]	ISA	I/O	MB
A86	IRQ10	ISA	I	MB	B86	LA[21]	ISA	I/O	MB
A87	IRQ15	ISA	I	MB	B87	LA[20]	ISA	I/O	MB

I/O column definitions relative to motherboard: O = Output from motherboard to riser
I = Input from riser to motherboard

Termination column definitions: MB = Termination/pullup/pulldown/debounce is on motherboard
RIS = Termination/pullup/pulldown is on riser card

NA = Not on motherboard or riser

Continued

Table 11, continued. ISA Segment, Riser Interconnect Pinout

Pin	Signal Name	Type	I/O	Termination	Pin	Signal Name	Type	I/O	Termination
A88	IRQ12	ISA	I	MB	B88	LA[19]	ISA	I/O	MB
A89	GND	PWR	NA	NA	B89	LA[18]	ISA	I/O	MB
A90	IRQ14	ISA	I	MB	B90	LA[17]	ISA	I/O	MB
A91	DRQ0	ISA	I	MB	B91	DACK0#	ISA	O	MB
A92	MEMR#	ISA	I/O	MB	B92	DACK5#	ISA	O	MB
A93	MEMW#	ISA	I/O	MB	B93	SD[8]	ISA	I/O	MB
A94	SD[9]	ISA	I/O	MB	B94	DACK6#	ISA	O	MB
A95	DRQ5	ISA	I	MB	B95	SD[10]	ISA	I/O	MB
A96	DRQ6	ISA	I	MB	B96	5VDC	PWR	NA	NA
A97	5VDC	PWR	NA	NA	B97	SD[11]	ISA	I/O	MB
A98	SD[12]	ISA	I/O	MB	B98	DRQ7	ISA	I	MB
A99	DACK7#	ISA	O	MB	B99	SD[13]	ISA	I/O	MB
A100	SD[14]	ISA	I/O	MB	B100	SD[15]	ISA	I/O	MB
A101	MASTER#	ISA	I	MB	B101	GND	PWR	NA	NA

I/O column definitions relative to motherboard: O = Output from motherboard to riser
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Termination column definitions: MB = Termination/pullup/pulldown/debounce is on motherboard
RIS = Termination/pullup/pulldown is on riser card

NA = Not on motherboard or riser

Table 12. IDE, Floppy, and Front Panel Section, Riser Interconnect Pinout

Pin	Signal Name	Type	I/O	Termination	Pin	Signal Name	Type	I/O	Termination
A102	IDEA_DD8	IDE	I/O	MB	B102	GND	PWR	NA	NA
A103	IDEA_RESET#	IDE	O	MB	B103	IDEA_DD7	IDE	I/O	MB
A104	IDEA_DD9	IDE	I/O	MB	B104	IDEA_DD6	IDE	I/O	MB
A105	5VDC	PWR	NA	NA	B105	IDEA_DD5	IDE	I/O	MB
A106	IDEA_DD4	IDE	I/O	MB	B106	IDEA_DD11	IDE	I/O	MB
A107	IDEA_DD10	IDE	I/O	MB	B107	IDEA_DD12	IDE	I/O	MB
A108	IDEA_DD3	IDE	I/O	MB	B108	GND	PWR	NA	NA
A109	IDEA_DD13	IDE	I/O	MB	B109	IDEA_DD14	IDE	I/O	MB
A110	IDEA_DD1	IDE	I/O	MB	B110	IDEA_DD2	IDE	I/O	MB
A111	GND	PWR	NA	NA	B111	IDEA_DD0	IDE	I/O	MB
A112	IDEA_DIOW#	IDE	O	MB	B112	IDEA_DD15	IDE	I/O	MB
A113	IDEA_DMARQ	IDE	I	MB	B113	IDEA_DIOR#	IDE	O	MB
A114	IDEA_IORDY	IDE	I	MB	B114	IDEA_CSEL	IDE	O	MB
A115	IDEA_DMACK#	IDE	O	MB	B115	IDEA_INTRQ	IDE	I	MB
A116	RESERVED	RES	NA	NA	B116	5VDC	PWR	NA	NA
A117	IDEA_DA2	IDE	O	MB	B117	IDEA_DA1	IDE	O	MB
A118	IDEA_CS0#	IDE	O	MB	B118	IDEA_DA0	IDE	O	MB
A119	5VDC	PWR	NA	NA	B119	IDEA_CS1#	IDE	O	MB
A120	IDEA_DASP#	IDE	I	RIS	B120	IDEB_DD8	IDE	I/O	MB
A121	IDEB_RESET#	IDE	O	MB	B121	IDEB_DD7	IDE	I/O	MB
A122	IDEB_DD9	IDE	I/O	MB	B122	GND	PWR	NA	NA
A123	IDEB_DD6	IDE	I/O	MB	B123	IDEB_DD10	IDE	I/O	MB
A124	IDEB_DD5	IDE	I/O	MB	B124	5VDC	PWR	NA	NA
A125	IDEB_DD11	IDE	I/O	MB	B125	IDEB_DD4	IDE	I/O	MB
A126	IDEB_DD12	IDE	I/O	MB	B126	IDEB_DD3	IDE	I/O	MB
A127	GND	PWR	NA	NA	B127	IDEB_DD13	IDE	I/O	MB
A128	IDEB_DD2	IDE	I/O	MB	B128	IDEB_DD14	IDE	I/O	MB
A129	IDEB_DD15	IDE	I/O	MB	B129	IDEB_DD1	IDE	I/O	MB
A130	IDEB_DIOW#	IDE	I/O	MB	B130	IDEB_DD0	IDE	I/O	MB
A131	IDEB_DMARQ	IDE	I	MB	B131	IDEB_DIOR#	IDE	O	MB
A132	IDEB_IORDY	IDE	I	MB	B132	IDEB_CSEL	IDE	O	MB
A133	GND	PWR	NA	NA	B133	IDEB_INTRQ	IDE	I	MB
A134	IDEB_DMACK#	IDE	O	MB	B134	IDEB_DA1	IDE	O	MB
A135*	3.3Vaux	PWR	O	NA	B135	IDEB_DA2	IDE	O	MB
A136	IDEB_DA0	IDE	O	MB	B136	IDEB_CS1#	IDE	O	MB
A137	IDEB_CS0#	IDE	O	MB	B137	IDEB_DASP#	IDE	I	RIS
A138	DRV2#	FLOPPY	GND	NA	B138	GND	PWR	NA	NA

I/O column definitions relative to motherboard: O = Output from motherboard to riser
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NA = Not on motherboard or riser

* Pin A135 is rated at 2A.

Continued

Table 12, continued. IDE, Floppy, and Front Panel Section, Riser Interconnect Pinout

Pin	Signal Name	Type	I/O	Termination	Pin	Signal Name	Type	I/O	Termination
A139	5VDC	PWR	NA	NA	B139	DRATE0	FLOPPY	O	NA
A140	RESERVED	RES	NA	NA	B140	FDS1#	FLOPPY	O	NA
A141	DENSEL	FLOPPY	O	NA	B141	FDS0#	FLOPPY	O	NA
A142	FDME0#	FLOPPY	O	NA	B142	DIR#	FLOPPY	O	NA
A143	INDX#	FLOPPY	I	RIS	B143	MSEN1	FLOPPY	I	NA
A144	FDME1#	FLOPPY	O	NA	B144	GND	PWR	NA	NA
A145	GND	PWR	NA	NA	B145	WRDATA#	FLOPPY	O	NA
A146	WE#	FLOPPY	O	NA	B146	TRK0#	FLOPPY	I	RIS
A147	STEP#	FLOPPY	O	NA	B147	MSEN0	FLOPPY	I	NA
A148	WP#	FLOPPY	I	RIS	B148	RDDATA#	FLOPPY	I	RIS
A149	HDSEL#	FLOPPY	O	NA	B149	DSKCHG#	FLOPPY	I	RIS
A150	SDA	MISC	I/O	MB	B150	GND	PWR	NA	NA
A151	SCL	MISC	O	MB	B151	IRSL0	MISC	I/O	NA
A152	FAN_TACH1	MISC	I	NA	B152	IRSL1	MISC	I/O	NA
A153	FAN_TACH2	MISC	I	NA	B153	IRSL2	MISC	I/O	NA
A154	FAN_TACH3	MISC	I	NA	B154	IRTX	MISC	I/O	NA
A155	FAN_CTL	MISC	I	NA	B155	IRRX	MISC	I/O	NA
A156	5VDC	PWR	NA	NA	B156	FP_SLEEP	MISC	I	MB
A157	USB1/3_N	MISC	I/O	Note 1	B157	FP_RST#	MISC	I	MB
A158	USB1/3_P	MISC	I/O	Note 1	B158	GND	PWR	NA	NA
A159	USB1/3_OC#	MISC	I	RIS	B159	PWRLED#	MISC	O	RIS
A160	USB2/4_N	MISC	I/O	Note 1	B160	PWOK	PWR	I	NA
A161	USB2/4_P	MISC	I/O	Note 1	B161	SOFT_ON/OFF#	PWR	I	MB
A162	USB2/4_OC#	MISC	I	RIS	B162	PS_ON#	PWR	O	NA
A163	GND	PWR	NA	NA	B163	LAN_WAKE	MISC	I	MB
A164	VBAT	MISC	O	RIS	B164	LAN_ACTVY_LED#	MISC	O	NA
A165	TAMP_DET#	MISC	I	MB	B165	MDM_WAKE#	MISC	I	MB
A166	MSG_WAIT_LED#	MISC	O	RIS	B166	RESERVED	RES	NA	NA
A167	RESERVED	RES	NA	NA	B167*	TPA-	1394	I/O	NA, Note 2
A168*	TPB+	1394	I/O	NA, Note 2	B168*	TPA+	1394	I/O	NA, Note 2
A169	5VSB	PWR	I	NA	B169*	TPB-	1394	I/O	NA, Note 2
A170	3.3VSENSE	PWR	O	NA	B170*	-5V	PWR	NA	NA

I/O column definitions relative to motherboard: O = Output from motherboard to riser
I = Input from riser to motherboard

Termination column definitions: MB = Termination/pullup/pulldown/debounce is on motherboard
RIS = Termination/pullup/pulldown is on riser card

NA = Not on motherboard or riser

Note 1: USB termination for EMI belongs on the riser close to the USG connector. Pulldown and series termination is on the motherboard.

Note 2: Four pins are assigned as differential pairs to implement 1394-1995 IEEE standard.

4.1.2 Miscellaneous and Front Panel Signals

Table 13. IDE, Floppy, and Front Panel Signal Descriptions

Signal	Pin	I/O	Description	Signal Type
Reserved				
RESERVED	A116	NA	These pins should not be used for any purpose. They are reserved to allow compatibility with future implementations of the interface; compatibility problems can result if these signals are misused.	NA
	A140	NA		NA
	A167	NA		NA
	B166	NA		NA
Infra-Red				
IRSL0	B151	O	These signals control and configure an infrared transceiver module.	5V TTL
IRSL1	B152	O		5V TTL
IRSL2	B153	O		5V TTL
IRTX	B154	O	Infrared serial output data.	5V TTL
IRRX	B155	I	Infrared serial input data.	5V TTL
LEDs				
PWRLED#	B159	O	Control signal for system power LED. A low level will signal the system is in a power on state, a high level will signal a power managed state. A current limiting series resistor (typ. Value 330 ohm) is located on the riser.	5V TTL
MSG_WAIT_LED#	A166	O	Control signal for telephony device to indicate a message is waiting. A low level will turn the LED on, and a high level will turn the LED off. A current limiting series resistor (typ. Value 330 ohm) is located on the riser.	5V TTL
LAN_ACTVY_LED#	B164	O	Control signal for a LAN Activity LED. A low level will turn the LED on and a high level will turn the LED off. A current limiting series resistor (typ. value 330 ohm) is located on the riser.	5V TTL
Front Panel Sleep				
FP_SLEEP	B156	I	This signal is driven from a front panel button to request a system level "sleep mode." This signal is active high. The motherboard provides debounce and pulldown resistor.	5V TTL
Front Panel Reset				
FP_RST#	B157	I	This signal is driven from a front panel button to request a system level reset. This signal is low level active. The motherboard provides debounce and pullup resistor.	Open drain
Modem Wake Up				
MDM_WAKE#	B165	I	A high to low transition of this signal will request a system "wake up." Note that activity may be initiated by a pulse train signal.	5V TTL
LAN Wake Up				
LAN_WAKE	B163	I	This signal, when pulsed high for at least 50ms, will request a system "wake up." When power is applied to the system, this signal must remain low.	5V TTL

I/O Column Definitions Relative to Motherboard: O = Output from motherboard to riser
I = Input from riser to motherboard

Continued

Table 13, continued. IDE, Floppy, and Front Panel Signal Descriptions

Signal	Pin	I/O	Description	Signal Type
USB				
USB1/3_N	A157	I/O	Universal Serial Bus Port. This signal pair comprises the differential data signal for a USB port. Refer to USB specification for more information.	per USB spec
USB1/3_P	A158	I/O		
USB2/4_N	A160	I/O	Universal Serial Bus Port. This signal pair comprises the differential data signal for a USB port. Refer to USB specification for more information.	per USB spec
USB2/4_P	A161	I/O		
USB1/3_OC#	A159	I	This signal is used to monitor the status of the USB power supply lines. This signal is low when an overcurrent condition exists on the USB power supply line and is high during normal operation. The riser contains the pull up resistors.	5V TTL
USB2/4_OC#	A162	I		
PC Speaker			Note: When mono audio is used, PCSPKR_LFT will function as the mono signal.	
PCSPKR_RT	B1	O	This signal pair provides the capability to drive a connector on the riser to which a speaker can be attached. Both speaker signals are DC driven on the motherboard, and can each drive 8 ohm speakers to ground.	application dependent
PCSPKR_LFT	B3	O		
Fan Control				
FAN_TACH1	A152	I	Signal from a fan tachometer to allow monitoring of fan speed. The motherboard must condition these signals to meet the input requirements of the monitoring device and the type of fan used.	0-12V max. open drain
FAN_TACH2	A153	I		
FAN_TACH3	A154	I		
FAN_CTL	A155	O	This signal is used to control fan RPM rate. The exact speed of the fans controlled by this signal will depend on the implementation. Because of this, the system designer should ensure that all of the system acoustics and cooling requirements are met when this signal is set for maximum fan speeds. This signal sets the fan's to maximum speed when the voltage potential on this pin is 10.5 volts or greater. This signal sets the fans to minimum speed (off) when this signal is 1volt or less. Fan speeds in between can be achieved by setting the voltage potential of this pin between 1 and +10.5 volts. The maximum current supplied by this pin is 50mA and is not meant to drive fans directly. Internal power supply fan driving circuitry has been allotted 20mA of the available 50mA from this signal. Remaining 30mA may be used for circuitry on riser or motherboard to drive other fans in the system. A 10K (minimum) pull up resistor to +12 Volts should be supplied on the riser card of the NLX system for FAN_CTL. This will ensure that as a default the fan control will be set to full speed	0-12V max.
Tamper Detection				
TAMP_DET#	A165	I	This signal indicates the state of an intrusion sensing device (switch or equivalent). This signal is low when the "chassis lid" is open indicating an intrusion. The signal should be open when the "chassis lid" is closed indicating normal operation. Debounce and associated circuitry is located on the motherboard.	Open drain

I/O Column Definitions Relative to Motherboard: O = Output from motherboard to riser
I = Input from riser to motherboard

Continued

Table 13, continued. IDE, Floppy, and Front Panel Signal Descriptions

Signal	Pin	I/O	Description	Signal Type
Serial bus				
SDA	A150	I/O	Serial data signal.	Open Drain
SCL	A151	O	Serial clock signal. Note: The NLX specification reserves EEPROM binary device address 1010111 for future riser configuration initiatives.	Open Drain
On / Off Control				
PS_ON#	B162	O	This signal controls the on/off state of the power supply. A low level will turn on the power supply, and a high level will turn off the power supply. The power supply provides a pullup to 5VSB.	CMOS open drain
SOFT_ON/OFF#	B161	I	System power on/off request signal. In an "off state," a low level pulse of at least 16ms indicates a switch on request. In an "on state," a low level pulse of at least 16ms indicates a switch off request. The motherboard provides debounce protection and a pullup resistor.	Open Drain Motherboard Specific
IEEE 1394†			See Figure 25 for further reference.	
TPA+	B168	I/O	IEEE 1394-1995 port. This signal pair comprises the differential data signal for a 1394 port. Refer to the 1394-1995 standards for more information. These pins are defined with respect to a 1394 PHY located on the motherboard. Risers implementing 1394 should have this taken into consideration in their design. *	Per IEEE standard 1394-1995
TPA-	B167	I/O		
TPB+	A168	I/O	IEEE 1394-1995 port. This signal pair comprises the differential data signal for a 1394 port. Refer to the 1394-1995 standards for more information. These pins are defined with respect to a 1394 PHY located on the motherboard. Risers implementing 1394 should have this taken into consideration in their design. *	Per IEEE standard 1394-1995
TPB-	B169	I/O		
PCI Power Management				
PCI_PM#	B51	I/O	This signal is used to change the power management state of PCI devices. Refer to the PCI Power Management specification for more information.	Open Drain

I/O Column Definitions Relative to Motherboard: O = Output from motherboard to riser
I = Input from riser to motherboard

* Speed requirements/capabilities for the 1394-1995 pin assignments depend on your specific implementation. Refer to the *IEEE Standard for a High Performance Serial Bus (1394-1995)* for more information.

The pullup and pulldown networks required for each differential pair must be placed close to the pins in the PHY. This also applies for repeater PHYs.

Continued

Table 13, continued. IDE, Floppy, and Front Panel Signal Descriptions

Signal	Pin	I/O	Description	Signal Type
Serial IRQ				
SER_IRQ	B8	I/O	This signal is used to implement a serial IRQ scheme to allow the reporting of ISA style interrupts over a single signal.	PCI TTL
Power				
PWOK	B160	I	This signal from the power supply is used to reset system logic and indicate proper operation of the power supply. During normal operation this signal is high; it is low during a fault condition or during power off.	5V TTL
VBAT	A164	O	Provides battery voltage to riser (battery is on the motherboard).	nom. 3V
3.3Vaux	A135	O	Provides 3.3V Standby power on the NLX riser.	3.3V TTL

I/O Column Definitions Relative to Motherboard

O = Output from motherboard to riser

I = Input from riser to motherboard

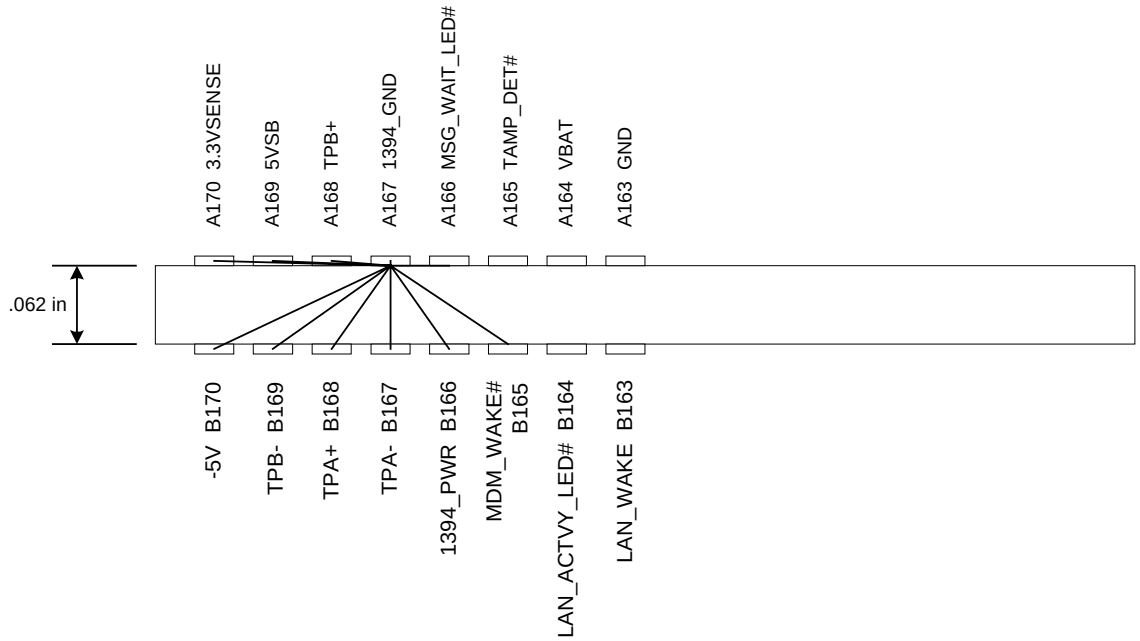

Figure 25. Riser Differential Pair Pins

5. NLX Motherboard Environmental, Safety, Regulatory, and Thermal Considerations

The NLX environmental considerations are specific to the motherboard. These considerations are not intended to be used at the system level.

5.1 Environmental

The following guidelines are suggested to ensure a high level of board/chassis synergy. They serve as a template of typical thermal, dynamic, and emissions targets that may be used in board and/or chassis development to create a system environment conducive to optimal motherboard (or system) performance, reliability, and service life. Close attention to motherboard/chassis interdependencies leads to a successful system solution.

5.1.1 Temperature Requirements

Storage temperature: -40°C to +70°C

Operational temperature: +10°C to +45°C

5.1.2 Board Shock

Unpacked 40 G trapezoidal waveform

Velocity change of 170 inches/second

Packaged Half sine 2 millisecond

5.1.3 Board Vibration

Unpacked: 5 Hz to 500 Hz ,3.1 gRMS random

Packed: 10 Hz to 500 Hz, 1.0 gRMS random

5.2 Safety

It is the responsibility of the system designer and/or board designer to provide the following safety requirements for their product.

UL 1950—CSA 950-95, 3RD EDITION, 28 JULY 1995

The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (USA and Canada)

CSA C22.2 NO. 950-93, 2ND EDITION

The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (Canada)

EN 60 950, 2ND EDITION, 1992 (WITH AMENDMENTS 1, AND 2)

The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (European Union)

IEC 950, 2ND EDITION, 1991 (WITH AMENDMENTS 1, 2, AND 3)

The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (International)

EMKO-TSE (74-SEC) 207/94

Summary of Nordic deviations to EN 60 950. (Norway, Sweden, Denmark, and Finland)

5.3 Regulatory Compliance

5.3.1 NLX CE Mark Compliance

Containment and suppression of EMI noise are the two general requirements for reducing EMI in a system. Containment of EMI usually centers around the chassis design, seams, and apertures. Suppression of noise generation centers around ground system design. The NLX Motherboard Specification is written to allow ground system design as either single-point grounding or multipoint grounding.

- The single-point grounding scheme may be possible using a slide-in I/O shield at the back of the chassis.
- The multipoint grounding scheme may be possible using a slide-in I/O shield and EMI clips attached to the motherboard. This scheme connects the motherboard's ground structure to the chassis at strategically located points.

5.3.1.1 Emissions

It is the responsibility of the system designer and/or board designer to provide the following emission requirements for their product.

CFR 47, Part 15, Subpart B, Class B

CISPR 22 (EN 55022) Class B.

5.3.1.2 Immunity

It is the responsibility of the system designer and/or board designer to provide the following immunity requirements for their product.

EN 50082-1:1992 Generic Immunity Requirement[2]

IEC 801-2:1984 ESD

IEC 801-3:1984 Radiated Electric Field

IEC 801-4:1988 EFT

5.3.1.3 Self Certified Emissions Compliance

It is the responsibility of the system designer and/or board designer to provide the Self Certified Emissions Compliance for their product.

Because of change in FCC Rules, a motherboard, which is considered a processor board, may now be self-certified or approved as a component to be used in systems assembled by integrators, which requires no further testing by meeting the following EMC specification with the chassis cover off:

CFR 47, Part 15, Subpart B, Class B + 3dB

5.4 NLX Thermal Recommendations

It is the responsibility of the system designer to provide a sufficient heat sink/airflow combination to cool the motherboard and processor. Please refer to manufacturer's component cooling specifications to determine system requirements.

[2] Subject to change.

6. Recommendations

6.1 Recommended IDSEL Assignments for PCI Slots and Onboard Devices

A board manufacturer can put a number of board devices on a motherboard. To avoid a conflict, the manufacturer must know which ID selects can be used for PCI slots. Figure 26 shows the PCI slot numbers, and Table 14 lists the recommended ID select assignments.

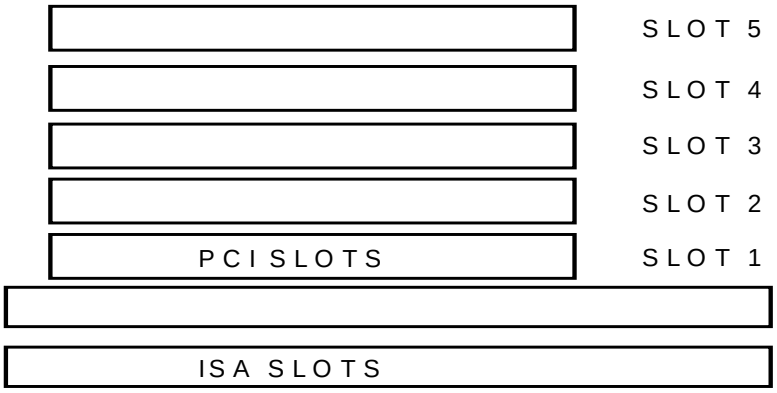

Figure 26. Recommended IDSEL Assignments (PCI Slot Numbers)

Table 14. Recommended IDSEL Assignments

Device number	AD line	Function
20	AD31	Slot 1
19	AD30	May not be used
18	AD29	Slot 2
17	AD28	May not be used
16	AD27	Slot 3
15	AD26	Free
14	AD25	Slot 4
13	AD24	Free
12	AD23	Slot 5 or PCI-PCI bridge for larger riser cards
11..6	AD22..17	Free
5	AD16	Reserved for AGP on board
4..1	AD15..12	Reserved for on board devices
0	AD11	Reserved for on board devices (e.g. motherboard chipset)

White 12 point font is recommended to clearly identify each PCI slot number on the riser card. Smaller white 8 point font is recommended to identify other connectors on the riser (e.g., label all of the power connector pins like +12V, -12V, +5V, -5V, +5VSB, GND, etc.).

6.2 Recommended INTA#..INTD# Interconnect at PCI Slots

BIOS uses a table to implement Plug and Play assignment of interrupts.

When the BIOS (as well as OS) assigns an interrupt to an add-in card, the BIOS must know exactly which INT pin is connected to the corresponding slot.

Table 15. Recommended PCI Interrupt Routing

Slot number	INT line	Connection to riser pin
1	INTA#	PCIINT0#
1	INTB#	PCIINT1#
1	INTC#	PCIINT2#
1	INTD#	PCIINT3#
2	INTA#	PCIINT1#
2	INTB#	PCIINT2#
2	INTC#	PCIINT3#
2	INTD#	PCIINT0#
3	INTA#	PCIINT2#
3	INTB#	PCIINT3#
3	INTC#	PCIINT0#
3	INTD#	PCIINT1#
4	INTA#	PCIINT3#
4	INTB#	PCIINT0#
4	INTC#	PCIINT1#
4	INTD#	PCIINT2#
5	INTA#	PCIINT0#
5	INTB#	PCIINT1#
5	INTC#	PCIINT2#
5	INTD#	PCIINT3#

6.3 PCI Implementation Issues

Because the high speed PCI bus exists on both the motherboard and riser, great care should be taken to ensure the integrity of the signals. Current simulations show, that to ensure signal integrity, a 33 ohm series termination resistor is recommended between the riser connector and the first I/O connector. Ideally this termination should be located as close to the riser connector as possible. Motherboard and riser vendors are encouraged to perform their own independent simulations that will help guide the choice and layout of components. Also, great care should be used in routing the PCI bus and clocks on the riser to ensure that trace length and signal skew are minimized.

6.4 Ultra DMA/33

It is recommended that NLX systems accommodating Ultra DMA/33 devices limit the IDE cable length to 12 inches for these devices.

6.5 Motherboard Rails—Mounting the Motherboard to Chassis

The NLX motherboard rail system enables the mechanical support required for new processors and the slide-in installation and removal of the motherboard. To ensure that any rail-mounted NLX motherboard can be inserted into any chassis design for NLX, the motherboard rail fully specified herein is recommended. Because each vendor is free to determine where in the assembly process the rails are installed, the rails are part of the chassis kit.

The rail design shown here is for plastic rails that contain a “ridge bumper” that contacts the motherboard but is not attached to it. The ridge bumper prevents the plastic rails from striking components during shipping. Metal rails, being stiffer, do not and must not have this ridge bumper, because it would damage secondary side motherboard traces.

- Figure 27 shows rail locations on the motherboard.
- Figures 28 and 29 show rail design side and section views, respectively.
- Figure 30 shows the latch view.

Figure 27 shows the rail features for attaching the rail to the motherboard and to the chassis. The rail flange geometry and position relative to the motherboard mounting holes are fully specified and fixed. This lets chassis manufacturers design chassis mounting schemes that will accept the rails on any given NLX board. A 0.140-inch clearance is defined between the top of the rail and the bottom of the motherboard for the length of the rails, except in the mounting hole locations, where the screw boss and support tabs exist.

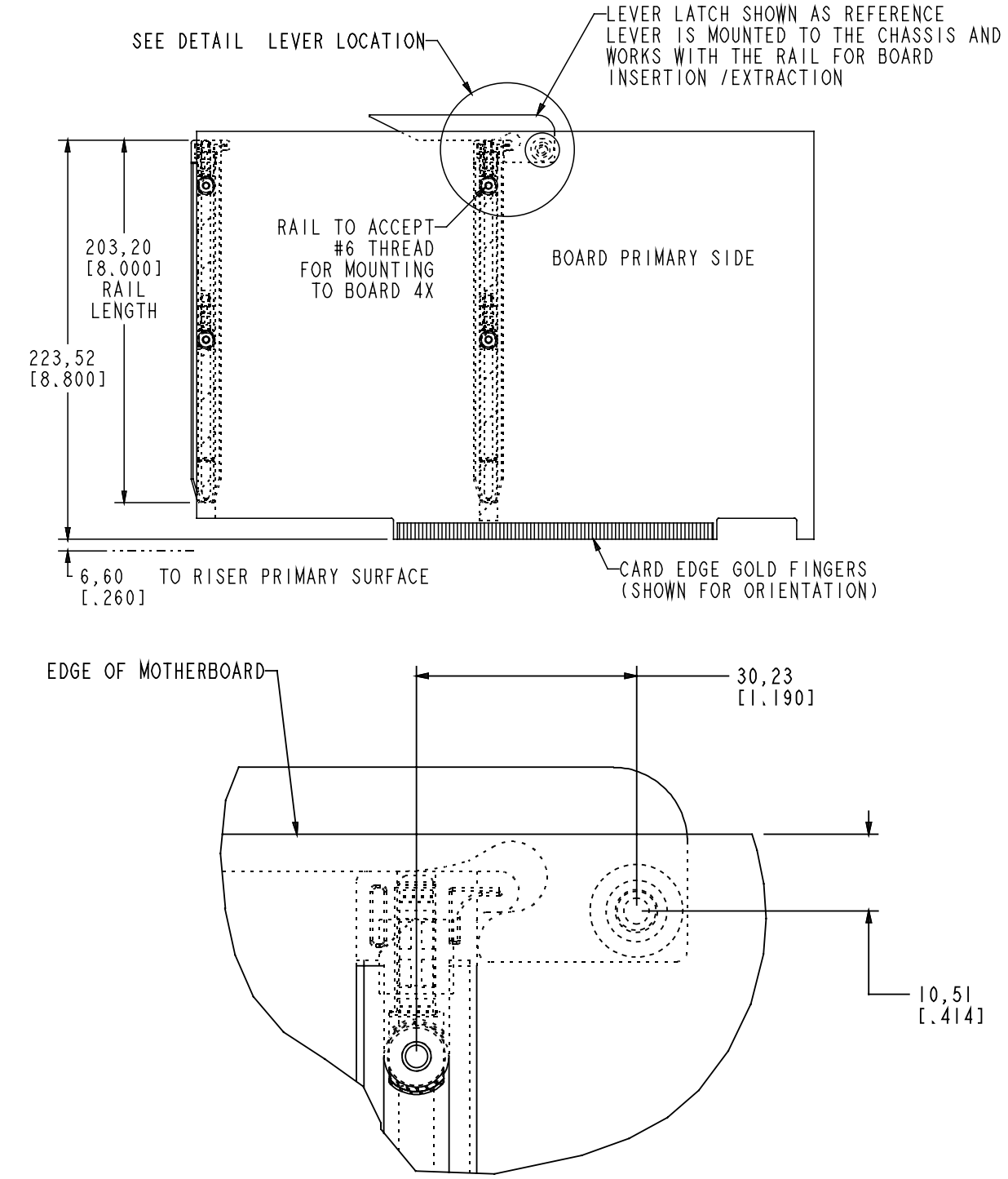

Figure 27. Rail Motherboard View

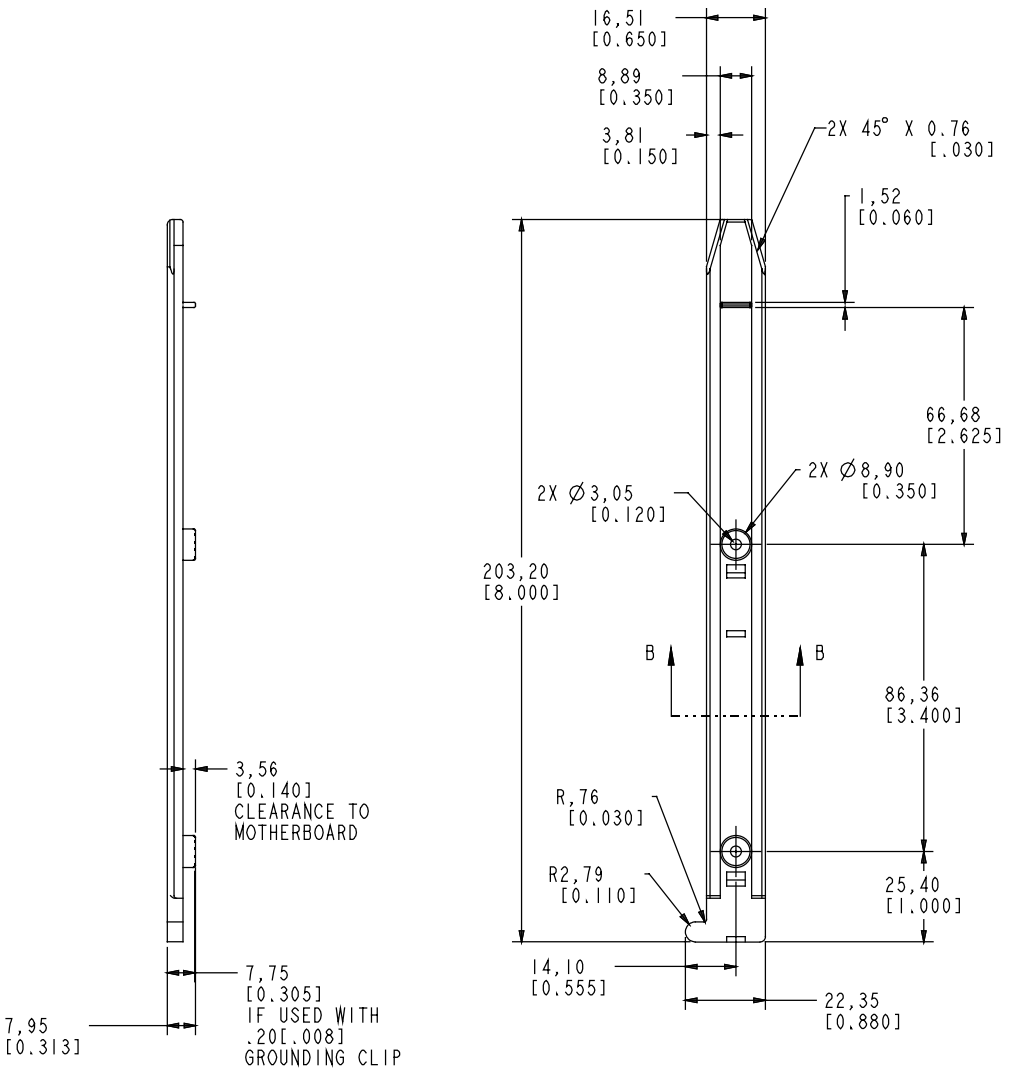

Figure 28. Rail Side View

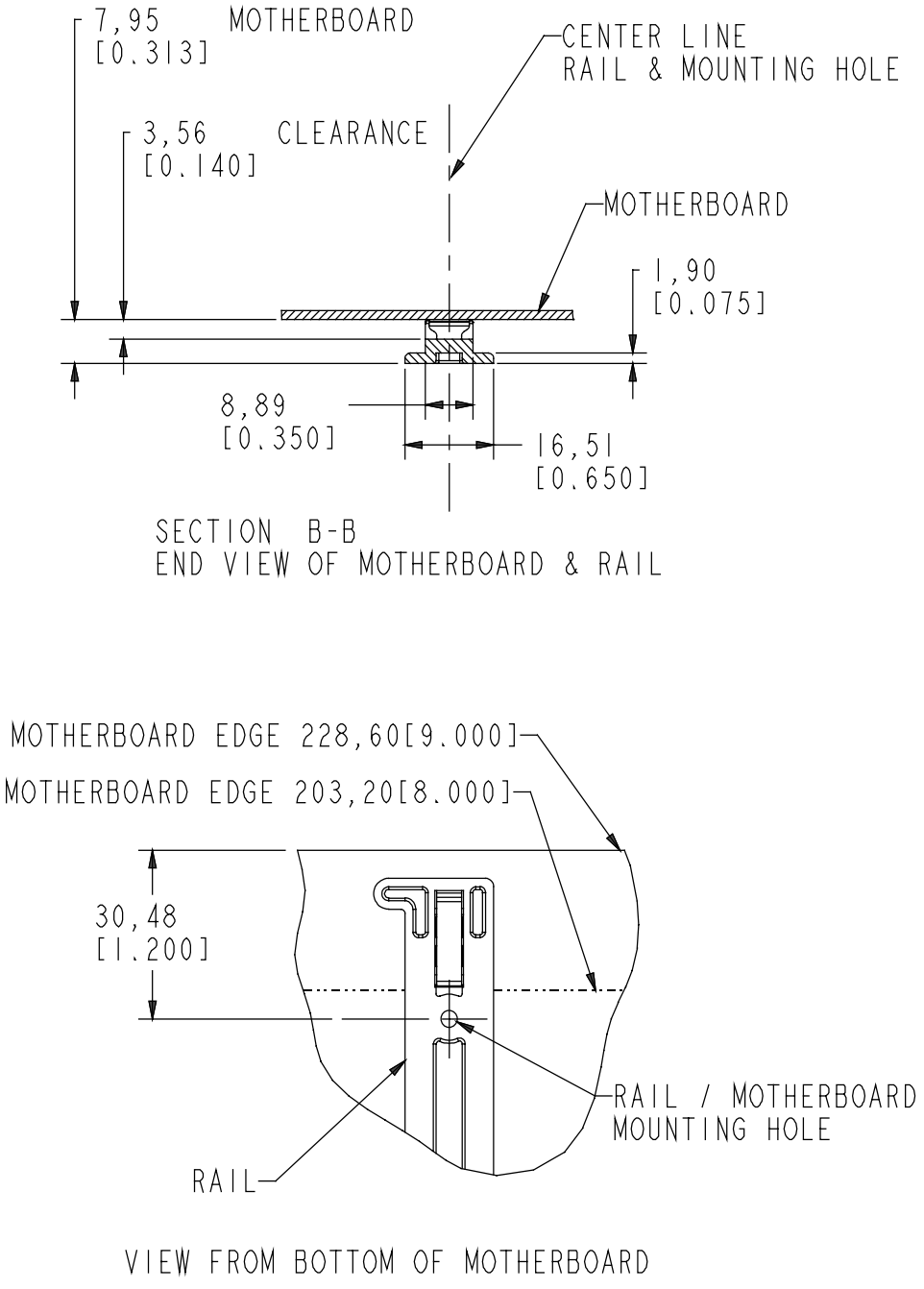

Figure 29. Rail Section View

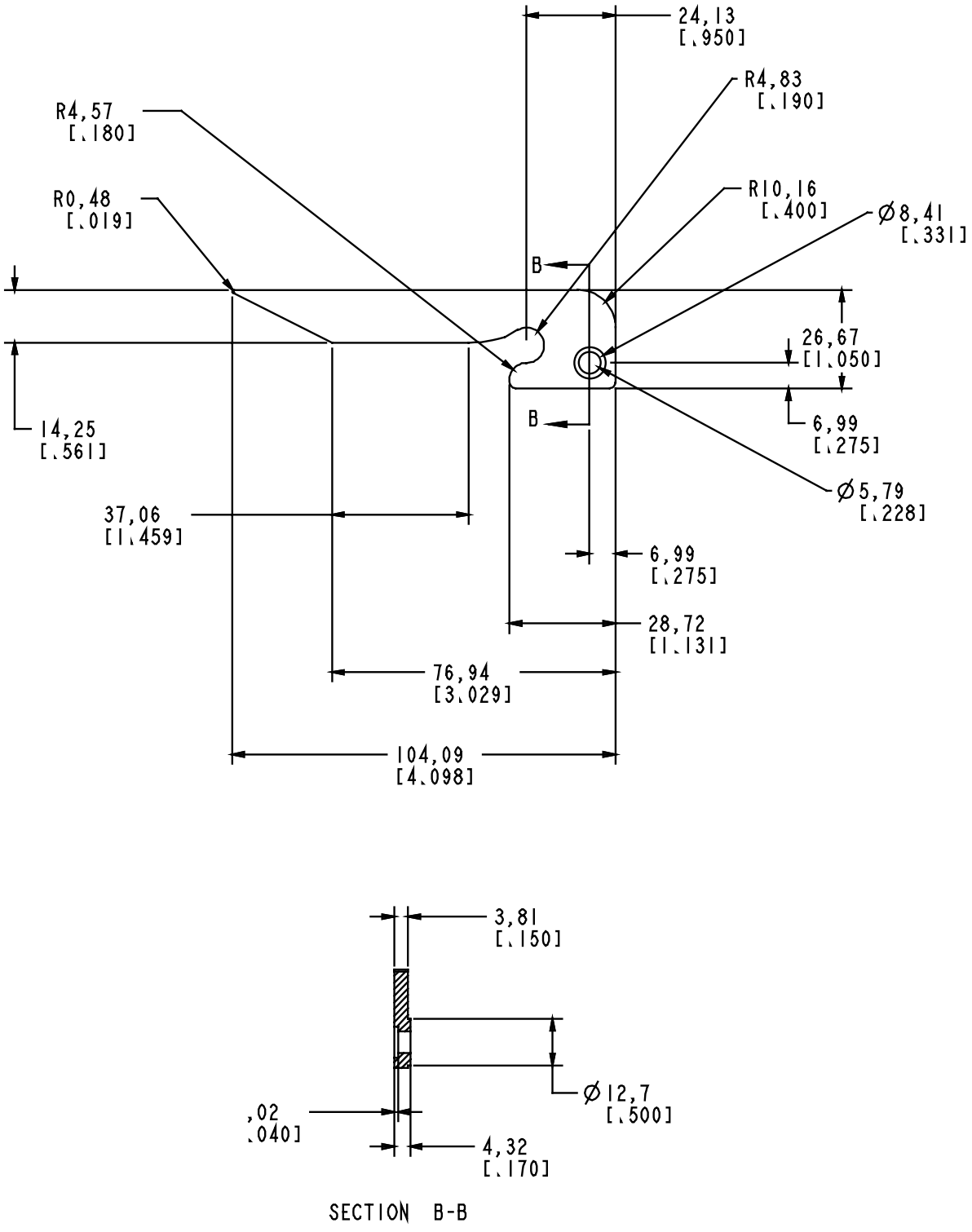

Figure 30. Latch View

6.6 NLX Motherboard Insertion and Extraction

The NLX motherboard is installed by sliding it into the riser already mounted to the chassis. The back of the motherboard is supported by the back panel I/O shield. The two rails guide the motherboard to the riser connector. It is recommended that NLX chassis designers include a visual alignment marking, such as an arrow or stamped line, on the base of the chassis such that it will align with the "connector key datum" on the motherboard in its proper insertion location. Refer to the NLX Card Edge, Board View, Figure 14. Motherboard designers may want to put a mark next to the "connector key datum" on the motherboard to make it easier for the installer to align the motherboard while inserting it. This will help the installer guide the rails into the chassis mounts. The rail system and a single lever latch work together to insert and remove the motherboard from the riser connector. The lever latch must be installed on the middle rail to provide sufficient leverage and to not interfere with the required chassis keepout areas for EMI clips. See Figure 34 for an example.

6.7 DC Voltage at the Motherboard

To assure proper motherboard operation, the NLX motherboard designer must know the voltage tolerances that will be supplied by the NLX riser to the motherboard. Table 16 lists the NLX specification recommendations for voltage requirements for the motherboard at the riser connection to ensure interoperability between NLX-compliant motherboards and risers.

NLX recommends the power supply connector be placed on the secondary side of the riser card, but the exact location of the connector is not specified. Refer to the *NLX Power Supply Recommendations* (a separate document) for details about potential NLX-compatible power supplies, including connector form-factors and pinouts, power requirements, etc.

Table 16. Recommended Voltage Tolerances for Motherboard at Riser Connection

Voltage	Tolerance
+5 VDC	±5 %
-5 VDC	±10 %
+12 VDC	±5 %
-12 VDC	±10 %
+3.3 VDC	±5 %
+5VSB	±5 %
+3.3Vaux	±4 %

7. Example Designs

7.1 Front Panel Support Example

Figure 31 shows an example of front panel I/O cabled from the riser card to the front panel. The connectors, switches, and indicators have been divided into two groups: standard I/O and high signal quality I/O. The first group includes the standard signals such as the power switch, power indicator, and fan and disk activity indicators. This group could use the standard header used on most motherboards today. Placement of these switches and indicators would be vendor-specific, and the same molded switch and indicator holders from previous chassis designs may be used.

The second I/O group could include USB or other I/O that may not be used on all systems. A PCB containing these I/O connectors and appropriate associated circuitry would be mounted to the front panel and cabled through a shielded cable back to the connector on the riser.

Advantages of the design shown in Figure 31:

- The same front panel header is used on many other motherboard designs.
- All the drive cables are on the riser, allowing for easier removal of the motherboard.
- Allows designs to have USB going out the front panel.
- Allows flexible options for front panel design.
- Designers can design their own cabling for the front panel.

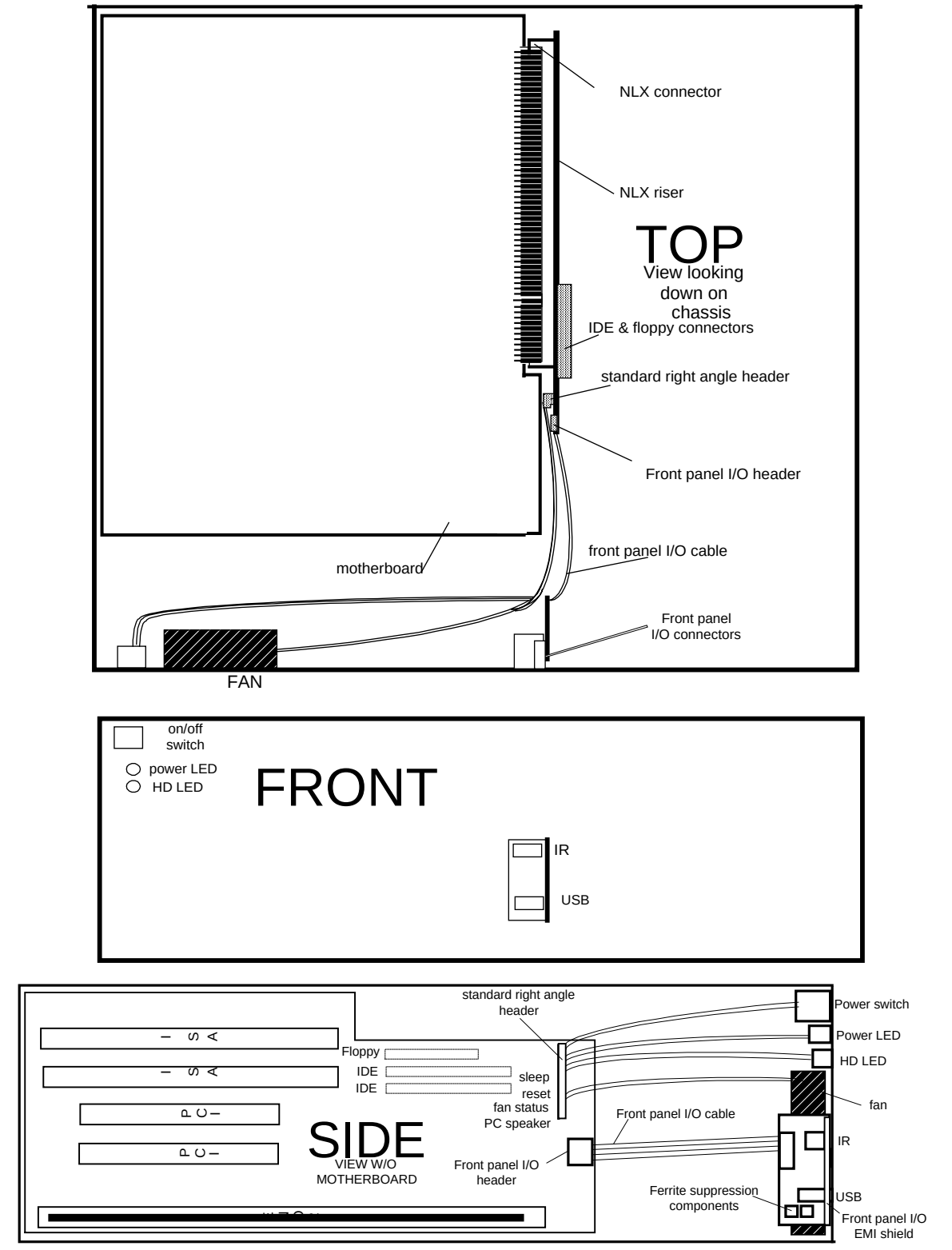

Figure 31. Front Panel Support Example

7.2 Riser Card Examples

Figures 32 and 33 show riser card examples. Actual NLX riser cards can extend longer; in these cases, the component/ feature restriction areas extend with the riser along its length to the ends. **See the notes for these figures on the next page.**

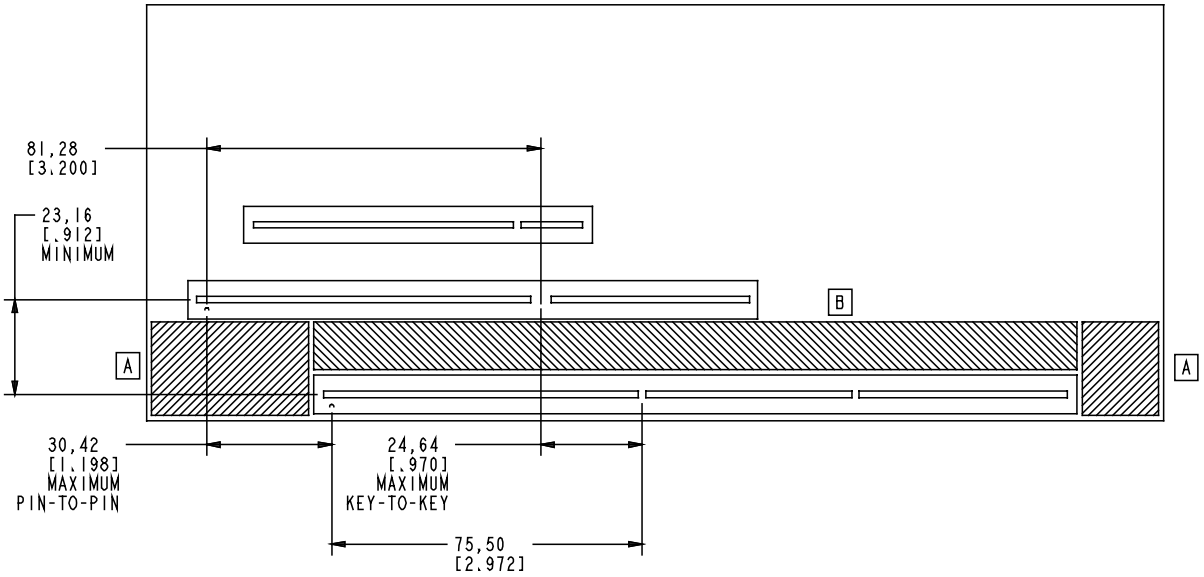

Figure 32. NLX Riser Example 1

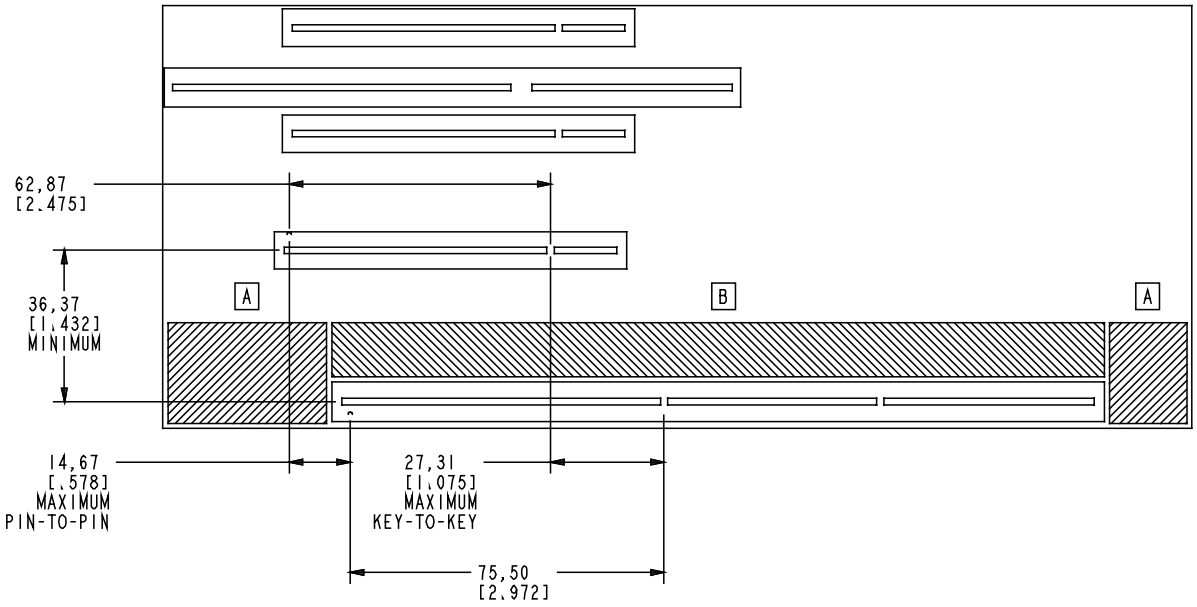

Figure 33. NLX Riser Example 2

Notes to Figures 32 and 33: Component heights are restricted to the following to ensure that riser card components do not interfere with motherboard components: **in Area A**, 0.200 inches maximum; **in Area B**, 0.600 inches maximum. Refer to Sections 3.3 and 3.8 and Figures 12 and 13 for details about component height restrictions in Areas A and B.

7.3 Chassis to Rail Assembly Example

Figure 34 shows an example chassis base with built-in rail guides. Rails are shown in the locations that would be used for the 13.6-inch motherboard.

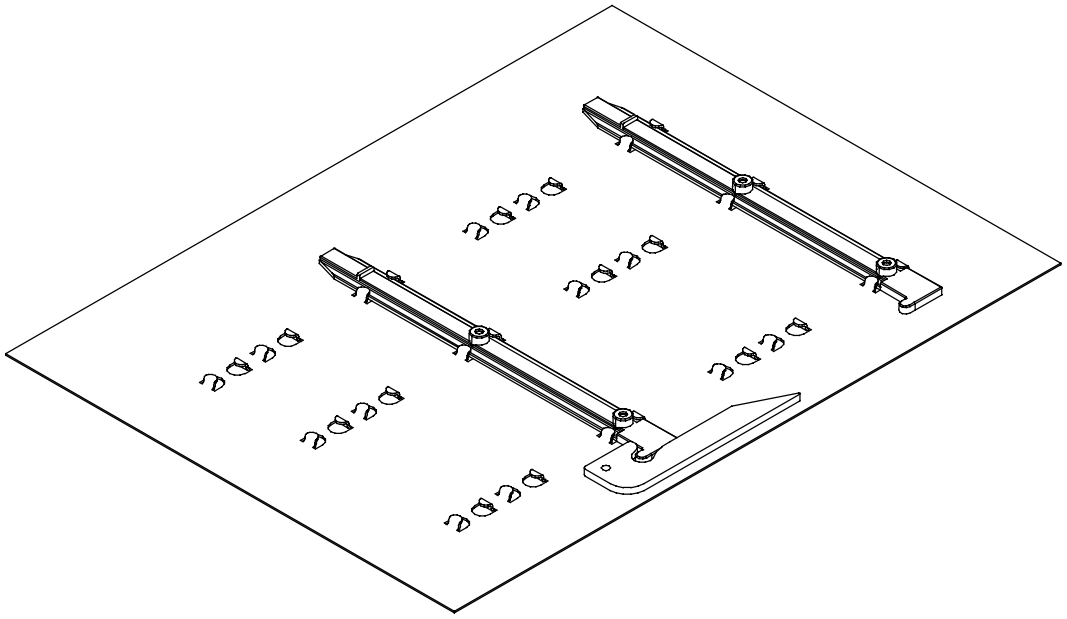

Figure 34. Chassis-to-Rail Mounting Method Example

7.4 Motherboard EMI Clip Example

The EMI clip protrudes through the secondary side of the motherboard and provides an electrical ground contact between the motherboard and chassis. The EMI clip can be either soldered or press-fit to the motherboard. Figure 35 shows examples of EMI clips, and Figure 36 shows an example of an EMI clip footprint for the motherboard attachment. The EMI clip is provided by the motherboard vendor.

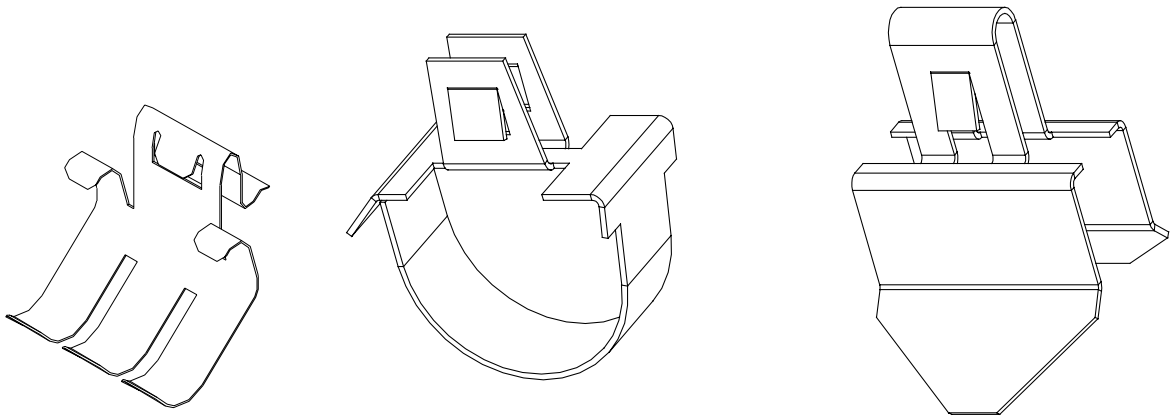

Figure 35. EMI Clip Examples

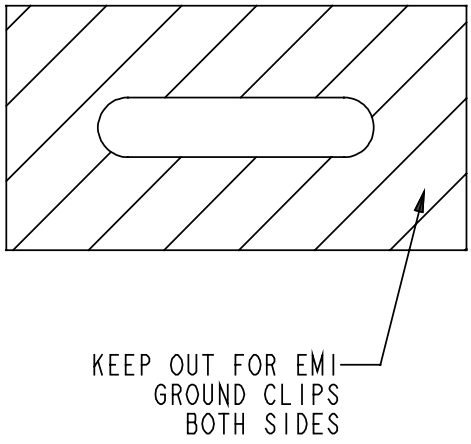

Figure 36. EMI Clip Footprint Example

7.5 Reference Clip Contact Impedance

The reference EMI Clip contact impedance is defined to be the Class R Bond per MIL-B-5087B, which is 2.5 milliohms.

7.6 Back Panel I/O Shield Example

Figure 37 shows an example back panel I/O shield. The motherboard vendor must ensure availability of the I/O shield.

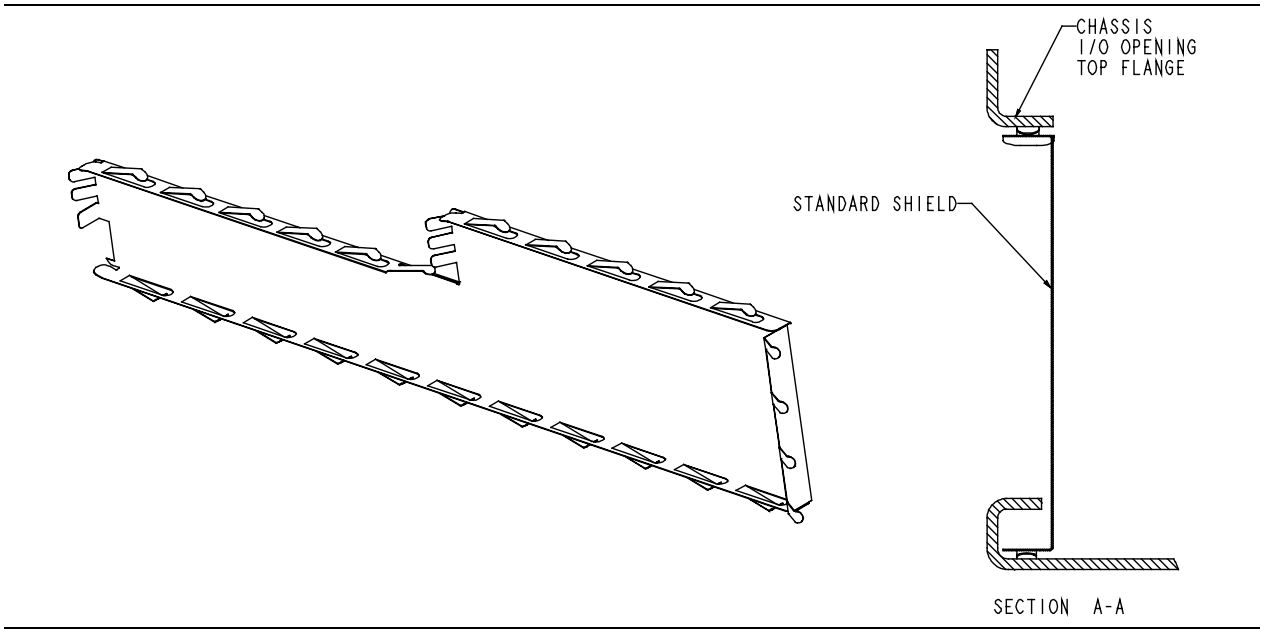

Figure 37. Back Panel I/O Shield Example

7.7 NLX Riser with Supplemental Connector Example

An optional “supplemental connector” is defined for designers who would like to eliminate all possible cables from the motherboard, or who simply need to use some of the less common signals from the motherboard. This supplemental connector is positioned rearward of the NLX riser connector, along the goldfinger edge where the “notch” at the back of the motherboard occurs. Refer to Figure 12, NLX Card Edge Detail, Primary (Top) Side, for the supplemental connector detail.

The optional supplemental connector is a 2x13 pin, 0.1 inches pitch, card edge connector (AMP 145274-1 or equivalent).

The signals are defined in Table 17. The X side is the bottom (secondary) side of the motherboard, and the Y side is the top (primary) side of the motherboard. Pin 1 is toward the back of the motherboard (back panel I/O connectors).

Table 17. Signals, NLX Riser with Supplemental Connector

Pin	Signal Name	Type	I/O *	Description	Signal Type
X1	CD_IN_LT	AUDIO	I	CDROM line in left	Analog 1V RMS
X2	AGND	PWR	NA	Low pass filtered ground for audio circuitry on the riser.	NA
X3	MIC_IN	AUDIO	I	Pre-amplified microphone input. Pre-amp circuitry to reside on riser or in microphone.	Analog 1V RMS
X4	LINE_OUT_LT	AUDIO	O	Analog line out left	Analog 1V RMS
X5	FP_SPKR_EN	AUDIO	I	This signal indicates if headphones have been plugged into the front panel LINE_OUT jack. The signal is connected to one of the wipers on the audio jack and is HIGH when the headphones are plugged into the front audio jack and LOW when they are not. The signal is pulled LOW through a pulldown on the motherboard (typically 100K).	TTL
X6	VOL_DN#	AUDIO	I	Connects to Volume Down switch on front panel, appropriate pullup resistor on motherboard. The motherboard provides debounce protection and a pullup resistor.	TTL
X7	GND	PWR	NA	Ground	NA
X8	SMI#	SYS	I	System Management Interrupt that is an input to the motherboard.	open drain
X9	AC_SD_IN1	AC'97	I	Serial, time division, multiplexed, AC'97 input stream to the motherboard from the codec on the riser (output from codec).	TTL
X10	AC_SD_IN2	AC'97	I	Serial, time division, multiplexed, AC'97 input stream to the motherboard from the codec on the riser (output from codec).	TTL
X11	AC_SD_IN3	AC'97	I	Serial, time division, multiplexed, AC'97 input stream to the motherboard from the codec on the riser (output from codec).	TTL
X12	AGND	PWR	NA	Low pass filtered ground for audio circuitry on the riser	NA
X13	MODEM_MIC	AUDIO	O	Preamplified microphone mono output signal from motherboard to telephony device	Analog 1V RMS

* I/O column: relative to motherboard, "O" = output, from motherboard to riser; "I" = input, from riser to motherboard.

Continued

Table 17 continued: Signals, NLX Riser with Supplemental Connector

Pin	Signal Name	Type	I/O *	Description	Signal Type
Y1	CD_IN_RT	AUDIO	I	CDROM line in right	Analog 1V RMS
Y2	CD_IN_GND	PWR	I	Isolated CDROM Ground.	NA
Y3	AVCC	PWR	O	Clean power from the motherboard to audio circuitry on the NLX riser; could be an isolated power source; 1.5 Ampere max. limitation because of the connector / gold finger limitation.	5-9V DC
Y4	LINE_OUT_RT	AUDIO	O	Analog line out right	Analog 1V RMS
Y5	FP_MIC_EN	AUDIO	I	This signal indicates if a microphone has been plugged into the front panel MIC_IN jack. The signal is connected to a wiper on the MIC_IN jack and is HIGH when the microphone is plugged in and LOW when it is not. The signal is pulled LOW through a pulldown resistor on the motherboard (Typically 100K).	TTL
Y6	VOL_UP#	AUDIO	I	Connects to Volume Up switch on front panel, appropriate pullup resistor on motherboard. The motherboard provides debounce protection and a pull up resistor.	TTL
Y7	AC_RST#	AC'97	O	AC'97 master H/W reset	TTL
Y8	AC_SD_IN0	AC'97	I	Serial, time division, multiplexed, AC'97 input stream to the motherboard from the codec on the riser (output from the codec).	TTL
Y9	GROUND	PWR	NA	Digital (main motherboard) ground plane.	NA
Y10	AC_SD_OUT	AC'97	O	Serial, time division, multiplexed, AC'97 output from the motherboard to the codec on the riser (input to the codec).	TTL
Y11	AC_SYNC	AC'97	O	48KHz fixed rate sample sync signal from the motherboard to the codec on the riser	TTL
Y12	AC_BIT_CLK	AC'97	I	12.288 MHz serial data clock	TTL
Y13	MODEM_SPKR	AUDIO	I	Analog mono input signal to motherboard from telephony device.	Analog 1V RMS

***** I/O column: relative to motherboard, "O" = output, from motherboard to riser; "I" = input, from riser to motherboard.

8. Revision History, Previous

Revision 1.1 to 1.2

- Edits and clarifications:
  Most of the figures have been edited to make the specification easier to understand and to assure consistency between figures. Examples of the changes include consistent usage of decimal places on dimensions and notation for english/metric, and the hatching used to identify gold fingers. Any structural changes are called out specifically in the notes.
- Removed revision history going from revision 0.9 to 1.0.
- Sections 1 and 2: Removed references to the basic riser.
- Section 3.1.4: NLX Board Complete Keepout Specification—Changed "chassis manufacturers" to "system assemblers."
- Section 3.2.1 added: EMI Grounding Using Motherboard Rails.
- Section 3.3: NLX Card Edge Connectors—changes include:
  - Added "front to back" in fourth paragraph.
  - Section 3.3.3 added —NLX Riser Card Considerations.
  - Moved "Riser Mechanical Support" and "Connector and Card Edge Alignment" paragraphs from section 2.1.1 to section 3.3.3.
  - Paragraph added on "Alignment of the 340-pin Connector and the Supplemental Connector."
- Section 3.3.4 added: Reserved Space for Workstation/Server Performance Connector Definition.
- Section 3.7: AGP Support—Changed "NLX-compliant chassis should contain a rubber bumper" to "NLX chassis should enable a rubber bumper."
- Section 3.9.2: Added the following text: "This chassis surface must be ***flat*** over the maximum top flange dimension; outside of this dimension, the chassis designer is free to implement any guide or alignment features desired. To standardize a shield design, the dimensions flagged with an asterisk must be used. Also required is the minimum motherboard location dimension of 7.62mm[.300 inches]. A standard shield must fit between the back of the chassis and the board mounted connectors at the MINIMUM MOTHERBOARD LOCATION. This will limit the standard shield flange length to a maximum of 5.84mm[.230 inches] plus tolerance. Any deviation from the above mentioned dimensions may require the use of a chassis specific shield."
- Section A.5: Motherboard Rails—Mounting the Motherboard to Chassis, changes to paragraphs two and three were made to clarify the spec.
- Figure 3.7.1 added: Ground Pad Detail on Chassis for EMI Clips on Rails.
- Figure 3.7.2 added: Rail Section View of Ground Pad.
- Figure 3.9: NLX Card Edge Detail, Primary (Top) Side—changed board width tolerance to +0.007, -0.005. Dimensioned cutout in front of 340-pin connector. Included 2.00mm reference dimension from gold finger centerline to notch edge.
- Figure 3.10.1 added: Reserved Space for Workstation/Server Performance Connector.

- Figure 3.12: AGP Connector Pin 1 Location—added AGP connector location detail.
- Figure 3.13: NLX Motherboard Primary Side Height Restrictions—changed keepout dimension from 4.700 inches to 4.750 inches. Changed second keepout dimension from 7.8 inches to 7.46 inches. Other figure changes are consistent with general figure changes noted above.
- Figure 3.15: Chassis Back Panel I/O Shield Opening—View changed to be viewed from outside the system.
- Figure 3.16: Side View of Double High I/O Shield Opening Dimensions—Added shield clearance detail, added 1.690 inches dimension for double high opening, added 0.300 inch dimension for motherboard to chassis gap.
- Figure 3.17 added: Side View of Single High I/O Shield Opening Dimensions.
- Figure 3.18 added: Side View of Double Stack I/O Shield Placement.
- Figure A.2: Rail Motherboard View—adjusted to account for EMI clip in rail design.
- Figure A.3: Rail Side View—adjusted to account for EMI clip in rail design. Taper added to the tip of the rail to ease insertion into guides during assembly.
- Figure A.4: Rail Section View—adjusted to account for EMI clip in rail design. Taper added to the tip of the rail to ease insertion into guides during assembly.
- Figure A.5: Latch View—This is an example design. We will be providing a second example in our design guide to enable the latch to "automatically" engage the rail head as the board is inserted. See the NLX web site for details.
- Figure B.5: EMI Clip Examples—added two more examples of EMI clips.
- Figure B7: Back Panel I/O Shield Example—added to figure a cross-section of the shield mounted in the chassis.
- Table 3.1: Clarified descriptions on hole sets B and C.
- Tables 4.5, 4.6, and 4.7: Changed floppy and IDE reserved signals to general reserved pins and adjusted tables accordingly.
- Table 4.8: PCI Segment, Riser Interconnect pinout
  - B8 (SER_IRQ) was termination on the riser, is now terminated on the motherboard
  - B51 (PCI_PM# signal) was terminated on the riser, is now terminated on the motherboard
- Table 4.10: IDE, Floppy, and Front Panel Section, Riser Interconnect Pinout
  - A140 was FLPY_RSVD, is now RESERVED
  - A116 was IDEA_RESRV, is now RESERVED
  - A135 was IDEB_RESRV, is now RESERVED
  - A138 (DRV2# signal) was terminated as GND, is now shown as NA
  - A150 was terminated as NA, is now terminated as MB
  - A151 was terminated as NA, is now terminated as MB, also I/O was changed to O
  - A159 was USB1/3_OC, is now USB1/3_OC#
  - A160 was terminated as NC, now terminated as RIS
  - A161 was terminated as NC, now terminated as RIS
  - A162 was USB2/4_OC, is now USB2/4_OC# , also was terminated as NC, is now terminated as RIS

- A165 was TAMP_DET, is now TAMP_DET#
- A166 was RESERVED, is now MSG_WAIT_LED# and terminated at the riser
- B159 was terminated as NA, is now terminated as RIS
- B160 PWRGOOD signal name changed to PWOK. This makes the signal consistent with the NLX power supply recommendations.
- B164 was ACTIVITY_LED, is now LAN_ACTVY_LED#, also was terminated as NA, is now terminated as RIS
- B161 was SOFT_ON/OFF, is now SOFT_ON/OFF#, also was terminated as NA, is now terminated as MB
- B163 was terminated as NA, is now terminated as MB
- B165 was terminated as NA, is now terminated as MB

- Table 4.11: IDE, Floppy, and Front Panel Signal Descriptions
  - USB descriptions: For pins A159 and A162, changed pullups from motherboard to riser
  - B1 and B3 SCSPKR_RT and SCSPKR_LFT added in the description a note that reads “Note: When mono audio is used, PCSPKR_LFT will function as the mono signal.”
  - B51 changed signal type from PCI TTL to Open Drain
  - B156 FP_SLEEP added to the description to read “The motherboard provides debounce and pulldown resistor.”
  - B157 FP_RST# Signal Type should be “open drain”
  - B159 PWRLED# Definition modified to “A low level will signal the system is in a poweron state, a high level will signal a power-managed state”.
  - B160 PWRGOOD signal name changed to PWOK. This makes the signal consistent with the NLX power supply recommendations.
  - B165 was MDM_WAKE, is now MDM_WAKE#
  - A116, A135, were IDE reserve pins, now general RESERVED pins.
  - A140 were Floppy reserve pins, now general RESERVED pin.
  - A151 changed I/O to O. Description added to reserve EEPROM binary device address 1010000 for future riser configuration initiatives.
  - A165 TAMP_DET# Signal type change, was open drain (VBAT), is now open drain
  - A166 MSG_WAIT_LED signal added. Description enhance to include: “Control signal for telephony device to indicate a message is waiting. A low level will turn the LED on, and a high level will trun the LED. Off. A current limiting series resistor (typ. value 330 ohm) is located on the riser.”
  - A166 taken off the reserved list
- Table B.1: Supplemental connector signals changed. I/O APIC signals removed. Telephony Audio added. Signal Definitions for AC’97 added.
  - Y3 description suggested 2.0amp max, now suggests 1.5amps
  - X6 was VOL_DN, is now VOL_DN#
  - X7 was IRQ0, is now GROUND, and description changed to ground

- X8 was IRQ1, is now SMI# with open drain signal type
- X9 was IRQ8, is now RESERVED
- X10 was AP_ACK1#, is now RESERVED
- X11 was GROUND, is now RESERVED
- X12 was AP_ACK2#, is now AGND
- X13 was AP_CS#, is now MODEM_MIC
- Y6 was VOL_UP, is now VOL_UP#
- Y12 (AC_BIT_CLK) signal type changed from Output to input
- Y13 was AP_REQ#, is now MODEM_SPKR

Revision 1.0a to 1.1

- Figure 3.7: Updated riser primary surface dimension to include metric equivalent, and put brackets around the .260 dimension.
- Figure 3.8: Changed the length dimension of the first segment of the 340 -pin card edge from 77mm to 77.5mm. Two associated dimensions changed also: 45.19mm was changed to 44.68mm, and 7.09mm was changed to 6.58mm. Labeled the number of gold fingers on each section of the card edge connector for the 340-pin connector. Corrected a visual inaccuracy on the last segment of the pins shown on the 340-pin card edge gold finger (closer to the front of the board). These pins "appeared" longer than the other segments; no dimensions were affected. Included "Primary" in the figure name.
- Figure 3.9: Changed dimension on the narrow end of the gold finger "paddle" from .6mm from .41mm (This change should enable more easily manufactured pcb boards. Removed unnecessary 11.68mm dimension in the upper right of the figure. Removed unnecessary character that existed after the word "side" in lower figure. Removed "Bottom Side" from the figure name.
- Figure 3.10: Changed the 146.35mm dimension to 146.29mm. Corrected a visual inaccuracy on the last segment of the pins shown on the 340-pin card edge gold finger (closer to the front of the board). These pins "appeared" longer than the other segments; no dimensions were affected. Changed pin label from "1B" to "B1". Changed 70.8 dimension to 70.79.
- Figure B.6: Removed the dimensions from the EMI clip detail drawing.
- Figures B.8 and B.9: Removed AGP card mechanical drawings. The AGP specification team will be modifying the AGP NLX bracket that is used for the AGP card. The modified design will enable a more user-friendly installation. The mechanical design will be available on a separate document on the NLX spec site and on the AGP spec site on the World Wide Web.
- Table 4.10: pin B161 changed from SOFT_ON/OFF to SOFT_ON/OFF#
- Section 2.1.1: Added the following statement: "Connector and Card Edge Alignment: The System designer should ensure that there exists enough clearance in the system rails so the motherboard can align properly with the connector. Too much tilt or lack of alignment will prevent board insertion and seating."
- Section 3.3: Added the following statement, "The seating depth of a NLX motherboard into the NLX card edge connector is defined to be the distance from the riser board

primary surface to the edge of the NLX motherboard when fully inserted into the connector. This distance is .260. Also, the minimum contact backout wipe within the connector for the upper and lower contacts on the gold finger pads shown in Figure 3.9 is 0.99 mm (.039 inches).

- Section 3.3: Added the following statement, “The total available mechanical lead-in for both the connector and the card edge is 5.38mm [.211inches]. If the motherboard is off-center from the connector by more than 2.69mm [.106], a mechanical interference will occur.”
- Section 3.3: Added 340-pin connector part number: AMP # 145275-1.
- Section 3.7: Removed the statement, “Appendix B.8 (AGP Add-in Card Chassis Support Example) defines an example of the chassis implications of the AGP slot on the motherboard and the size and location of an opening in the back of the NLX chassis”.
- Section 4.1: Changed MDM_WAKE to MDM_WAKE#.
- Section 4.1: Changed TAMP_DET to TAMP_DET#. This eliminates a constant drain on VBAT. Also changed the description wording FROM: “This signal is low when the “switch” is open and is high when the “switch” is closed. This signal is pulled high to VBAT on the motherboard via a 1 Kohm resistor”, and is CHANGED TO: “This signal is *low* when the "chassis lid" is open indicating an intrusion. The signal should be *open* when the "chassis lid" is closed indicating normal operation. Debounce and associated circuitry uses battery voltage and is located on the motherboard.” Also, TAMP_DET signal type was changed from TTL (VBAT), to Open drain (VBAT).
- Section 4.1: Added location of signal termination for all 340 card edge connections in Tables 4.8, 4.9, 4.10.
- Section 4.1: Changed FP_SLEEP# to FP_SLEEP (from active low to active high).
- Section 4.1: FAN_CTL signal type changed from output instead of an input. Also the description was changed FROM: “This signal sets the fans to maximum speed when the voltage potential on this pin is near ground (0 volts), whereby this pin sinks a total maximum of 1 ampere. This signal sets the fans to minimum speed (off) when this signal floats, whereby this pin sinks no current. Fan speeds in between can be achieved by setting the voltage potential of this pin between 0 and +12 volts (say +6 volts), or limiting the current sink of this pin. TO: “This signal sets the fans to maximum speed when the voltage potential on this pin is 10.5 volts or greater. This signal sets the fans to minimum speed (off) when this signal is 1 volt or less. Fan speeds in between can be achieved by setting the voltage potential of this pin between 1 and +10.5 volts. The maximum current supplied by this pin is 50mA and is not meant to drive fans directly. Internal power supply fan driving circuitry has been allotted 20mA of the available 50mA from this signal. Remaining 30mA may be used for circuitry on riser or motherboard to drive other fans in the system.”
- Section 4.1: Changed PCI_PM signal to PCI_PM#. Also, the pull up resistor was defined as on the riser.
- Section A.6: Added NLX Motherboard Insertion and Extraction statement: "It is recommended that NLX chassis designers include a visual alignment marking, such as an arrow or stamped line, on the base of the chassis such that it will align with the

'connector key datum' on the motherboard in its proper insertion location. Refer to the NLX Card Edge Board view, Figure 3.10. Motherboard designers may want to put a mark next to the 'connector key datum,' on the motherboard to facilitate the users alignment during insertion. This will help the installer guide the rails into the chassis mounts."

Revision 1.0 to 1.0a

- Section 3.3: Replaced Figure 3.10 with clarified drawing of NLX connector.
- Section B.2: Figures B.2 and B.3, adjusted shaded areas of keepout zones to match outline of riser card. Renamed keepout zones on recommended riser layout. Relaxed recommended keepout restrictions. Also reworded the keepout area explanations.

Revision 1.8, Figure and Table Number Updates

Table 18. Figure Number Updates

Now (in Version 1.8)	In earlier versions	Now (in Version 1.8)	In earlier versions
1	2.1	20	3.16
2	2.2	21	3.17
3	3.2	22	3.18
4	3.3	23	3.19
5	3.4	24	3.20
6	3.5	25 (new)	—
7	3.6	26	A.1
8	3.7	27	A.2
9	3.8	28	A.3
10	3.7.1	29	A.4
11	3.7.2	30	A.5
12	3.9	31	B.1
13	3.10	32	B.2
14	3.11	33	B.3
15 (new)	—	34	B.4
16	3.12.1	35	B.5
17	3.13	36	B.6
18	3.14	37	B.7
19	3.15		

Table 19. Table Number Updates

Now (in Version 1.8)	In earlier versions
1	not numbered
2	3.1
3	4.1
4	4.2
5	4.3
6	4.4
7	4.5
8	4.6
9	4.7
10	4.8
11	4.9
12	4.10
13	4.11
14	A.1
15	A.2
16	A.3
17	B.1
18	new
19	new