AMD

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HDT6 Overview

December 2004

Who Am I:

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Name: David “T” hanairongroj

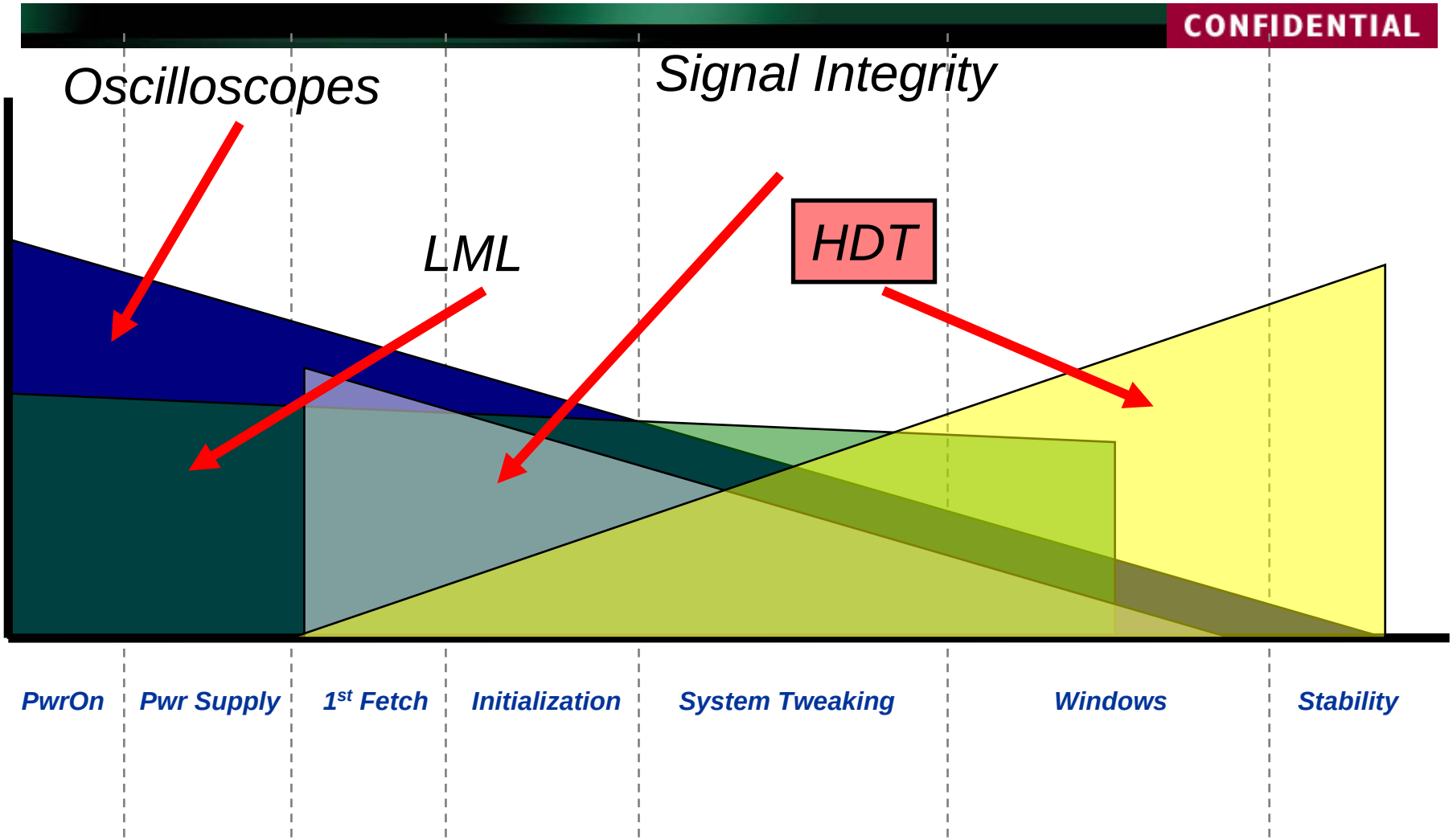
Group: Global Services

Background:

- Worked in SRD developing Windows application drivers for 5+ years

- Recently moved to new group and beginning to embark into world of BIOS and assisting customers with system software questions.

Board Development Timeline



Agenda

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- Introduction to HDT
- Hardware Requirements
- HDT Protocol / Internals
- Exploring the Work Area
- HDT Features
- Practical HDT Scenarios / Examples
- Q&A

Introduction: HDT Software History

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- HDT – **AMD Hardware Debug Tool**
- HDT 2
  - A dialog based Windows application
  - Target AMD's 6th and 7th generation processors using Telepath
- HDT 3
  - An MDI based Windows application
  - Targets 7th generation uni-processor (UP) using Raven only
- HDT 4/5 (5 for rev E processors only)
  - An MDI based Windows application
  - Target 7th generation UP and 8th generation multi-processor (MP) using Raven/HDT MP Adapter (Sprocket)
  - First released Jan 2002 to support 8th generation processor bring-up
- HDT 6
  - A Microsoft .NET framework based Windows application
  - Targets 7th generation UP thru 8th generation multiple node and core platform
  - Released Nov 2004 under NDA to support multi-core bring-up

Introduction: What HDT is?

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- HDT is AMD's Hardware Debug Tool.
- HDT supports both single and multiple processors (also supports dual core processors)
- HDT allows a user to access and debug the internal state of the AMD Opteron™, AMD Athlon™ 64, AMD Athlon and AMD Sempron™ processors.
  - Knowledge of the AMD Athlon & Opteron™ processor micro architecture and the *AMD's BIOS and Kernel Developers Guide* are essential.
- The HDT tool is used to examine processor registers, memory, cache contents, with additional features to set breakpoints, disassemble code, etc..
- Communication based on the JTAG standard / IEEE 1149.1
- In addition to the standard JTAG commands HDT incorporates a number of proprietary commands.

Introduction: What HDT is NOT

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- HDT CANNOT debug a dead processor
  - System must have clocks and begin some type of code execution
  - HDT microcode must work
- HDT is NOT a logic analyzer, especially for the lower subsystem buses
- HDT is NOT a kernel debugger
  - HDT is a target – host debugger. It debugs target images at host. The target state halts when entering HDT mode
  - Cannot load symbols or view source code (e.g. windbg) yet
- HDT is NOT a performance analyzer tool
- HDT is NOT psychic
  - The user must know what state the processor is in and is responsible for all actions

Introduction: Who Uses HDT?

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- AMD Internal Users
  - Hardware Debug Engineers: platform debug team
  - BIOS Engineers
  - System characterization
  - Software Developers: Diagnostics, Special Tools, Drivers (SRD)
- External Users
  - BIOS/Chipset vendors (desktop, mobile, server, supercomputer, etc.)
  - System ODM and OEM
  - Kernel/OS developers (Microsoft, Suse, etc.)
  - NDA agreement is required to use AMD HDT

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HW Requirements: System Setup

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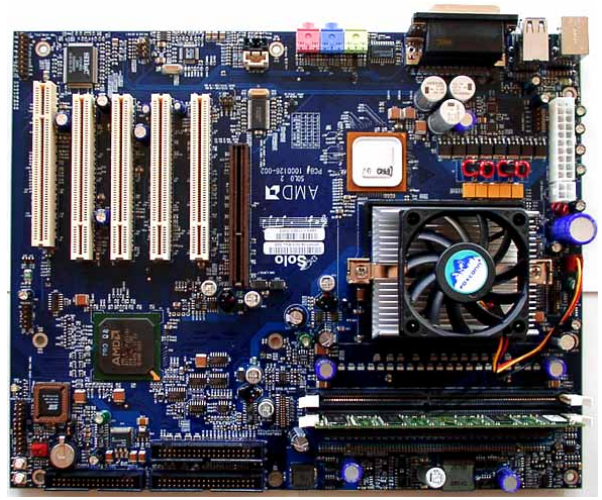
Host System
(HDT Software)

HDT Hardware
Adapter (Raven) –
JTAG Emulator

Target System -
(TAP interface to
JTAG Engine)



HW Requirements: System Setup

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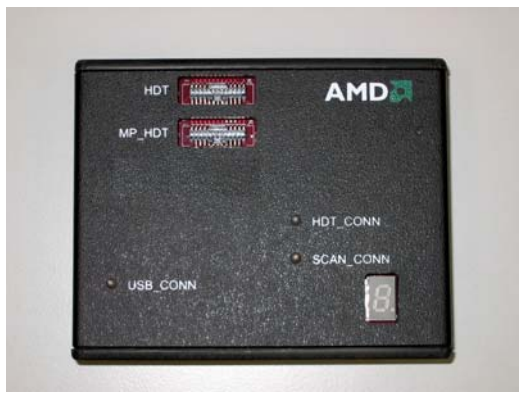
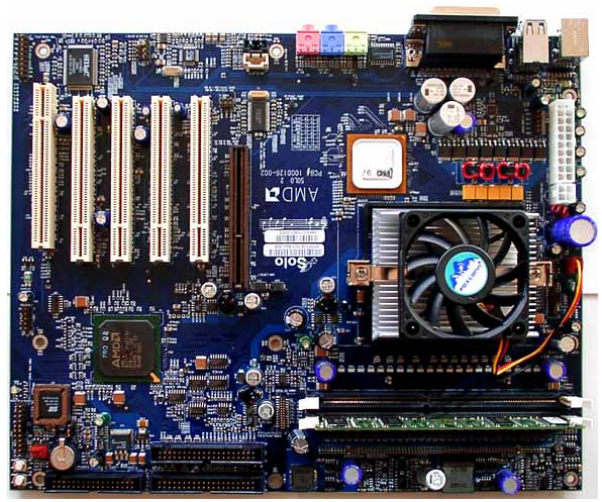
Host System
(HDT Software)

HDT Hardware
Adapter (Possum) –
JTAG Emulator



Target System -
(TAP interface to
JTAG Engine)



HW Requirements: Host System

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- Operating System
  - Microsoft® Windows® 2000 with SP2 or Windows XP Professional, and Microsoft .NET framework
- Memory
  - 256 Mbytes or greater
- Disk Space
  - 100 Mbytes free space for installation. Additional space is used during operations for features that collect large amounts of data.
- Ports
  - If using a Macraigor Raven, setup parallel port to be Enhanced Parallel Port (EPP). No other devices can be used on the parallel port when using HDT.
  - If using a USB HDT Adapter, use a USB 1.1 or USB 2.0 (recommended) port.
- Graphics/Monitor
  - 1024 x 768 true color at a minimum

HW Requirements: Target System

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- Processor
  - Any AMD Opteron™, AMD Athlon™ 64, AMD Athlon™, or AMD Sempron™ processors.
- TAP Connector
  - HDT Header
- Percussion Card
  - Required if target system is based on the Melody platform

HW Requirements: Adapters

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- Uni-Processor Test System
  - Macraigor Raven
  - AMD USB HDT Adapter
    - The adapter is used for AMD Opteron™ and AMD Athlon™ 64 processors ONLY and will not work for previous generations (e.g. AMD Athlon, AMD Duron™, etc.)
    - HDT version 6 or greater is required to use the USB HDT Adapter
    - USB 2.0 is recommended, but USB 1.1 will work at very low speeds.
- Multi-Processor Test System
  - Macraigor Raven & AMD MP Hardware Adapter (Sprocket)
  - AMD USB HDT Adapter

HW Requirements: User Knowledge

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- **Knowledge of:**
  - **AMD64 Technology**
  - **Eight Generation Architecture, BIOS, MSRs, etc.**
  - **HyperTransport™ Technology**
  - **Test Access Port (TAP) & JTAG (IEEE 1149.1) standards**
    - **NOT required**
    - **However, it will provide the user with behind the scenes insight into how the HDT software accomplishes feature tasks**

HW Requirements: HDT Kit

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AMD HDT Uni-Processor Adapter Kit

AMD
www.amd.com

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HW Requirements: HDT Kit

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HW Requirements: HDT Kit

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HW Requirements: HDT USB Adapter Kit (Possum)

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HW Requirements: HDT USB Adapter

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HW Requirements: Debug Header Overview

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- The HDT header enables the “Hardware Debug Tool” to be connected to the processor.
- The HDT header is a 26 pin surface mount connector (versus the 16 pin through hole header found on 7th Generation family motherboards.)
- All 8th Generation motherboard designs are required to provide the site for the connector, especially for **a multi-processor motherboard**.
- The HDT connector is populated only for a system for which HDT will be used. (The surface mount part has a minimal impact on landscape usage.)
- All signals are low frequency; however, it is recommended that the placement be kept to within 3 inches of the processor and routed to shortest length.

HW Requirements: Debug Headers on Serenade (*HDT and MP HDT Headers*)

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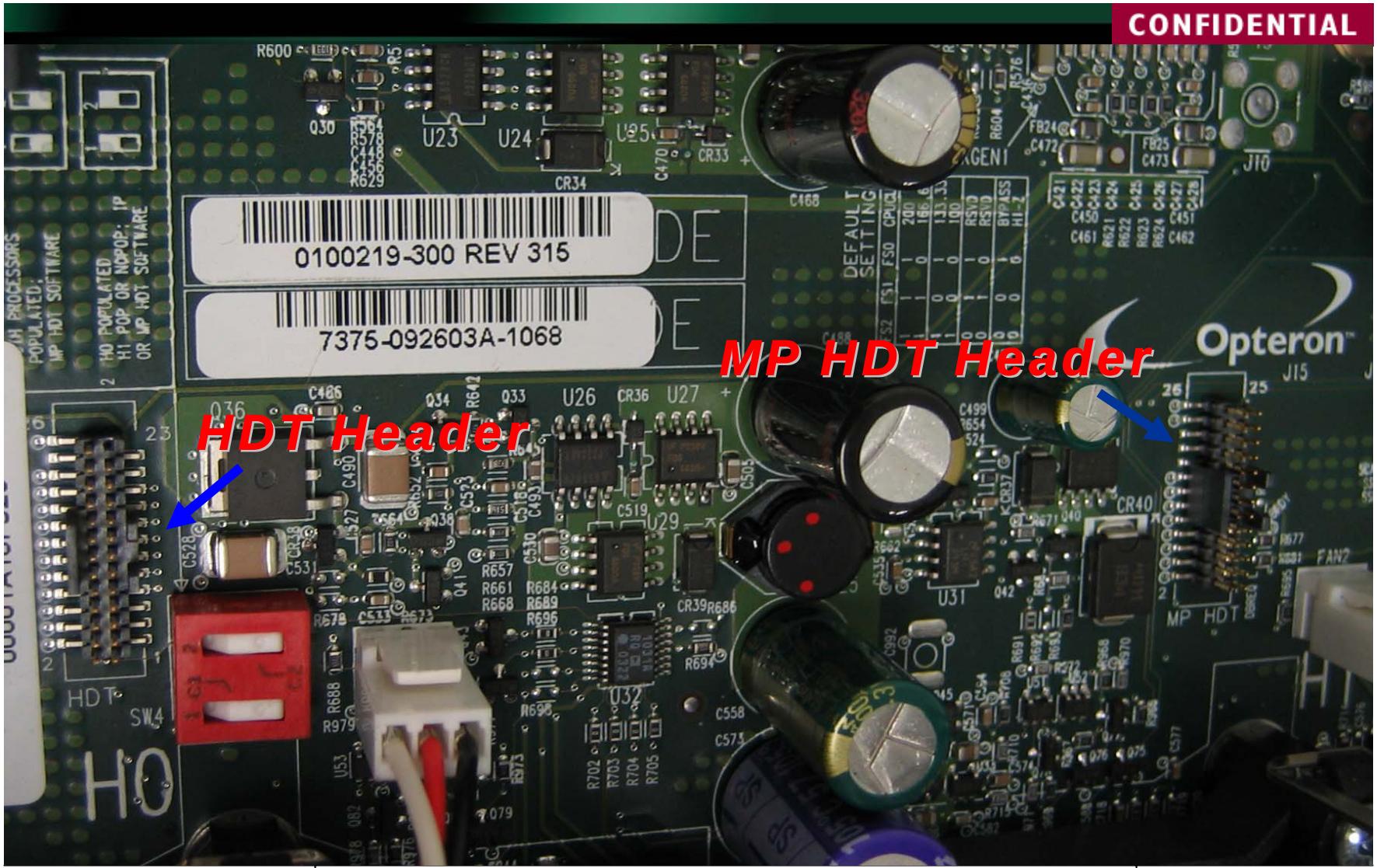

HW Requirements: Debug Headers on AMD USB HDT Adapter (Possum)

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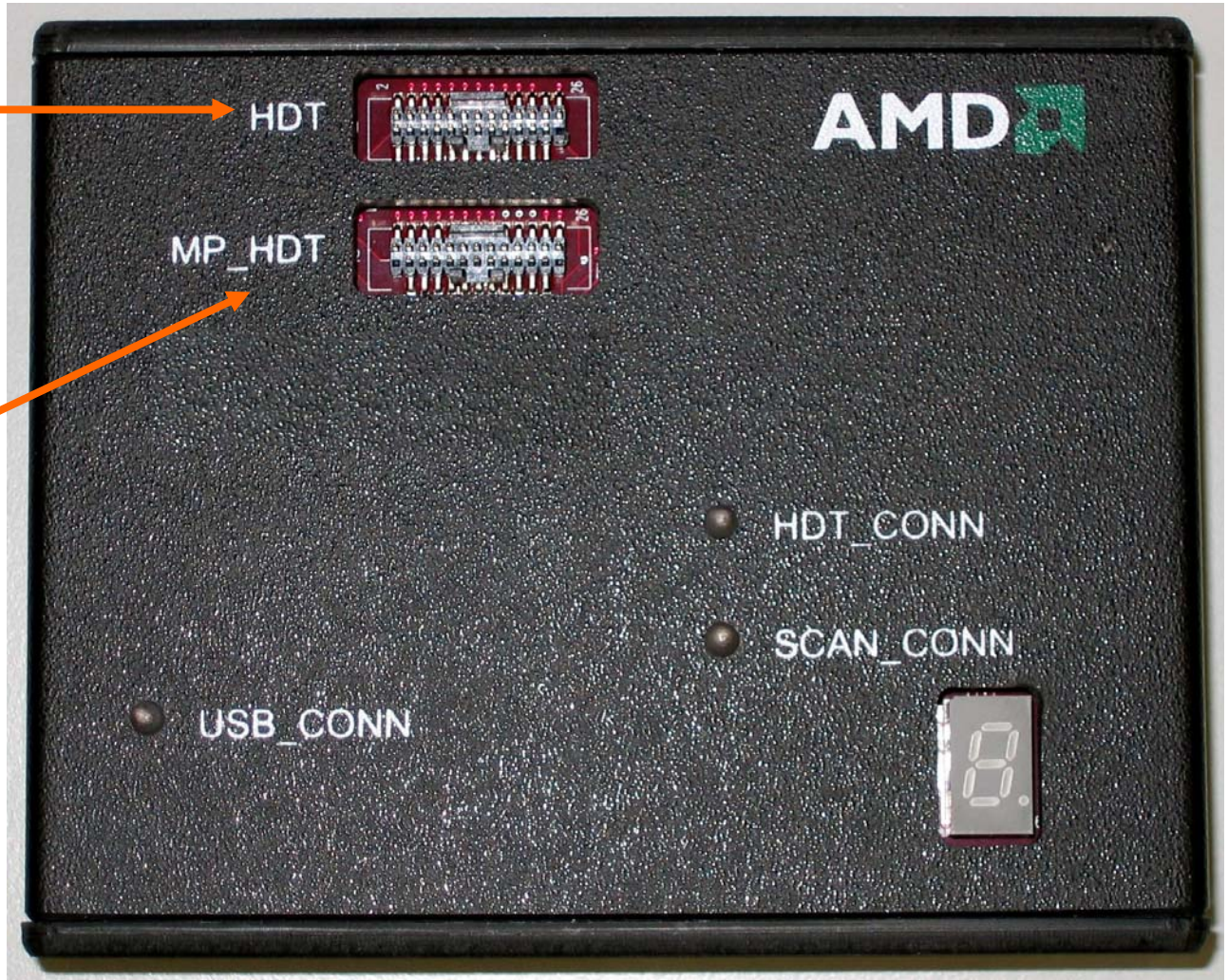
Connect this port to PCB HDT header

Connect this port to PCB MP HDT header only if debugging a MP target



HW Requirements: Target System HDT Header - Mechanical

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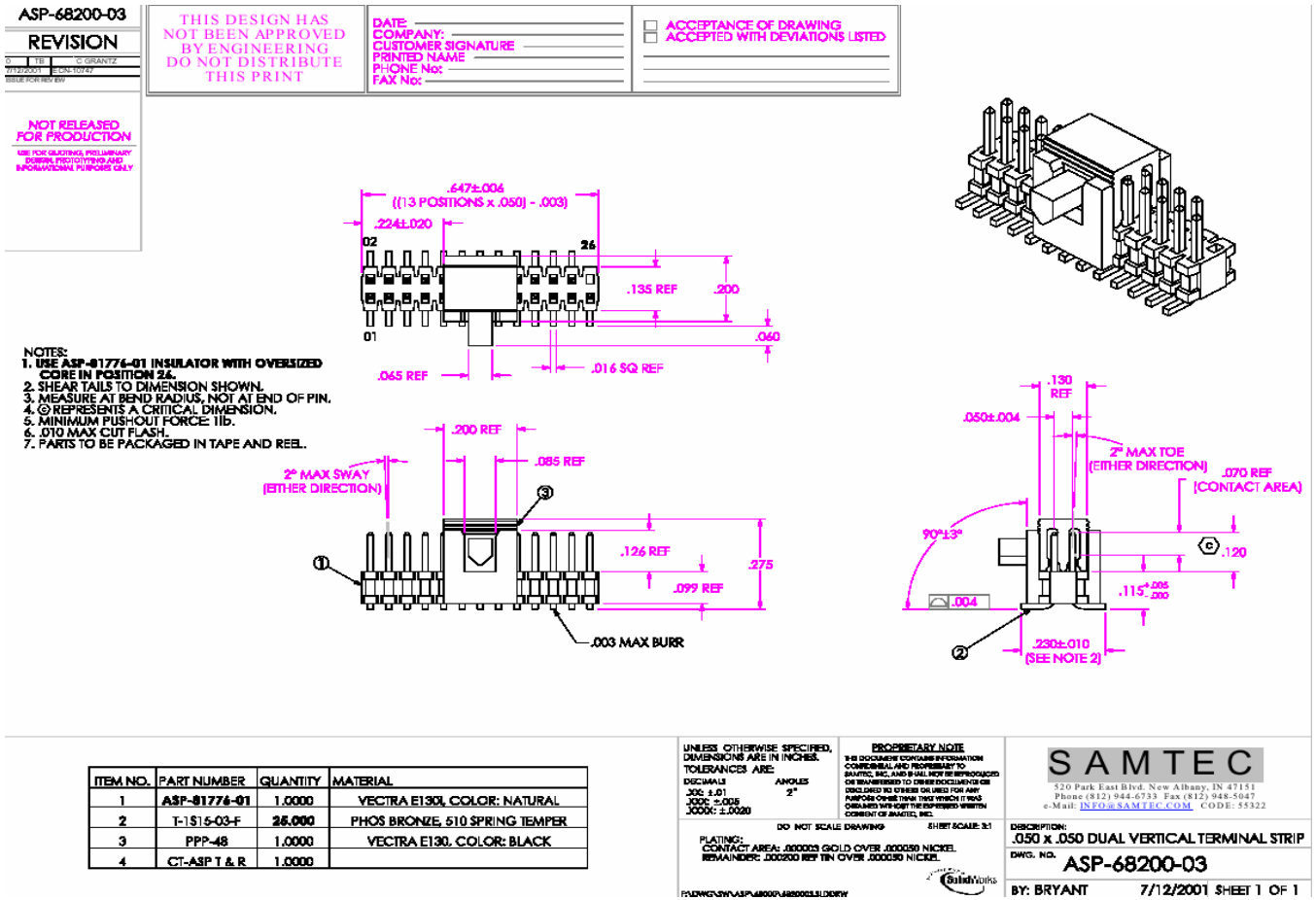
- Samtec 6820007

Samtec 6820008



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HDT Protocol/Internals

- AMD HDT Mode Is:

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- A special debug operating mode that is powered by the AMD microcode JTAG engine (through TAP)
  - Test Access Port (TAP) is a part of processor access pins, which is designed for HDT communication
  - TAP provides a back door access directly to processor core. The internal info of system can be accessed without other component involved
- Under HDT Mode:

1. **Target processor halts to stop all instructions, stack, and registers except for JTAG engine and Time Stamp Counter**
2. **Target can then be driven and/or overwritten by HDT software on host system via JTAG engine.**

How to Set Target in HDT Mode

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- How To Set Processor In HDT Mode.

  1) DBReq: Debug Mode Request
     - A DBReq pin on the processor. Assert it (logical high) to TRY and set in HDT Mode
     - Deassert DBReq to resume DBReq state for next request

  2) Redirection: Redirect #DB Exception to HDT Mode
     - HDT_CFG.Redir can set target to HDT mode if #DB occurs (e.g. hitting a breakpoint)

- How To Know If In HDT Mode.

  – **DBRdy**: Debug Mode Ready State
     - DBRdy pin on processor indicates whether target is in HDT Mode.
     - DBRdy differs from DBReq. DBReq does not have to result in DBRdy
     - HDT functions can only work if and only if DBRdy is HIGH

Enter HDT via DBReq Assertion

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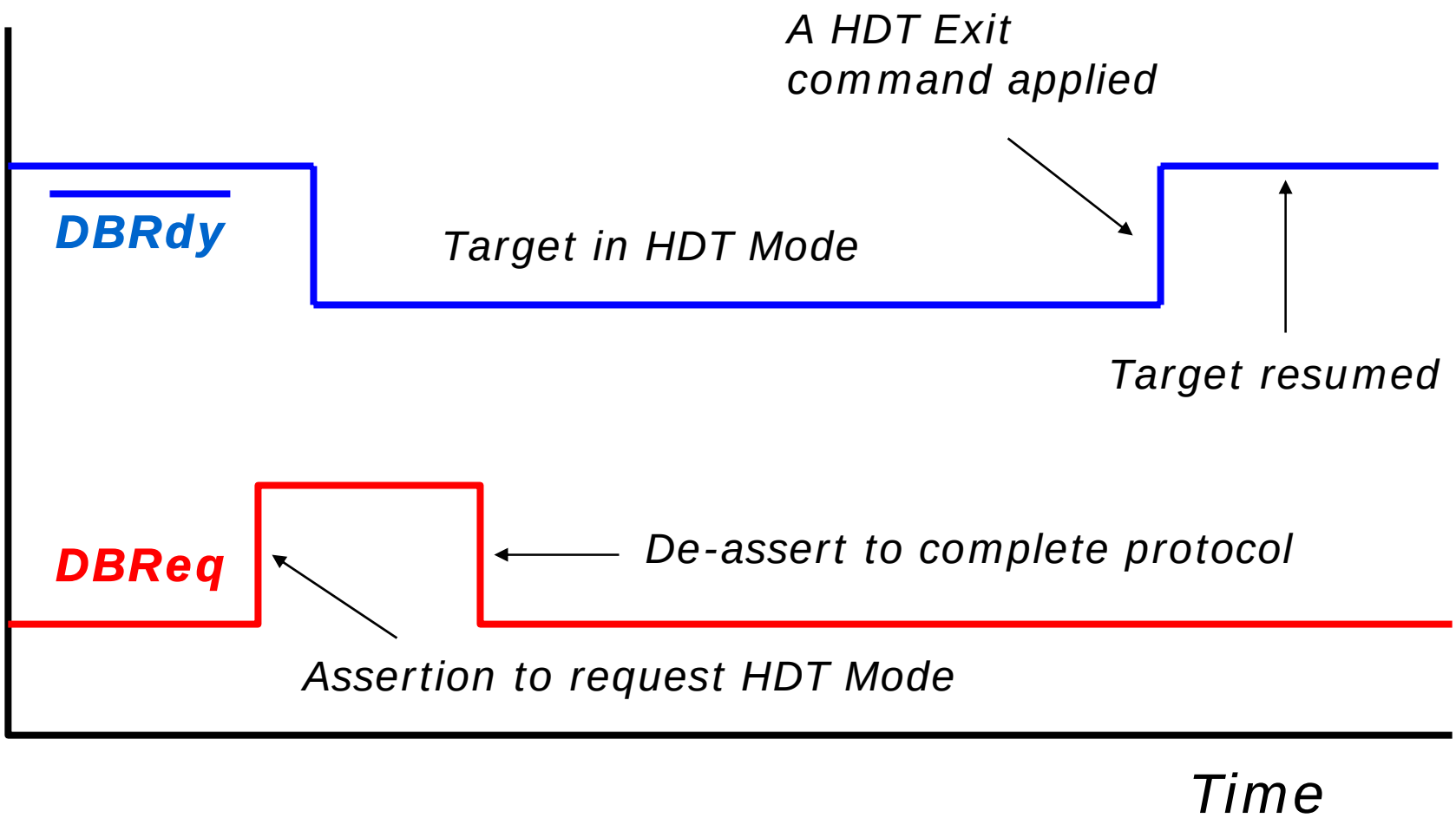

Enter HDT via Redirecting #DB

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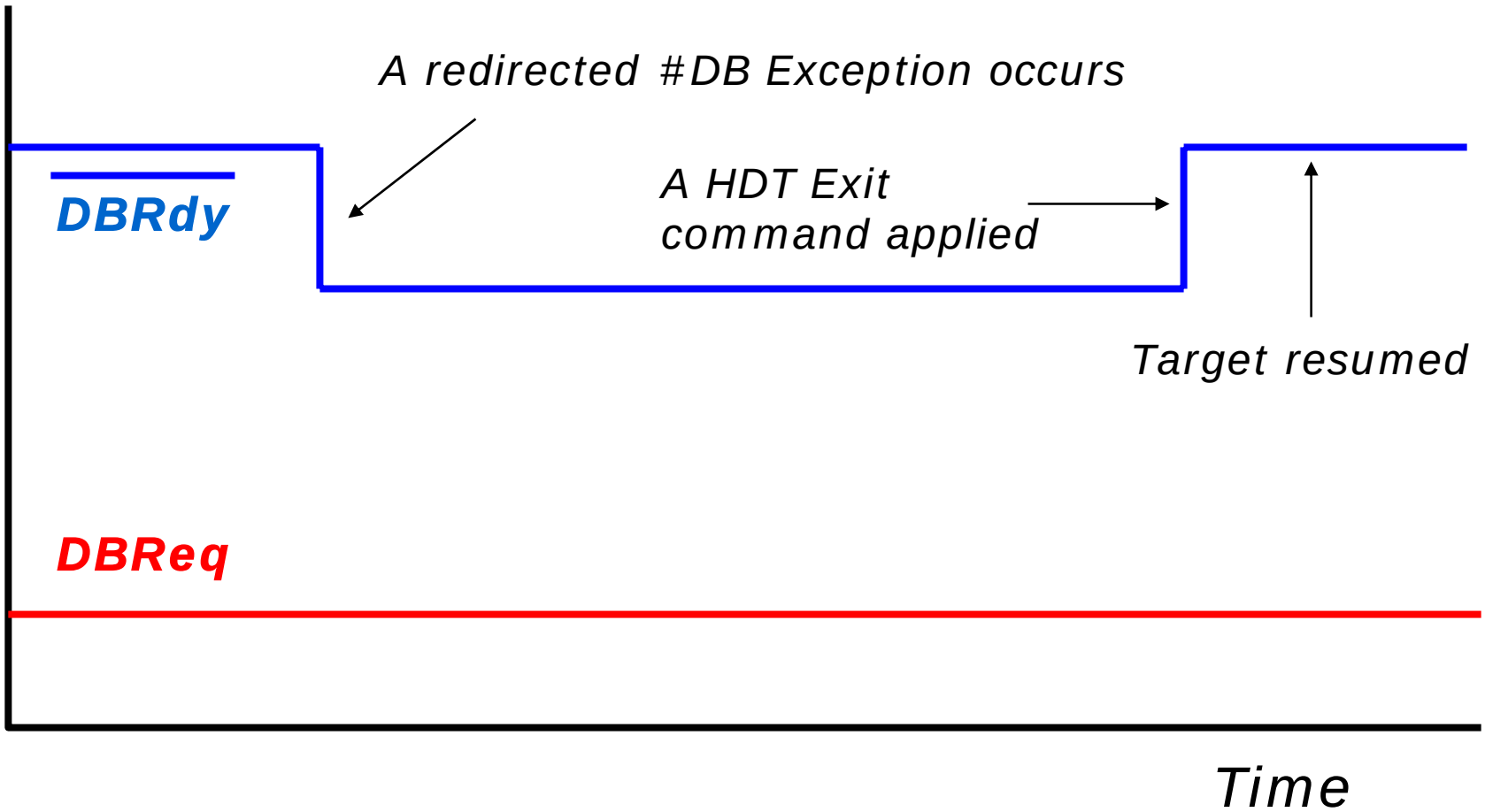

AMD Hardware Debug Tool (AMD Internal Only)

File Edit View Features HDT Windows Help

Enter HDT debug mode

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Te
- I/O Ports
- Instruction Cache Arr
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1	0	Legacy 32-bit Mode	BSP	DBReq	1024

Refresh

Auto Refresh

Press "HDT On" to request to get into HDT Mode

start AMD Hardware Debu... 12:50 PM

HDT in 8th Generation BIOS Boot-up

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- Stackless Initialization – HDT is most efficient tool to debug the process
  - HyperTransport™ Initialization
    - Initialize routing tables for HT links – coherent and non-coherent (HyperTransport™ Trace)
    - Initialize APIC (APIC features)
  - Cache Initialization (Cache Array features)
  - Processor Register default value loading (Processor Registers, such as CPU, MSR registers, etc)
    - Pre-initialize CPU/Chipset to get chipset basic functions
- Initialization of DRAM controller
  - Set MTRR, etc (Processor Register features, Memory Dump, Disassembly, etc)
  - Shadow BIOS code into DRAM
    - Copy BIOS code into target DRAM and set the buffer readonly (Memory type, MTRR registers, Memory Dump, Disassembly, etc)

HDT in 8th Generation BIOS Boot-up (cont)

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- Initialization of ACPI (SMM functions TBD)
- APIC Setup
  - Set MP tables (APIC and PCI features)
- PCI Emulates PCI devices and allocate resources
  - Initialize boot devices (PCI features, IO Access, Breakpoint, Disassembly, etc)
    - Video device is a must
    - Drives – Floppy, CD ROM, HD, etc
- Keyboard initialization
- Setup MP tables
- Memory test
- CPU speed setup
- BIOS Setup page
- Search boot device
- Load 1st 512 bytes to setup MP table, ACPI, etc in right locations where Kernel can use them

HDT Commands:

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- HDT Commands are a special set of JTAG instructions
  - Resume target program
  - Single Step target program
  - Access IO port
  - Access target GPR
  - Access target MSR
  - Access target memory

  DBReq and DBRdy are NOT HDT commands (actual signals to/from processor).

- See Section 12.2.5 of *BIOS and Kernel Developer's Guide for the AMD Athlon™ 64 and AMD Opteron™ Processors (Pub 26094 Rev. 3.23)* for HDT command details

How HDT works for MP

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- A daisy chain technique used to connect multiple processors on target
  - Each processor employs a AMD HyperTransport™ node. In HDT 6, the terminology “node” is used to refer to processor (socket)
  - A JTAG scan in/out can be daisy-chained. Each JTAG instruction length can be multiplied by the number of processors. MP will execute the instruction simultaneously.
  - A special device, Sprocket, has been used in HDT MP Adapter and HDT USB Adapter to perform 8th generation MP access for HDT.

- However, DBReq/DBRdy can not be daisy-chained because they are not HDT commands (actual signals to/from processor)

How HDT works for MP (cont.)

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- What Sprocket does
  - The Sprocket logic has been included in AMD USB HDT connector. The HDT MP adapter performs Sprocket function when using Raven as connector.
  - Allows connections from Sprocket to the target system to be accomplished with inexpensive IDC ribbon cables:
    - one target-side header for connection to a standard 8th generation HDT header (HDT commands sent).
    - one target-side header for connection to the additional DBREQ/DBRDY pairs of a MP system.
  - Provides the ability to arbitrarily execute HDT commands on any one of the daisy-chained processors. Able to set other processors in bypass state.
  - Provides a means of asserting the DBREQ and reading the DBRDY pins of any of up to eight processors.
  - Allow HDT software to detect the number of CPUs in the JTAG chain.
  - Detect redirected #DB assertion from one of MP processors, and set DBReg assert to all processors.
  - Detect target reset occurrence (**only if Possum is used**).

How HDT works for MP (cont.)

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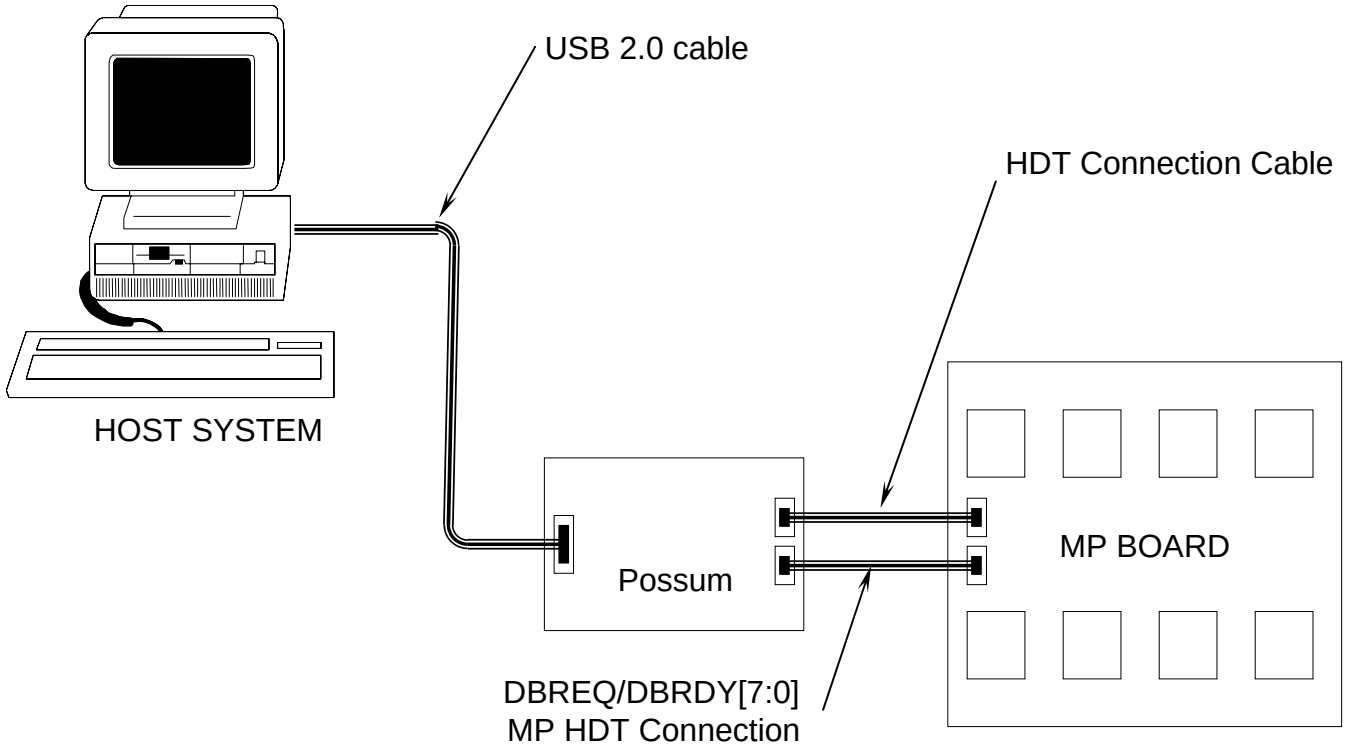
- Use “HDT USB Adapter”, which is coded as “Possum”. It supports up to 8 processors.



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Exploring the HDT Work Area

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Topics:

1. Verifying Connectivity
2. The HDT Layout
3. HDT Toolbars
4. Working With Panels

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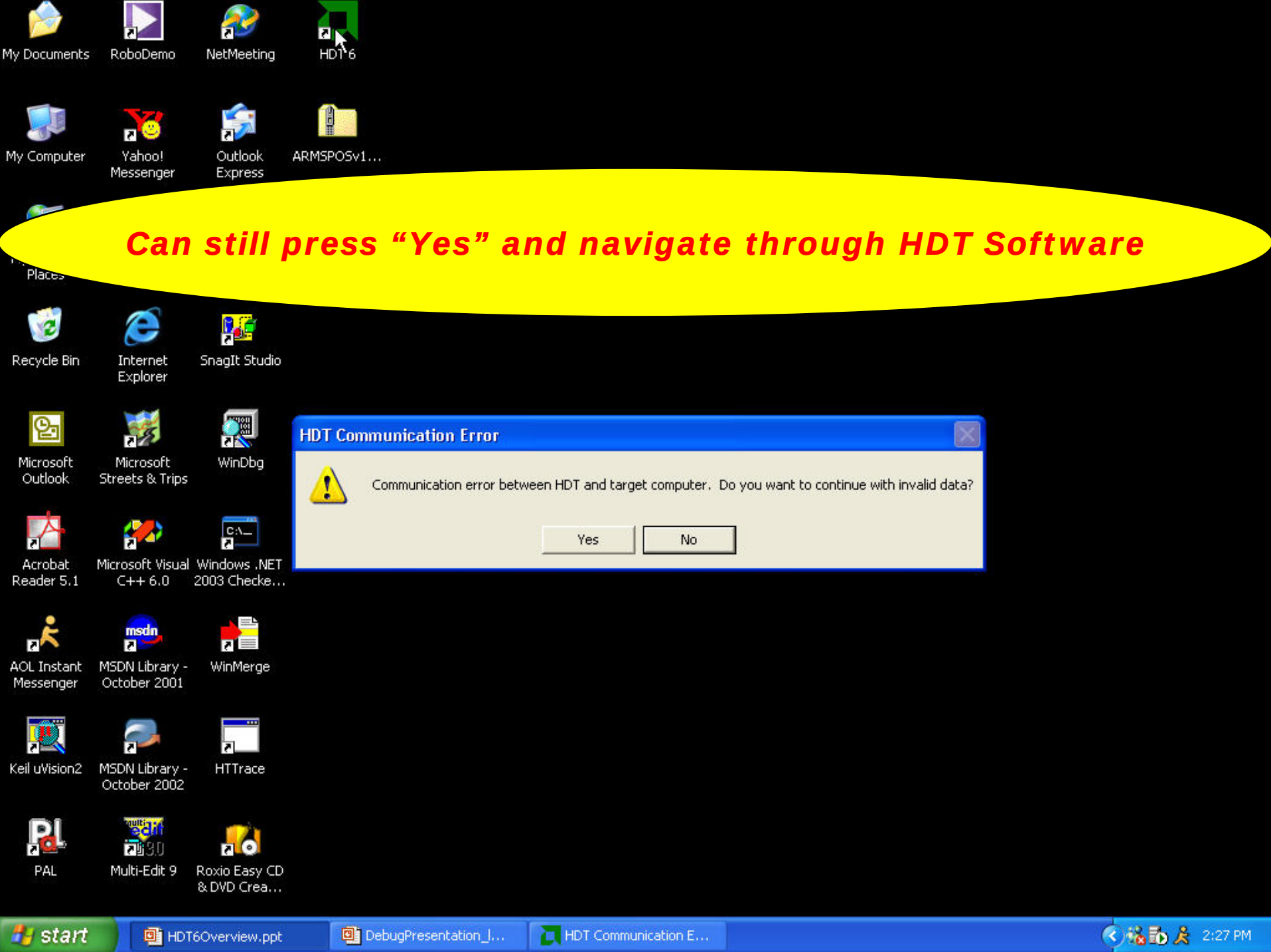
1) Verifying Connectivity

Can still press "Yes" and navigate through HDT Software



AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
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- Debug Utilities
- Download Tools
- HyperTransport™ Te
- I/O Ports
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- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers
  - CPU Registers
  - Debug Registers
  - FPU Registers
  - Last Branch Reg
  - MCA Registers
  - Model Specific R
  - MTRR Registers
  - Performance Reg
  - Program Register
  - Segment Registe
  - Single MSR
  - SSE Registers
  - TR & SMM Regis

Status Info

Node	CPU Name	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_A0/1-sh-claw-754	0	1	1	Invalid Operating Mode	BSP	B0	576

Refresh

Auto Refresh

CPU Registers 1

Name	Value
rAX	FFFFFFFFFFFFFFFF
rBX	FFFFFFFFFFFFFFFF
rCX	FFFFFFFFFFFFFFFF
rDX	FFFFFFFFFFFFFFFF
rSP	FFFFFFFFFFFFFFFF
rBP	FFFFFFFFFFFFFFFF
rSI	FFFFFFFFFFFFFFFF
rDI	FFFFFFFFFFFFFFFF
rFLAG	FFFFFFFFFFFFFFFF
rIP	FFFFFFFFFFFFFFFF
CR0	FFFFFFFF
CR2	FFFFFFFEFFFFFFFF
CR3	FFFFFFFFFFFFFFFF
CR4	FFFFFFFF
CR8	FFFFFFFF
R8	FFFFFFFFFFFFFFFF
R9	FFFFFFFFFFFFFFFF
R10	FFFFFFFFFFFFFFFF
R11	FFFFFFFFFFFFFFFF
R12	FFFFFFFFFFFFFFFF
R13	FFFFFFFFFFFFFFFF
R14	FFFFFFFFFFFFFFFF
R15	FFFFFFFFFFFFFFFF

If NOT in "HDT Mode", press "Refresh" and user will see INVALID data

Node 0 | Core 0 | Refresh | Wr Chgs | Wr All

start | HDT6Overview.ppt | DebugPresentation_I... | AMD Hardware Debu... | 2:28 PM

AMD Hardware Debug Tool (AMD Confidential)

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  - Segment Registe
  - SEM Registers
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  - SSE Registers
  - TR & SMM Regis

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1					

Refresh

Auto Refresh

CPU Registers 1

Name	Value
rAX	00000000FFDFFC50
rBX	00000000FFDFF000
rCX	000000000001E66C
rDX	00000000F3E93102
rSP	0000000080539544
rBP	0000000080539550
rSI	0000000080541DA0
rDI	0000000080542000
rFLAG	0000000000000213
rIP	00000000806B2FAA
CR0	8001003B
CR2	00000000BF8B08CF
CR3	0000000000039000
CR4	000006D9
CR8	00000000
R8	0000000000000000
R9	0000000000000000
R10	0000000000000000
R11	0000000000000000
R12	0000000000000000
R13	0000000000000000
R14	0000000000000000
R15	0000000000000000

If in "HDT Mode", press "Refresh" and user will see VALID data

Node 0 | Core 0 | Refresh | Wr Chgs | Wr All

start | HDT6Overview.ppt | DebugPresentation_I... | AMD Hardware Debu... | 2:29 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Resume operation at current state

- APIC
- BTHB Debuggers
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- L2 Cache Arrays
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- PCI Configuration
- Processor Registers
  - CPU Registers
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  - Segment Registe
  - SEM Registers
  - Single MSR
  - SSE Registers
  - TR & SMM Regis

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1					

Refresh

Auto Refresh

CPU Registers 1

Name	Value
rAX	00000000FFDFFC50
rBX	00000000FFDFF000
rCX	000000000001E66C
rDX	00000000F3E93102
rSP	0000000080539544
rBP	0000000080539550
rSI	0000000080541DA0
rDI	0000000080542000
rFLAG	0000000000000213
rIP	00000000806B2FAA
CR0	8001003B
CR2	00000000BF8B08CF
CR3	0000000000039000
CR4	000006D9
CR8	00000000
R8	0000000000000000
R9	0000000000000000
R10	0000000000000000
R11	0000000000000000
R12	0000000000000000
R13	0000000000000000
R14	0000000000000000
R15	0000000000000000

Node 0 | Core 0 | Refresh | Wr Chgs | Wr All

Several "EXIT" options available to leave "HDT Mode"

start | HDT6Overview.ppt | DebugPresentation_I... | AMD Hardware Debu... | 2:30 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

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  - SEM Registers
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  - SSE Registers
  - TR & SMM Regis

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	0	n/a	n/a	n/a	n/a	n/a

Refresh

Auto Refresh

CPU Registers 1

Name	Value
rAX	00000000FFDFFC50
rBX	00000000FFDFF000
rCX	000000000001E66C
rDX	00000000F3E93102
rSP	0000000080539544
rBP	0000000080539550
rSI	0000000080541DA0
rDI	0000000080542000
rFLAG	0000000000000213
rIP	00000000806B2FAA
CR0	8001000
CR2	00000000B
CR3	000000
CR4	
CR8	
R8	00000000
R9	0000000000000
R10	0000000000000000
R11	0000000000000000
R12	0000000000000000
R13	0000000000000000
R14	0000000000000000
R15	0000000000000000

If user had good communication/connection and Exited "HDT Mode", pressed "Refresh" button, fields are color-coded to indicate that not in "HDT Mode"

Node 0 | Core 0 | Refresh | Wr Chgs | Wr All

start | HDT6Overview.ppt | DebugPresentation_I... | AMD Hardware Debu... | 2:30 PM

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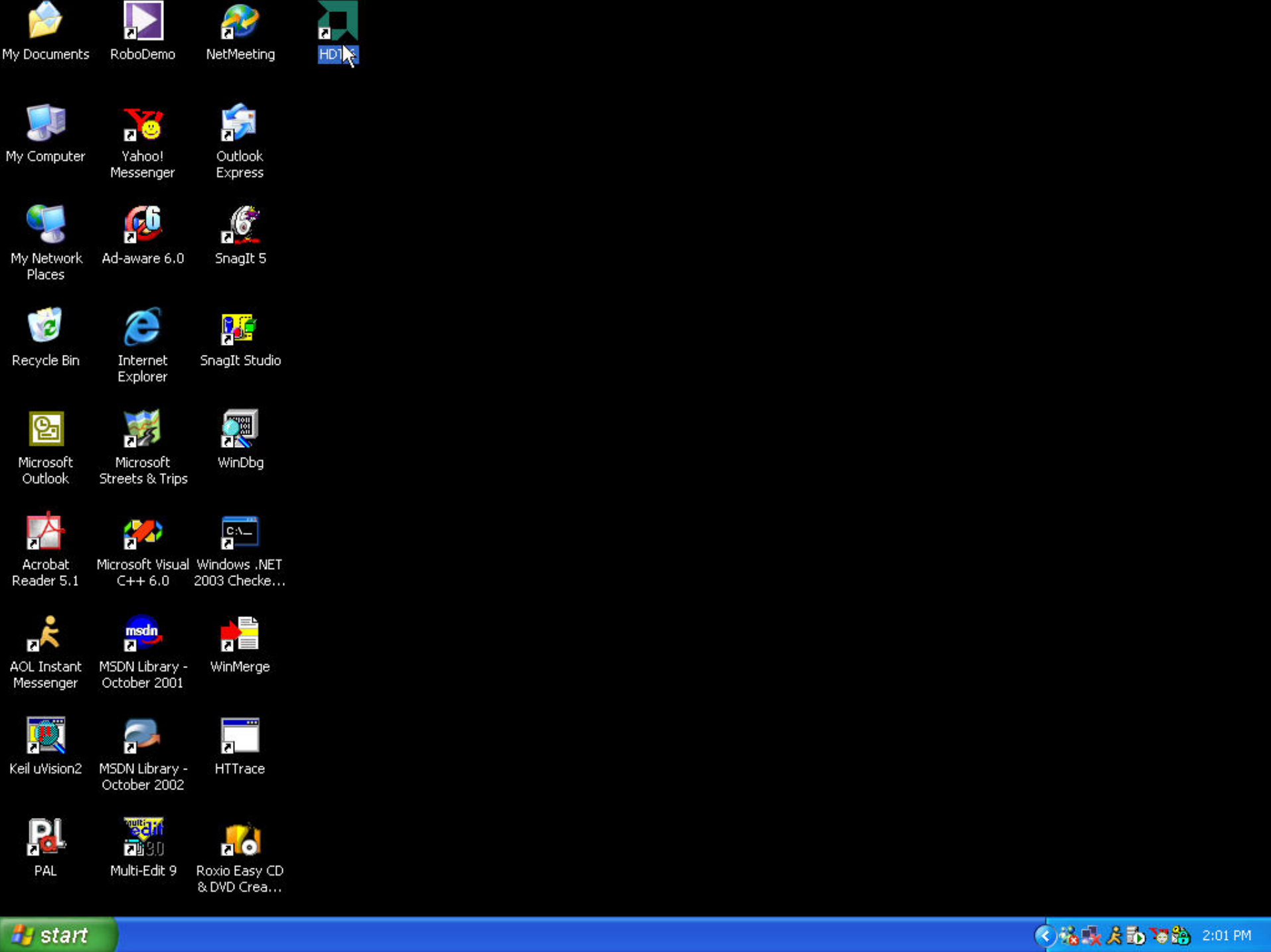
2) The HDT Layout


My Documents
RoboDemo
NetMeeting
HD1
My Computer
Yahoo! Messenger
Outlook Express
My Network Places
Ad-aware 6.0
SnagIt 5
Recycle Bin
Internet Explorer
SnagIt Studio
Microsoft Outlook
Microsoft Streets & Trips
WinDbg
Acrobat Reader 5.1
Microsoft Visual C++ 6.0
Windows .NET 2003 Checke...
AOL Instant Messenger
MSDN Library - October 2001
WinMerge
Keil uVision2
MSDN Library - October 2002
HTTrace
PAL
Multi-Edit 9
Roxio Easy CD & DVD Crea...
start
2:01 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

1) Menu Bar

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
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- Processor Registers
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  - Model Specific Registers
  - MTRR Registers
  - Performance Registers
  - Program Registers
  - Segment Registers
  - SEM Registers
  - Single MSR
  - SSE Registers
  - TR & SMM Registers

5) Feature Explorer

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB States	L2 Size
0	SH_B0/2-claw-754	0	0	1					

Refresh

Auto Refresh

3) Status Info

2) Toolbar

CPU Registers 1

Name	Value
rAX	00000000FFDFFC50
rBX	00000000FFDFF000
rCX	000000000008559D
rDX	00000000F3460102
rSP	0000000080539544
rBP	0000000080539550
rSI	0000000080541DA0
rDI	0000000080542000
rFLAG	0000000000000213
rIP	00000000806B2FAA
CR0	8001003B
CR2	000000000017A000
CR3	0000000000039000
CR4	000006D9
CR8	00000000
R8	0000000000000000
R9	0000000000000000
R10	0000000000000000
R11	0000000000000000

4) Work Area

Node 0 | Core 0 | Refresh | Wr Chgs | Wr All

Script Console

Console | History

>

6) Script Console

start | AMD Hardware Debu... | 4:29 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

*NOTE: HDT 6.0 and greater will ONLY support "Multi-Core" processors

Feature

- API
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers
  - CPU Registers
  - Debug Registers
  - FPU Registers
  - Last Branch Registers
  - MCA Registers
  - Model Specific Registers
  - MTRR Registers
  - Performance Registers
  - Program Registers
  - Segment Registers
  - SEM Registers
  - Single MSR

Node	BSP/AP	#DB Status	L2 Size

Refresh

Auto Refresh

CPU Registers 1

Name	Value
rAX	00000000FFDFFC50
rBX	00000000FFDFF000
rCX	000000000008559D
rDX	00000000F3460102
rSP	0000000080539544
rBP	0000000080539550
rSI	0000000080541DA0
rDI	0000000080542000
rFLAG	0000000000000213
rIP	00000000
CR0	8001003B
CR2	000000000017A000
CR3	00000
CR4	
C	
R8	00000000
R9	0000000000000000
R10	0000000000000000

5) Wr All: write ALL/EVERYTHING to target.

4) Wr Chngs: write ONLY user changes to target.

3) Refresh: retrieve current feature data from target.

1*) Node: selects physical processor package

Node 0 | Core 0 | Refresh | Wr Chgs | Wr All

Console | History

>

2*) Core: user can select which "CORE" to access for a "Multi-Core" processor.

start | AMD Hardware Debu... | 4:29 PM

Exploring the HDT Work Area

CONFIDENTIAL

- Menu Bar Area: provides access to basic functions.
  - The definition is similar to standard Windows® application
  - but ***Features*** and ***HDT*** menu bars define special HDT functions
- Toolbar Area: provides shortcut accesses to HDT functions.
- Status Info: provides overall target status, such as the number of Nodes, Cores, DBRdy, DBReq, etc.
- Working Area: contains HDT feature windows. The feature windows can be docked and floated.

Exploring the HDT Work Area

CONFIDENTIAL

- Node Selector: a selection box allowing the user to select the node (processor/socket) on a MP target to access.
- Core Selector: a selection box allowing the user to select the core within a node to access.
- Feature Explorer: shows the HDT features available. Double click on any feature to open that feature window in the Working Area.
- Script Console: a special command console that can accept HDT/Perl script commands and perform text display.

Exploring the HDT Work Area: Status Info

CONFIDENTIAL

- Basic status: info shown without being in HDT Mode. Updates automatically when DBRdy/DBReq changes.

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_C0/1/4-claw-754	0	0	1					

Refresh

☐ Auto Refresh

- Advanced status: info is shown only if accessing HDT command. Updates by clicking the *Refresh* button in Status Info area or selecting the option *Auto Refresh*.

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_C0/1/4-claw-754	0	0	1	0	Long 64-bit Mode	BSP	DBReq	1024

Refresh

☐ Auto Refresh

CONFIDENTIAL

3) HDT Toolbars

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Open Ctrl+O
Rename... F2
Save Ctrl+S
Save As...
Print Ctrl+P
Print Preview
Open Layout Ctrl+L
Save Layout As
Save Layout and Feature Data
Recent Layouts
Exit Alt+F4

PCI Configuration
Processor Registers

fo

CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
5H_B0/2-claw-754	0	0	0	n/a	n/a	n/a	n/a	n/a

Refresh
Auto Refresh

Toolbar - Similar to any Windows Application

Script Console

Console History

>

start AMD Hardware Debu... 2:30 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Copy Ctrl+C
Paste Ctrl+V
Find Ctrl+F

Featur

- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	0	n/a	n/a	n/a	n/a	n/a

Refresh

Auto Refresh

Script Console

Console History

>

start AMD Hardware Debu... 2:30 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Status Info Ctrl+I

Script Console Ctrl+N

Feature Explo

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers

How to Toggle "Status Info" and "Script Console" ON and OFF

Script Console

Console History

start AMD Hardware Debu... 2:31 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debug
- Data Cache A
- Debug Utilitie
- Download To
- HyperTransp
- I/O Ports
- Instruction Ca
- JTAG Instruc
- L2 Cache Arr
- Memory Debu
- PCI Configura
- Processor Re

- APIC
  - I/O APIC Locator
  - IO APIC Registers
  - Local APIC Registers
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers

An alternate way to view "Features" instead of through "Feature Explorer"

Script Console

Console History

start AMD Hardware Debu... 2:31 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Commands
Miscellaneous
Script Console

HDT On Alt+F5
Exit HDT F5
Exit rIP
Exit HDT Resume
HDT Reset
HDT Init
HDT SMI
HDT RSM
Set LBR=1
Set BPS=0
Disable BIST
Single Step F8
Step Transfer
Flush Cache
Flush TLB
Reset TAP
DB Req Assert
DB Req DeAssert
Toggle DB Req
DBReady
PollDBReady

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers

An alternate way to view "Commands" instead of through "Toolbar"

start AMD Hardware Debu... 2:31 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Commands
Miscellaneous
Script Console

Refresh All
Logging
Options

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers

HDT is very customizable, allowing users to change interface to own preference

Script Console

Console History

start AMD Hardware Debu... 2:31 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers

Property Page

- General
- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Technolo
- Instruction Cache Arrays
- JTAG Instructions
- Memory Debuggers
- PCI Configuration
- Processor Registers

Name	Value
Refreshed Color	
Written Color	Blue
Changed Color	Red
ReadOnly Color	Aqua
Background Error Color	Pink
Background Invalid Color	Yellow
Detect CPU Reset	☐
Detect Trigger In	☑
IO Access Node	0

Default Apply OK Cancel

If BIOS resets, will break into HDT if "Detect CPU Reset" checked. Only works with USB Possum Interface

start AMD Hardware Debu... 2:32 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers

Property Page

- General
- APIC
  - I/O APIC Locator
  - IO APIC Registers
  - Local APIC Registers
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Technolo
- Instruction Cache Arrays
- JTAG Instructions
- Memory Debuggers
- PCI Configuration
- Processor Registers

Name	Value
Open with Node	0
Open with Core	0
Refresh sync with Single Step	☐
Refresh sync with HDT On	☐
Refresh sync with HDT Off	☐

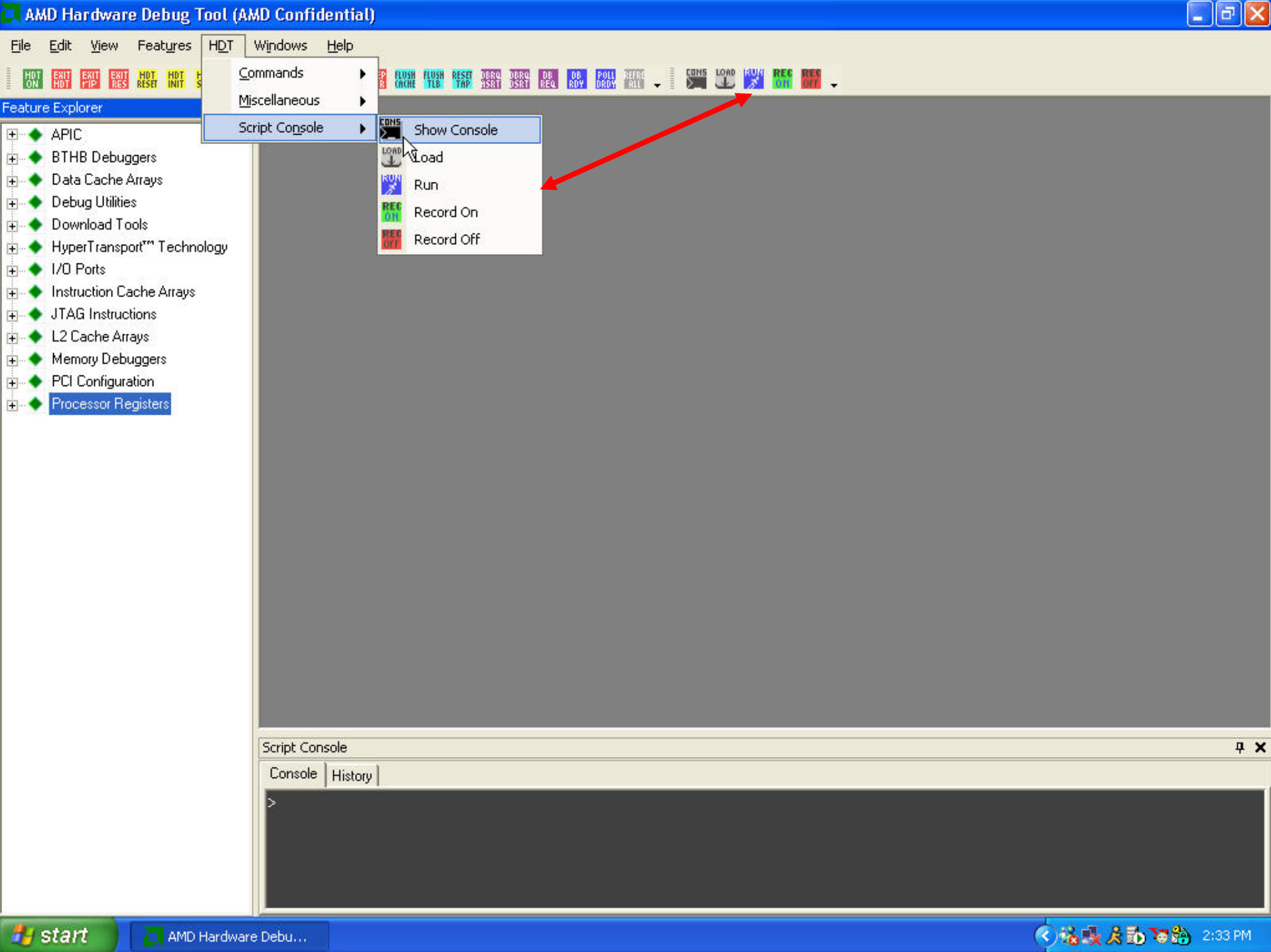
Default Apply OK Cancel

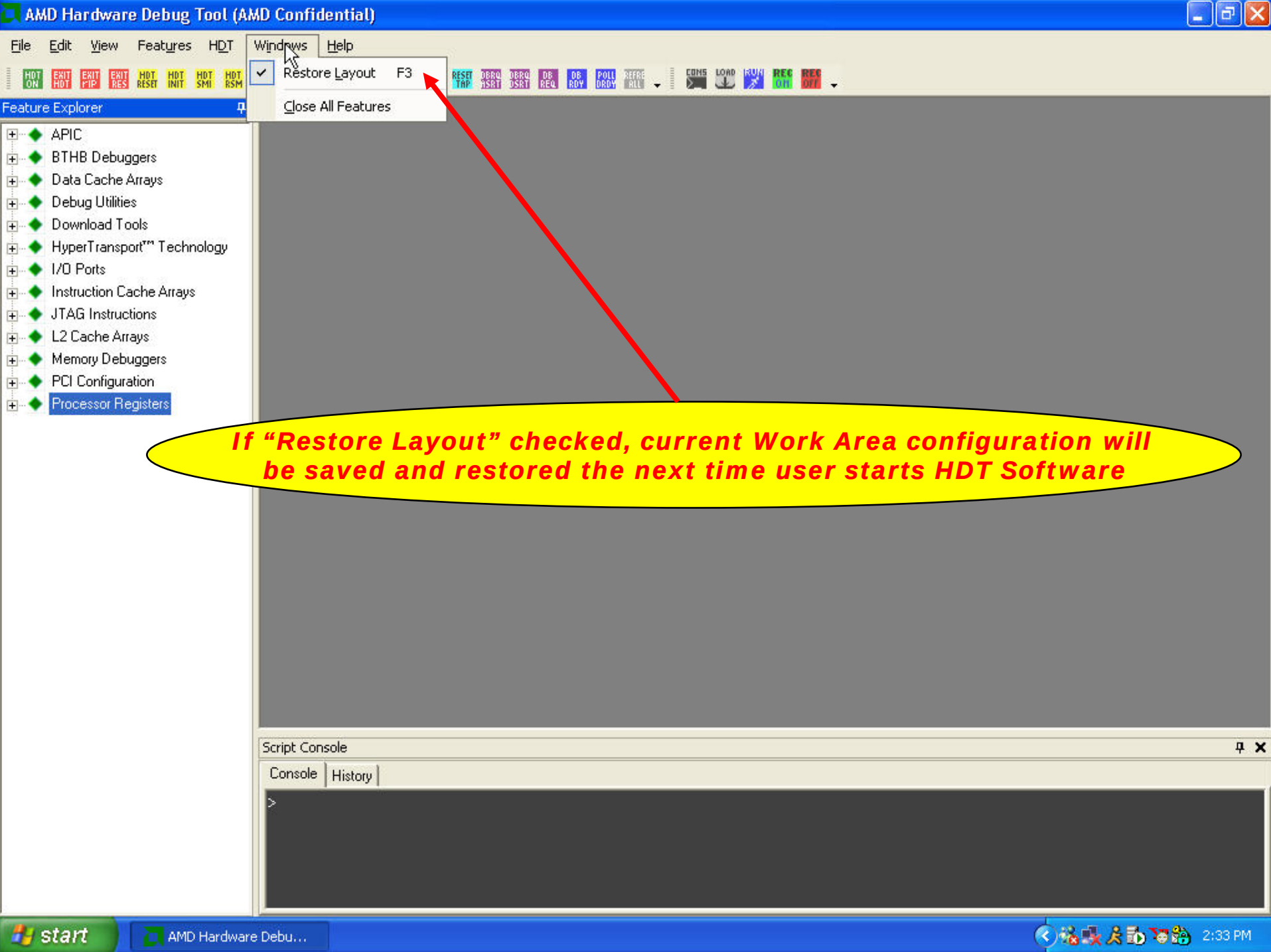
Script Console

Console History

>

start AMD Hardware Debu... 2:32 PM


AMD Hardware Debug Tool (AMD Confidential)
File
Edit
View
Features
HDT
Windows
Help
Commands
Miscellaneous
Script Console
Show Console
Load
Run
Record On
Record Off
Feature Explorer
APIC
BTHB Debuggers
Data Cache Arrays
Debug Utilities
Download Tools
HyperTransport™ Technology
I/O Ports
Instruction Cache Arrays
JTAG Instructions
L2 Cache Arrays
Memory Debuggers
PCI Configuration
Processor Registers
Script Console
Console
History
start
AMD Hardware Debu...
2:33 PM


AMD Hardware Debug Tool (AMD Confidential)
File Edit View Features HDT Windows Help
Restore Layout F3
Close All Features
Feature Explorer
APIC
BTHB Debuggers
Data Cache Arrays
Debug Utilities
Download Tools
HyperTransport™ Technology
I/O Ports
Instruction Cache Arrays
JTAG Instructions
L2 Cache Arrays
Memory Debuggers
PCI Configuration
Processor Registers
If "Restore Layout" checked, current Work Area configuration will be saved and restored the next time user starts HDT Software
Script Console
Console
History
start
AMD Hardware Debu...
2:33 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers

About...

AMD

AMD HDT (AMD Confidential)

AMD HDT Version: 6.0.812.26446
October 01, 2004

JTAG Framework Version: 000103182377800d
Grid Control Version: 2.0.5.1
Suite Tools Version: 2.0.5.1
Shared Control Version: 2.0.5.1

USB 2.0

Legal Agreement

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All rights reserved.

Click here to report bug or enhancement

Click on following link to send email to debug.tools@amd.com.

start AMD Hardware Debu... About... 2:34 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Te
- I/O Ports
- Instruction Cache Arr
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1					

Refresh

Auto Refresh

Script Console

Console History

>

start AMD Hardware Debu... 4:48 PM

"Toolbar" can be dragged and moved to different area

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Te
- I/O Ports
- Instruction Cache Arr
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1					

Refresh

Auto Refresh

Script Console

Console History

>

start AMD Hardware Debu... 4:49 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Te
- I/O Ports
- Instruction Cache Arr
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1					

Refresh

Auto Refresh

"Toolbar" can also be made floatable by dragging to desired location

Script Console

Console History

start AMD Hardware Debu... 4:49 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Te
- I/O Ports
- Instruction Cache Arr
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1					

Refresh

Auto Refresh

ScriptConso...

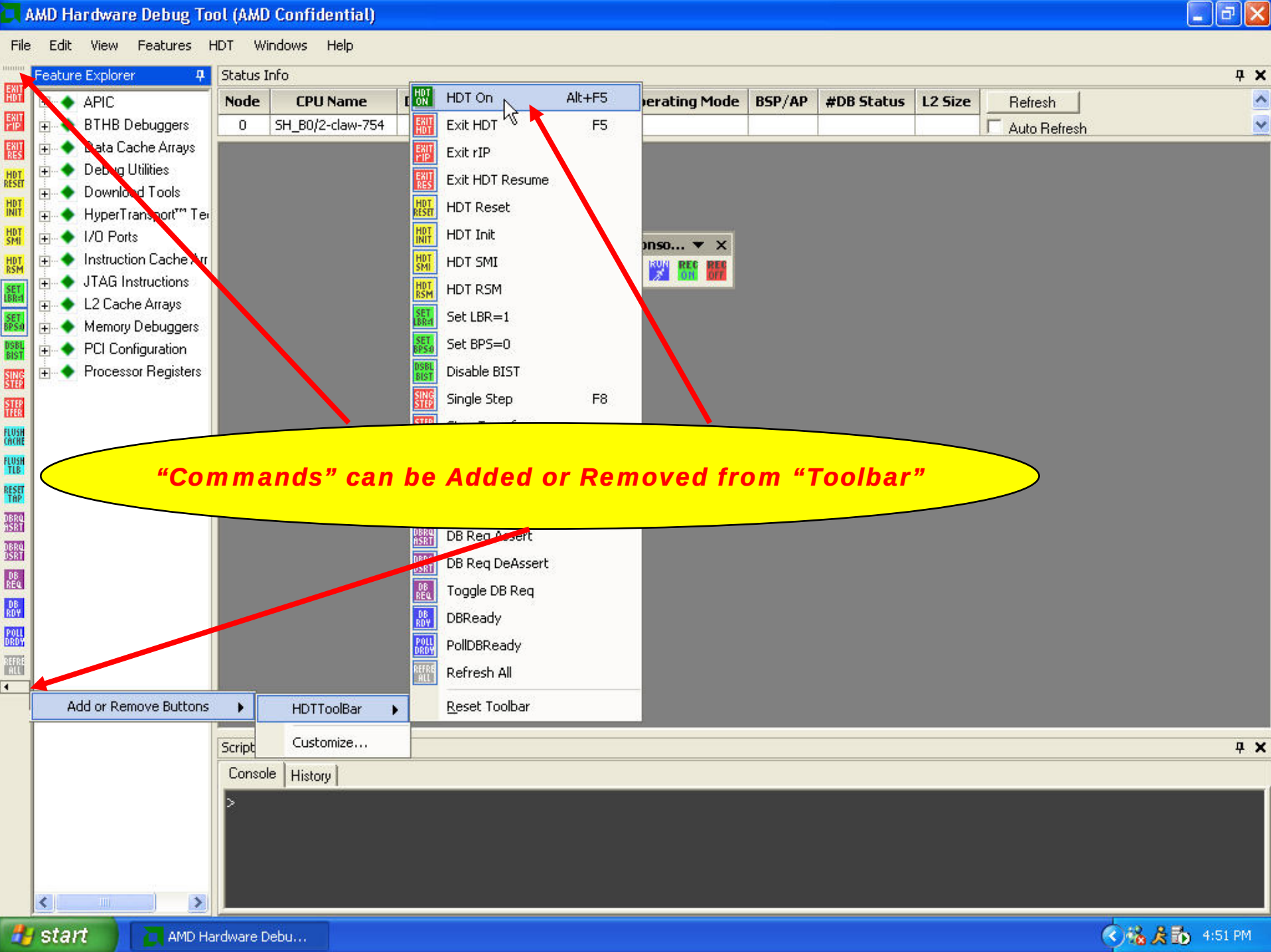
CONS LOAD RUN REC ON REC OFF

Script Console

Console History

>

start AMD Hardware Debu... 4:50 PM



"Commands" can be Added or Removed from "Toolbar"

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Te
- I/O Ports
- Instruction Cache Arr
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1					

Refresh

Auto Refresh

ScriptConso...

Add or Remove Buttons

HDTToolBar

Customize...

Script

Console History

start AMD Hardware Debu... 4:51 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Favorite Layouts Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Te
- I/O Ports
- Instruction Cache Arr
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1					

Refresh

Auto Refresh

ScriptConso...

Customize

Toolbars | Commands | Options

Toolbars:

- MainMenuBar
- HDTToolBar
- ScriptConsoleToolbar

New

Delete

Reset

Close

User can TURN ON / OFF Toolbars through "Customize"

start AMD Hardware Debu... 4:52 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Favorite Layouts Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Te
- I/O Ports
- Instruction Cache Arr
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1					

Refresh

Auto Refresh

ScriptConso...

Customize

Toolbars | Commands | Options

Toolbars:

- MainMenuBar
- HDTToolBar
- ScriptConsoleToolbar

New

Delete

Reset

Close

Script Console

Un-checking removes specified "Toolbar"

start AMD Hardware Debu... 4:52 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Te
- I/O Ports
- Instruction Cache Arr
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2
0	SH_B0/2-claw-754	0	0	1					

ScriptConsoleToolbar
HDTToolBar
Customize...

As a shortcut, user can Right-Click and customize "Toolbars"

Script Console

Console | History

>

start AMD Hardware Debu... 5:00 PM

CONFIDENTIAL

4) Working With Panels

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Reg

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	0	n/a	n/a	n/a	n/a	n/a

Refresh

Auto Refresh

Panels can be moved and rearranged to desired location.
"Push Pin" minimizes (horizontal pin) and maximizes (vertical pin) panel

Script Console

Console History

start AMD Hardware Debu... 2:08 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers

re	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
	0	n/a	n/a	n/a	n/a	n/a

Refresh

Auto Refresh

start AMD Hardware Debu... 2:09 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	0	n/a	n/a	n/a	n/a	n/a

Refresh

Auto Refresh

Panel now minimized and can be shown by hovering mouse over "Feature Explorer"

Script Console

Console History

>

start AMD Hardware Debu... 2:09 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers

re	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
	0	n/a	n/a	n/a	n/a	n/a

Refresh

Auto Refresh

start AMD Hardware Debu... 2:09 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers

Dockable
Floating
Auto Hide

CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
H_B0/2-claw-754	0	0	0	n/a	n/a	n/a	n/a	n/a

Refresh

Auto Refresh

User can also Right-Click on panel to display and select settings

Script Console

Console History

>

start AMD Hardware Debu... 2:29 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers
  - CPU Registers
  - Debug Registers
  - FPU Registers
  - Last Branch Registers
  - MCA Registers
  - Model Specific Registers
  - MTRR Registers
  - Performance Registers
  - Program Registers
  - Segment Registers
  - SEM Registers
  - Single MSR
  - SSE Registers
  - TR & SMM Registers

Let us continue to explore how to manage "Work Area"

Script Console

Console | History

>

start AMD Hardware Debu... 2:34 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache A
- JTAG I
- L2 Cache Array
- Memory Debuggers
- PCI Configuration
- Processor Registers
  - CPU Registers
  - Debug Registers
  - FPU Registers
  - Last Branch Registers
  - MCA Registers
  - Model Specific Registers
  - MTRR Registers
  - Performance Registers
  - Program Registers
  - Segment Registers
  - SEM Registers
  - Single MSR
  - SSE Registers
  - TR & SMM Registers

CPU Registers 1

Name	Value
rAX	
rBX	
rCX	
rDX	
rSP	
rBP	
rIP	
CR0	
CR2	
CR3	
CR4	
CR8	
R8	
R9	
R10	
R11	
R12	
R13	
R14	
R15	

Depending on user's platform, user can select which "Node" or "Core" to display specified information for

Node 0 | Core 0 | Refresh | Wr Chgs | Wr All

Script Console

Console | History

>

start | AMD Hardware Debu... | 2:35 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Te
- I/O Ports
- Instruction Cache Ar
- JTAG Ins
- L2 Cach
- Memory Debuggers
- PCI Configuration
- Processor Registers
  - CPU Registers
  - Debug Registers
  - FPU Registers
  - Last Branch Reg
  - MCA Registers
  - Model Specific R
  - MTRR Registers
  - Performance Reg
  - Program Register
  - Segment Registe
  - SEM Registers
  - Single MSR
  - SSE Registers
  - TR & SMM Regis

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1					

Refresh

Auto Refresh

CPU Registers 1 | CPU Registers 2

Name	Value
rAX	
rBX	
rCX	
rSI	
rDI	
rFLAG	
rIP	
CR0	
CR2	
CR3	
CR4	
CR8	
R8	
R9	
R10	
R11	

Node 0 | Core 0 | Refresh | Wr Chgs | Wr All

User can bring up MANY instances of same "Feature".
Each new feature will be auto-incremented and added as a new tab group

Script Console

Console | History

>

start | AMD Hardware Debu... | 5:12 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers
  - CPU Registers
  - Debug Registers
  - FPU Registers
  - Last Branch Registers
  - MCA Registers
  - Model Specific Registers
  - MTRR Registers
  - Performance Registers
  - Program Registers
  - Segment Registers
  - SEM Registers
  - Single MSR
  - SSE Registers
  - TR & SMM Registers

CPU Registers 1 | Debug Registers 1

Name	Value
DR0	
DR0_Data_Match	
DR0_Data_Mask	
DR0_ADDR_MASK	
DR1	
DR2	
DR3	
DR6	
DR7	
DBGCTLMSR	
DBGCTLMSR2	
DebugStatus	
ExcpBP_RIP	
ExcpBP_RIP_MASK	
ExcpBP_Ctl	
McodeCtl	

Node 0 | Core 0 | Refresh | Wr Chgs | Wr All

Script Console

Console | History

start | AMD Hardware Debu... | 2:35 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Inst
- L2 Cach
- Memory Debuggers
- PCI Configuration
- Processor Registers
  - CPU Registers
  - Debug Registers
  - FPU Registers
  - Last Branch Registers
  - MCA Registers
  - Model Specific Registers
  - MTRR Registers
  - Performance Registers
  - Program Registers
  - Segment Registers
  - SEM Registers
  - Single MSR
  - SSE Registers
  - TR & SMM Registers

CPU Registers 1 | Debug Registers 1 | **Performance Registers 1**

Name	Value
PERF_CTR0	
PERF_CTR1	
PERF_CTR2	
PERF_CTR3	
PERF_CTL0	

Each new "Feature" invoked will be added to CURRENT tab group, but can further be separated into its own group for better management.

Node 0 | Core 0 | Refresh | Wr Chgs | Wr All

Script Console

Console | History

start | AMD Hardware Debu... | 2:36 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor R...
  - Last Branch Registers
  - MCA Registers
  - Model Specific Registers
  - MTRR Registers
  - Performance Registers
  - Program Registers
  - Segment Registers
  - SEM Registers
  - Single MSR
  - SSE Registers
  - TR & SMM Registers

CPU Registers 1 | Debug Registers 1 | Performance Registers 1

Name	Value
PERF_CTR0	
PERF_CTR1	
PERF_CTR2	
PERF_CTR3	
PERF_CTL0	
PERF_CTL1	
PERF_CTL2	
PERF_CTL3	
TSC	

- Dockable
- Floating
- Rename Performance Registers 1 F2
- New Horizontal Tab Group
- New Vertical Tab Group

At any time, user can Right-Click on a feature and create a new Horizontal/Vertical Tab Group, in addition to additional settings seen above.

Node 0 | Core 0 | Refresh | Wr Chgs | Wr All

Script Console

Console | History

start | AMD Hardware Debu... | 2:37 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers
  - CPU Registers
  - Debug Registers
  - FPU Registers
  - Last Branch Registers
  - MCA Registers
  - Model Specific Registers
  - MTRR Registers
  - Performance Registers
  - Program Registers
  - Segment
  - SSE Registers
  - TR & SMM Registers

CPU Registers 1 | Debug Registers 1

Name	Value
DR0	
DR0_Data_Match	
DR0_Data_Mask	
DR0_ADDR_MASK	
DR1	
DR2	
DR3	
DR6	
DR7	
DBGCTLMSR	
DBGCTLMSR2	
DebugStatus	
ExcpBP_RIP	
ExcpBP_RIP_MASK	
ExcpBP_Ctl	
McodeCtl	

Performance Registers 1

Name	Value
PERF_CTR0	
PERF_CTR1	
PERF_CTR2	
PERF_CTR3	
PERF_CTL0	
PERF_CTL1	
PERF_CTL2	
PERF_CTL3	
TSC	

Core 0 Refresh Wr Chgs Wr All

Creating a NEW Vertical Group separates the specified feature into a new group

Script Console

Console | History

start AMD Hardware Debu... 2:38 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers
  - CPU Registers
  - Debug Registers
  - FPU Registers
  - Last Branch Registers
  - MCA Registers
  - Model Specific Registers
  - MTRR Registers
  - Performance Registers
  - Program Registers
  - Segment
  - SSE Registers
  - TR & SMM Registers

CPU Registers 1 | Debug Registers 1

Name	Value
DR0	
DR0_Data_Match	
DR0_Data_Mask	
DR0_ADDR_MASK	
DR1	
DR2	
DR3	
DR6	
DR7	
DBGCTLMSR	
DBGCTLMSR2	
DebugStatus	
ExcpBP_RIP	
ExcpBP_RIP_MASK	
ExcpBP_Ctl	
McodeCtl	

Performance Registers 1

Name	Value
PERF_CTR0	
PERF_CTR1	
PERF_CTR2	
PERF_CTR3	
PERF_CTL0	
PERF_CTL1	
PERF_CTL2	
PERF_CTL3	
TSC	

Dockable
Floating
Rename Performance Registers 1 F2
Move Previous

Core 0 Refresh Wr Chgs Wr All

User may decide to revert back, and move this current/selected feature back to the previous group

Script Console

Console | History

start AMD Hardware Debu... 2:38 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers
  - CPU Registers
  - Debug Registers
  - FPU Registers
  - Last Branch Registers
  - MCA Registers
  - Model Specific Registers
  - MTRR Registers
  - Performance Registers
  - Program Registers
  - Segment
  - SSE Registers
  - TR & SMM Registers

CPU Registers 1 | Debug Registe

Name	Value
DR0	
DR0_Data_Match	
DR0_Data_Mask	
DR0_ADDR_MASK	
DR1	
DR2	
DR3	
DR6	
DR7	
DBGCTLMSR	
DBGCTLMSR2	
DebugStatus	
ExcpBP_RIP	
ExcpBP_RIP_MASK	
ExcpBP_Ctl	
McodeCtl	

Dockable
Floating
Rename Debug Registers 1 F2
New Horizontal Tab Group
New Vertical Tab Group

Core 0 Refresh Wr Chgs Wr All

Script Console

Console History

>

start AMD Hardware Debu... 2:38 PM

A different example of creating a NEW Horizontal Tab Group for this feature.

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers
  - CPU Registers
  - Debug Registers
  - FPU Registers
  - Last Branch Registers
  - MCA Registers
  - Model Specific Registers
  - MTRR Registers
  - Performance Registers
  - Program Registers
  - Segment Registers
  - SEM Registers
  - Single MSR
  - SSE Registers
  - TR & SMM Registers

CPU Registers 1 | Performance Registers 1

Name	Value
PERF_CTR0	
PERF_CTR1	
PERF_CTR2	
PERF_CTR3	
PERF_CTL0	
PERF_CTL1	
PERF_CTL2	
PERF_CTL3	
TSC	

Node 0 | Core 0 | Refresh | Wr Chgs | Wr All

Debug Registers 1

Name	Value
DR0	
DR0_Data_Match	
DR0_Data_Mask	
DR0_ADDR_MASK	
DR1	
DR2	
DR3	
DR6	
DR7	
DBGCTLMSR	
DBGCTLMSR2	

Node 0 | Core 0 | Refresh | Wr Chgs | Wr All

Now 2 Groups are created!

Script Console

Console | History

>

start | AMD Hardware Debu... | 2:38 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers
  - CPU Registers
  - Debug Registers
  - FPU Registers
  - Last Branch Registers
  - MCA Registers
  - Model Specific Registers
  - MTRR Registers
  - Performance Registers
  - Program Registers
  - Segment Registers
  - SEM Registers
  - Single MSR
  - SSE Registers
  - TR & SMM R...

CPU Registers 1 | Performance Registers 1

Name	Value
PERF_CTR0	
PERF_CTR1	
PERF_CTR2	
PERF_CTR3	
PERF_CTL0	
PERF_CTL1	
PERF_CTL2	
PERF_CTL3	
TSC	

Node 0 | Core 0 | Refresh | Wr Chgs | Wr All

Debug Registers 1 | Last Branch Registers 1

Name	Value
LastBranchFromIP	
LastBranchToIP	
LastIntFromIP	
LastIntToIP	

Wr Chgs | Wr All

A NEW feature invoked will be added to the group that was previously highlighted.

start | AMD Hardware Debu... | 2:39 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers
  - CPU Registers
  - Debug Registers
  - FPU Registers
  - Last Branch Registers
  - MCA Registers
  - Model Specific Registers
  - MTRR Registers
  - Performance Registers
  - Program Registers
  - Segment Registers
  - SEM Registers
  - Single MSR
  - SSE Registers
  - TR & SMM Registers

CPU Registers 1 | Performance Registers 1

Name	Value
PERF_CTR0	
PERF_CTR1	
PERF_CTR2	
PERF_CTR3	
PERF_CTL0	
PERF_CTL1	
PERF_CTL2	
PERF_CTL3	
TSC	

Node 0 | Core 0 | Refresh | Wr Chgs | Wr All

Debug Registers 1 | Last Branch Registers 1

Name	
DR0	
DR0_Data_Match	
DR0_Data_Mask	
DR0_ADDR_MASK	
DR1	
DR2	
DR3	
DR6	
DR7	
DBGCTLMSR	
DBGCTLMSR2	

Dockable
Floating
Rename Debug Registers 1 F2
Move Previous
New Horizontal Tab Group

Node 0 | Core 0 | Refresh | Wr Chgs | Wr All

Script Console

Console | History

>

start | AMD Hardware Debu... | 2:40 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers
  - CPU Registers
  - Debug Registers
  - FPU Registers
  - Last Branch Registers
  - MCA Registers
  - Model Specific Registers
  - MTRR Registers
  - Performance Registers
  - Program Registers
  - Segment Registers
  - SEM Registers
  - Single MSR
  - SSE Registers
  - TR & SMM Registers

CPU Registers 1 | Performance Registers 1 | **Debug Registers 1**

Name	Value
DR0	
DR0_Data_Match	
DR0_Data_Mask	
DR0_ADDR_MASK	
DR1	
DR2	
DR3	
DR6	
DR7	
DBGCTLMSR	
DBGCTLMSR2	

Node 0 | Core 0 | Refresh | Wr Chgs | Wr All

Last Branch Registers 1

Name	Value
LastBranchFromIP	
LastBranchToIP	
LastIntFromIP	
LastIntToIP	

Node 0 | Core 0 | Refresh | Wr Chgs | Wr All

Script Console

Console | History

>

start | AMD Hardware Debu... | 2:40 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers
  - CPU Registers
  - Debug Registers
  - FPU Registers
  - Last Branch Registers
  - MCA Registers
  - Model Specific Registers
  - MTRR Registers
  - Performance Registers
  - Program Registers
  - Segment Registers
  - SEM Registers
  - Single MSR
  - SSE Registers
  - TR & SMM Registers

CPU Registers 1 | Performance Registers 1 | Debug Registers 1

Name	Value
DR0	
DR0_Data_Match	
DR0_Data_Mask	
DR0_ADDR_MASK	
DR1	
DR2	
DR3	
DR6	
DR7	
DBGCTLMSR	
DBGCTLMSR2	

Node 0 | Core 0 | Refresh | Wr Chgs | Wr All

Last Branch Registe

Name	Va
LastBranchFromIP	
LastBranchToIP	
LastIntFromIP	
LastIntToIP	

Dockable
Floating
Rename Last Branch Registers 1 F2
Move Previous

Refresh | Wr Chgs | Wr All

Script Console

Console | History

>

start | AMD Hardware Debu... | 2:47 PM

User can rename feature's "Title Bar" to own preference.

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers
  - CPU Registers
  - Debug Registers
  - FPU Registers
  - Last Branch Registers
  - MCA Registers
  - Model Specific Registers
  - MTRR Registers
  - Performance Registers
  - Program Registers
  - Segment Registers
  - SEM Registers
  - Single MSR
  - SSE Registers
  - TR & SMM Registers

CPU Registers 1 | Performance Registers 1 | Debug Registers 1

Name	Value
DR0	
DR0_Data_Match	
DR0_Data_Mask	
DR0_ADDR_MASK	
DR1	
DR2	
DR3	
DR6	
DR7	
DBGCTLMSR	
DBGCTLMSR2	

Node 0 | Core 0 | Refresh | Wr Chgs | Wr All

Rename Feature

Old Name: Last Branch Registers 1

Enter New Name: LBR Node 0

OK | Cancel

Last Branch Registers

Name	Value
LastBranchFromIP	
LastBranchToIP	
LastIntFromIP	
LastIntToIP	

Node 0 | Core 0 | Refresh | Wr Chgs | Wr All

Script Console

Console | History

start | AMD Hardware Debu... | Rename Feature | 2:48 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers
  - CPU Registers
  - Debug Registers
  - FPU Registers
  - Last Branch Registers
  - MCA Registers
  - Model Specific Registers
  - MTRR Registers
  - Performance Registers
  - Program Registers
  - Segment
  - SSE Registers
  - TR & SMM Registers

CPU Registers 1 | Performance Registers 1 | Debug Registers 1

Name	Value
DR0	
DR0_Data_Match	
DR0_Data_Mask	
DR0_ADDR_MASK	
DR1	
DR2	
DR3	
DR6	
DR7	
DBGCTLMSR	
DBGCTLMSR2	

Node 0 | Core 0 | Refresh | Wr Chgs | Wr All

LBR Node 0

Name	Value
LastBranchFromIP	
LastBranchToIP	
LastIntFromIP	
LastIntToIP	

Core 0 | Refresh | Wr Chgs | Wr All

Script Console

Console | History

>

start | AMD Hardware Debu... | 2:48 PM

Name was changed from default "Last Branch Register 1" to user-specified name "LBR Node 0"

Agenda

CONFIDENTIAL

- Introduction to HDT
- Hardware Requirements
- HDT Protocol / Internals
- Exploring the Work Area
- HDT Features
- Practical HDT Scenarios / Examples
- Q&A

HDT Features

CONFIDENTIAL

Topics:

1. Common Feature Controls
2. APIC
3. BTHB Debuggers
4. Cache Arrays
5. Data, Instruction, and L2 Cache Line Translator
6. Debug Utilities
7. Download Tools
8. HyperTransport™
9. I/O Ports
10. Memory Debuggers
11. PCI Configuration
12. Processor Registers
13. Script Console

HDT Features

CONFIDENTIAL

- Platform-based feature
  - The info or data applies for the entire target platform, such as PCI device info, HyperTransport™ info, etc.
  - Neither Node nor Core selection needed. The info does not apply to any specific node or core.
  - Although the info does not apply to any Node or Core, an accessed Node will be defined in property page to identify the communication path.
- Node-based feature
  - The feature info or data applies for a Node that is identified by the Node selector, such as Northbridge registers.
- Core-based feature
  - The info or data of a specific core will be defined by a combination of Node and Core selectors, such as GPRs.

CONFIDENTIAL

1) Common Feature Controls

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1					

Refresh

Auto Refresh

CPU Registers 1

Name	Value
rAX	00000000FFDFFC50
rBX	00000000FFDFF000
rCX	0000000000000486
rDX	00000000FFFFFFFF
rSP	0000000080539544
rBP	0000000080539550
rSI	0000000080541DA0
rDI	0000000080542000
rFLAG	0000000000000217
rIP	00000000806B2FAA
CR0	8001003B
CR2	00000000E14C4036
CR3	0000000000039000
CR4	000006D9
CR8	00000000
R8	11
R9	0000000000000000
R10	0000000000000000
R11	0000000000000000

Node 0 | Core 0 | Refresh | Wr Chgs | Wr All

Script Console

User can edit register fields by clicking in area and typing desired value. Reminder, values will not be written unless submitted.

start | AMD Hardware Debu... | 4:44 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq
0	SH_B0/2-claw-754	0

CPU Registers 1

Name	Value
rAX	00000000FFDFFC50
rBX	00000000FFDFF000
rCX	0000000000000486
rDX	00000000FFFFFFFF
rSP	0000000080539544
rBP	0000000080539550
rSI	0000000080541DA0
rDI	0000000080542000
rFLAG	0000000000000217
rIP	00000000806B2FAA
CR0	8001003B
CR2	00000000E14C4036
CR3	0000000000039000
CR4	000006D9
CR8	00000000
R8	0000000000000011
R9	0000000000000000
R10	0000000000000000
R11	0000000000000000

Node 0 | Core 0 | Refresh | Wr Chgs | Wr All

Script Console

Property Page

- General
- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Technolo
- Instruction Cache Arrays
- JTAG Instructions
- Memory Debuggers
- PCI Configuration
- Processor Registers

Name	Value
Refreshed Color	@
Written Color	Blue @
Changed Color	Red @
ReadOnly Color	Aqua @
Background Error Color	Pink @
Background Invalid Color	Yellow @
Detect CPU Reset	☐
Detect Trigger In	☑
IO Access Node	0

Default | Apply | OK | Cancel

User knows that value is not written to target through color-coding.
User can specify own settings.

start | AMD Hardware Debu... | 4:52 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1					

Refresh

Auto Refresh

CPU Registers 1

Name	Value
rAX	00000000FFDFFC50
rBX	00000000FFDFF000
rCX	0000000000000486
rDX	00000000FFFFFFFF
rSP	0000000080539544
rBP	0000000080539550
rSI	0000000080541DA0
rDI	0000000080542000
rFLAG	0000000000000217
rIP	00000000080
CR0	80
CR2	00000000E1
CR3	0000000000
CR4	00
CR8	00
R8	0000000000
R9	0000000000
R10	0000000000
R11	0000000000

Copy
Paste
Find...
Reset current cell to Zero
Reset all cells to Zero
Display Type
View Bitmap...
Load...
Save As...
Show Register Address
Properties

Node 0 | Core 0 | Refresh | Wr Chgs | Wr All

Script Console

User can Right-Click on field to show features/settings available for selected field.

start | AMD Hardware Debu... | 4:45 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB De
- Data Cac
- Debug U
- Downloa
- HyperTra
- I/O Ports
- Instructio
- JTAG Ins
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size

Refresh

Auto Refresh

Bitmap Dialog

44	43	40	39	36	35	32	31	28	27	24	23	20	19	16	15	12	11	8	7	4	3	0
0	0		0		0		8		0		6		B		2		F		A		A	

0x00000000806B2FAA

OK Cancel

rBP	0000000080539550
rSI	0000000080541DA0
rDI	0000000080542000
rFLAG	0000000000000217
rIP	00000000806B2FAA
CR0	8001003B
CR2	00000000E14C4036
CR3	0000000000039000
CR4	000006D9
CR8	00000000
R8	0000000000000011
R9	0000000000000000
R10	0000000000000000
R11	0000000000000000

Node 0 Core 0 Refresh Wr Chgs Wr All

Script Console

Console History

>

start AMD Hardware Debu... Bitmap Dialog 4:46 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1					

Refresh

Auto Refresh

CPU Registers 1

Name	Value
rAX	00000000FFDFFC50
rBX	00000000FFDFF000
rCX	0000000000000486
rDX	00000000FFFFFFFF
rSP	0000000080539544
rBP	0000000080539550
rSI	0000000080541DA0
rDI	0000000080542000
rFLAG	000000000
rIP	000000008
CR0	8
CR2	00000000E
CR3	000000000
CR4	0
CR8	0
R8	000000000
R9	000000000
R10	000000000
R11	000000000

Copy
Paste
Find...
Reset current cell to Zero
Reset all cells to Zero
Display Type
View Bitmap...
Subfields...
Load...
Save As...
Show Register Address
Properties

Node 0 | Core 0 | Refresh | Wr Chgs | Wr All

Script Console

Some registers may or may not have sub-fields depending on the register definition.

start | AMD Hardware Debu... | 4:46 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1					

Refresh

Auto Refresh

CPU Registers 1

Name	Value
rAX	00
rBX	00
rCX	00
rDX	00
rSP	00
rBP	00
rSI	00
rDI	00
rFLAG	00
rIP	00
CR0	
CR2	00
CR3	00
CR4	
CR8	
R8	00
R9	00
R10	00
R11	00

rFLAG Subfields

Name	Start Bit	End Bit	Value
CarryFlag	0	0	☑ CF
ParityFlag	2	2	☑ PF
AuxiliaryFlag	4	4	☑ AF
ZeroFlag	6	6	☐ ZF
SignFlag	7	7	☐ SF
TrapFlag	8	8	☐ TF
InterruptFlag	9	9	☑ IF
DirectionFlag	10	10	☐ DF
OverflowFlag	11	11	☐ OF
IOPrivlegeFlag	12	12	☐ IOPL
NestedTask	14	14	☐ NT
ResumeFlag	16	16	☐ RF
Virtual8086Mode	17	17	☐ VM
AlignmentCheck	18	18	☐ AC
VirtualInterruptFlag	19	19	☐ VIF
VirtualInterruptPending	20	20	☐ VIP

OK Cancel

Node 0 Core 0 Refresh Wr Chgs Wr All

Script Console

Console History

>

start AMD Hardware Debu... 4:47 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
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- Memory Debuggers
- PCI Configuration
- Processor Registers

HWCR Subfields

Name	Start Bit	End Bit	Value
SMM Code Lock	0	0	☑ SMMLOCK
Slow SFENCE Enable	1	1	☐ SLOWFENCE
Cacheable Memory Disable	3	3	☐ TLBCACHEDIS
INVD to WBINVD Conversion	4	4	☑ INVD_WBINVD
MROM Patching Disable	5	5	☑ PATCHDIS
TLB Flush Filter Disable	6	6	☑ FFDIS
Disable x86 LOCK prefix functionality	7	7	☑ DISLOCK
IGNNE Port Emulation Enable	8	8	☑ IGNNE_EM
Enable Special Bus Cycle On Exit From HLT	12	12	☑ HLTXSPCYCEN
Special Bus Cycle On SMI Disable	13	13	☑ SMISPCYCDIS
Special Bus Cycle On RSM Disable	14	14	☑ RSMSPCYCDIS
SSE Instructions Disable	15	15	☑ SSEDIS
32-bit Address Wrap Disable	17	17	☑ WRAP32DIS
MCi Status Write Enable	18	18	☑ MCi_STATUS_WREN
Halt Power save Disable	19	19	☑ FRCTL_HALT_DIS
Startup FID Status	24	29	3F

OK Cancel

Status L2 Size Refresh Auto Refresh

Core 0 Refresh Wr Chgs Wr All

start AMD Hardware Debu... 4:47 PM

CONFIDENTIAL

2) APIC

HDT Features
- APIC Feature Group

CONFIDENTIAL

- IO APIC Locator
  - Search APIC device
  - A platform based feature
- IO APIC Registers
  - IO APIC Registers for a specific IO APIC device
  - A platform based feature
- Local APIC Registers
  - Access local APIC registers that are defined in a node/core

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
  - I/O APIC Locator
  - IO APIC Registers
  - Local APIC Registers
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1					

Refresh

Auto Refresh

CPU Registers 1 | I/O APIC Locator 1

I/O APIC Name	Base Address	Registers
Legacy I/O APIC	FEC00000	Show

Refresh

Script Console

Console | History

>

Pressing "Refresh" will search entire system for I/O APICs.
Pressing "Show" will bring up registers for the specified I/O APIC

start AMD Hardware Debu... 4:59 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
  - I/O APIC Locator
  - IO APIC Registers
  - Local APIC Registers
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1					

Refresh

Auto Refresh

CPU Registers 1 | I/O APIC Locator 1 | IO APIC Registers 1

Name	Address
Base Address	FEC00000

Header

Name	Value
I/O APIC ID [00]	
I/O APIC Version [01]	
I/O APIC ARB [02]	

Redirection Table

Name	Int Vec	Del Mode	Dest Mode	Del Status	Int Pin Pol	Rem Irr	Trig Mode	Int Mask	Dest Field

Refresh | Wr Chgs | Wr All

Script Console

Console | History

>

start | AMD Hardware Debu... | Microsoft PowerPoint ... | 5:00 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
  - I/O APIC Locator
  - IO APIC Registers
  - Local APIC Registers
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1					

Refresh

Auto Refresh

CPU Registers 1 | I/O APIC Locator 1 | IO APIC Registers 1

Name	Address
Base Address	FEC00000

Header

Name	Value
I/O APIC ID [00]	02000000
I/O APIC Version [01]	00170011
I/O APIC ARB [02]	02000000

Redirection Table

Name	Int Vec	Del Mode	Dest Mode	Del Status	Int Pin Pol	Rem Irr	Trig Mode	Int Mask	Dest Field
I/O APIC IRQ 000 [010]	FF	7	0	0	0	0	0	1	00
I/O APIC IRQ 001 [012]	93	1	1	0	0	0	0	0	00
I/O APIC IRQ 002 [014]	FF	0	0	0	0	0	0	1	00
I/O APIC IRQ 003 [016]	FF	0	0	0	0	0	0	1	00
I/O APIC IRQ 004 [018]	92	1	1	0	0	0	0	0	00
I/O APIC IRQ 005 [01A]	FF	0	0	0	0	0	0	1	00
I/O APIC IRQ 006 [01C]	B3	1	1	0	0	0	0	1	00
I/O APIC IRQ 007 [01E]	FF	0	0	0	0	0	0	1	00
I/O APIC IRQ 008 [020]	D1	0	1	0	0	0	0	0	00
I/O APIC IRQ 009 [022]	B1	1	1	0	1	1	1	0	00
I/O APIC IRQ 010 [024]	FF	0	0	0	0	0	0	1	00

Refresh | Wr Chgs | Wr All

Script Console

Console | History

Reminder! Always press "Refresh" to retrieve most current data.

start | AMD Hardware Debu... | Microsoft PowerPoint ... | 5:00 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
  - I/O APIC Locator
  - IO APIC Registers
  - Local APIC Registers
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1					

Refresh

Auto Refresh

CPU Registers 1 | I/O APIC Locator 1 | IO APIC Registers 1 | **Local APIC Registers 1**

Name	Value
APICBASE	00000000FEE00900
Local APIC ID [20]	00000000
Local APIC Version [30]	00040010
Task Priority [80]	00000041
Arbitrat. Priority [90]	000000D0
Processor Priority [A0]	00000041
EOI [B0]	
Remote Read [C0]	00000000
Logical Destinat. [D0]	01000000
Destination Format [E0]	FFFFFFFF
Spur-Interrupt Vec [F0]	011F
ISR 000-031 [100]	00000000
ISR 032-063 [110]	00000000
ISR 064-097 [120]	00000000
ISR 098-127 [130]	00000000
ISR 128-159 [140]	00000000
ISR 160-191 [150]	00000000
ISR 192-223 [160]	00000000
ISR 224-255 [170]	00000000
TMR 000-031 [180]	00000000
TMR 032-063 [190]	00000000

Node 0 | Core 0 | Refresh | Wr Chgs | Wr All

Script Console

Console | History

>

start | AMD Hardware Debu... | Microsoft PowerPoint ... | 5:01 PM

CONFIDENTIAL

3) BTHB Debuggers

HDT Features

- BTHB Debuggers Group

CONFIDENTIAL

- BTHB stands for Branch Trace History Buffer
  - Refer to BKDG for details
- BTHB Control feature
  - Setup BTHB debug settings
  - When resuming target program, the BTHB debug info will be stored in memory buffer the feature defines
- BTHB Data Viewer feature
  - Retrieve the BTHB buffer that existed in target. The displayed info can be filtered by various ways
  - Interpret the buffer data into BTHB trace entry info
  - See BKDG for definition detail
- BTHB Code Flow feature
  - According to BTHB trace entry info, and combining with other target info, retrieve target memory to recreate the code flow history
  - Multiple columns of code view display different info
  - Color coded special entries

AMD Hardware Debug Tool (AMD Internal Only)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
  - BTHB Code Flow
  - BTHB Control
  - BTHB Data View
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Te
- I/O Ports
- Instruction Cache Arr
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1	0	Legacy 32-bit Mode	BSP	DBReq	1024

Refresh

☑ Auto Refresh

BTHB Control 1

Trace Buffer Addresses	
BHTraceBase	0000000000000000
BHTracelimit	0000000000000000
BHTracePtr	0000000000000000

User Data	
BHTraceUsrD	

Trace Control	
BHTraceCTL	00000000
Message Goes to DRAM	☐ DRAM
Trace Enable	☐ TEN
Enable Full Trace Record	☐ TALL
Unconditional Branches Entered Into Bitmap	☐ TBIT
Enable Time Stamp	☐ TSP
Enable Debug Interrupt On Trace Buffer Overflow	☐ TINT
Memory Type Descriptor	0:UC-Uncacheable
Enable Privilege Level Specific Trace	Trace All Code
TRNG Field Privilege	Ring 0
Trace SMI Code	Trace All Code
Trace Operation Control	0:Start trace now, Don't stop (Continuous Mode)

Node 0 | Core 0 | Refresh | Wr Chgs | Wr All

start | AMD Hardware Debu... | Microsoft PowerPoint ... | 4:41 PM

AMD Hardware Debug Tool (AMD Internal Only)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
  - BTHB Code Flow
  - BTHB Control
  - BTHB Data View
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Te
- I/O Ports
- Instruction Cache Arr
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1	0	Legacy 32-bit Mode	BSP	DBReq	1024

Refresh

☑ Auto Refresh

BTHB Control 1

Trace Buffer Addresses	
BHTraceBase	0000000000000000
BHTracelimit	0000000000000000
BHTracePtr	0000000000000000

User Data	
BHTraceUsrD	

Trace Control	
BHTraceCTL	00000000
Message Goes to DRAM	☐ DRAM
Trace Enable	☐ TEN
Enable Full Trace Record	☐ TALL
Unconditional Branches Entered Into Bitmap	☐ TBIT
Enable Time Stamp	☐ TSP
Enable Debug Interrupt On Trace Buffer Overflow	☐ TINT
Memory Type Descriptor	0:UC-Uncacheable
Enable Privilege Level Specific Trace	Trace All Code
TRNG Field Privilege	
Trace SMI	
Trace Operation Control	Don't stop (Continuous Mode)

Setup For CodeFlow
Load...
Save As...
Properties

An easy way to setup for collecting traces was already defined.

Node 0 | Core 0 | Refresh | Wr Chgs | Wr All

start | AMD Hardware Debu... | Microsoft PowerPoint ... | 4:44 PM

AMD Hardware Debug Tool (AMD Internal Only)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
  - BTHB Code Flow
  - BTHB Control
  - BTHB Data View
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Te
- I/O Ports
- Instruction Cache Arr
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1	0	Legacy 32-bit Mode	BSP	DBReq	1024

Refresh

☑ Auto Refresh

BTHB Control 1

Trace Buffer Addresses	
BHTraceBase	00000000000A0000
BHTracelimit	00000000000A7FFF
BHTracePtr	0000000000000000

User Data	
BHTraceUsrD	

Trace Control	
BHTraceCTL	00010340
Message Goes to DRAM	☑ DRAM
Trace Enable	☑ TEN
Enable Full Trace Record	☐ TALL
Unconditional Branches Entered Into Bitmap	☐ TBI
Enable Time Stamp	☐
Enable Debug Interrupt On Trace Buffer Overflow	☐ TINT
Memory Type Descriptor	6:WB-Writeback
Enable Privilege Level Specific Trace	Trace All Code
TRNG Field Privilege	Ring 0
Trace SMI Code	Trace All Code
Trace Operation Control	0:Start trace now, Don't stop (Continuous Mode)

Reminder: Press "Wr All" or "Wr Chgs" to submit changes

Node 0 | Core 0 | Refresh | Wr Chgs | Wr All

start | AMD Hardware Debu... | 1:29 PM

AMD Hardware Debug Tool (AMD Internal Only)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
  - BTHB Code Flow
  - BTHB Control
  - BTHB Data View
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Te
- I/O Ports
- Instruction Cache Arr
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1	0	Legacy 32-bit Mode	BSP	DBReq	1024

Refresh

☑ Auto Refresh

BTHB Control 1

Trace Buffer Addresses	
BHTraceBase	00000000000A0000
BHTracelimit	00000000000A7FF7
BHTracePtr	0000000000000000

User Data	
BHTraceUsrD	

Trace Control	
BHTraceCTL	00010340
Message Goes to DRAM	☑ DRAM
Trace Enable	☑ TEN
Enable Full Trace Record	☐ TALL
Unconditional Branches Entered Into Bitmap	☐ TBIT
Enable Time Stamp	☐ TSP
Enable Debug Interrupt On Trace Buffer Overflow	☐ TINT
Memory Type Descriptor	6:WB-Writeback
Enable Privilege Level Specific Trace	Trace All Code
TRNG Field Privilege	Ring 0
Trace SMI Code	Trace All Code
Trace Operation Control	0:Start trace now, Don't stop (Continuous Mode)

Node 0 | Core 0 | Refresh | Wr Chgs | Wr All

start | AMD Hardware Debu... | 1:30 PM

AMD Hardware Debug Tool (AMD Internal Only)

File Edit View Features HDT Windows Help

Resume operation at current state

Exit HDT to allow system to run and buffer to be filled.

Feature Explorer

- APIC
- BTHB Debuggers
  - BTHB Code Flow
  - BTHB Control
  - BTHB Data View
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- Download Tools
- HyperTransport™ Te
- I/O Ports
- Instruction Cache Arr
- JTAG Instructions
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- Memory Debuggers
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq				
0	SH_B0/2-claw-754	0	0	1	0	

Auto Refresh

BTHB Control 1

Trace Buffer Addresses	
BHTraceBase	00000000000A0000
BHTracelimit	00000000000A7FF7
BHTracePtr	0000000000000000

User Data	
BHTraceUsrD	

Trace Control	
BHTraceCTL	00010340
Message Goes to DRAM	☑ DRAM
Trace Enable	☑ TEN
Enable Full Trace Record	☐ TALL
Unconditional Branches Entered Into Bitmap	☐ TBIT
Enable Time Stamp	☐ TSP
Enable Debug Interrupt On Trace Buffer Overflow	☐ TINT
Memory Type Descriptor	6:WB-Writeback
Enable Privilege Level Specific Trace	Trace All Code
TRNG Field Privilege	Ring 0
Trace SMI Code	Trace All Code
Trace Operation Control	0:Start trace now, Don't stop (Continuous Mode)

Node 0 | Core 0 | Refresh | Wr Chgs | Wr All

start | AMD Hardware Debu... | 1:30 PM

AMD Hardware Debug Tool (AMD Internal Only)

File Edit View Features HDT Windows Help

Enter HDT debug mode

Enter "HDT Mode" to view/analyze buffered data.

Feature Explorer

- APIC
- BTHB Debuggers
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  - BTHB Data View
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- HyperTransport™ Te
- I/O Ports
- Instruction Cache Arr
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core							
0	SH_B0/2-claw-754	0	0	0	n/a	n/a	n/a	n/a	n/a	Auto Refresh

BTHB Control 1

Trace Buffer Addresses	
BHTraceBase	00000000000A0000
BHTracelimit	00000000000A7FF7
BHTracePtr	0000000000000000

User Data	
BHTraceUsrD	

Trace Control	
BHTraceCTL	00010340
Message Goes to DRAM	☑ DRAM
Trace Enable	☑ TEN
Enable Full Trace Record	☐ TALL
Unconditional Branches Entered Into Bitmap	☐ TBIT
Enable Time Stamp	☐ TSP
Enable Debug Interrupt On Trace Buffer Overflow	☐ TINT
Memory Type Descriptor	6:WB-Writeback
Enable Privilege Level Specific Trace	Trace All Code
TRNG Field Privilege	Ring 0
Trace SMI Code	Trace All Code
Trace Operation Control	0:Start trace now, Don't stop (Continuous Mode)

Node 0 | Core 0 | Refresh | Wr Chgs | Wr All

start | AMD Hardware Debu... | 1:30 PM

AMD Hardware Debug Tool (AMD Internal Only)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
  - BTHB Code Flow
  - BTHB Control
  - BTHB Data View
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- Download Tools
- HyperTransport™ Te
- I/O Ports
- Instruction Cache Arr
- JTAG Instructions
- L2 Cache Arrays
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- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1	0	Legacy 32-bit Mode	BSP	DBReq	1024

Refresh

☑ Auto Refresh

BTHB Control 1

Trace Buffer Addresses	
BHTraceBase	00000000000A0000
BHTracelimit	00000000000A7FF7
BHTracePtr	000000000000333C

User Data	
BHTraceUsrD	

Trace Control	
BHTraceCTL	00010340
Message Goes to DRAM	☑ DRAM
Trace Enable	☑ TEN
Enable Full Trace Record	☐ TALL
Unconditional Branches Entered Into Bitmap	☐ T
Enable Time Stamp	☐ TS
Enable Debug Interrupt On Trace Buffer Overflow	☐ TINT
Memory Type Descriptor	6:WB-Writeback
Enable Privilege Level Specific Trace	Trace All Code
TRNG Field Privilege	Ring 0
Trace SMI Code	Trace All Code
Trace Operation Control	0:Start trace now, Don't stop (Continuous Mode)

Press "Refresh" to see "BHTracePtr" has incremented, signifying that data was buffered.

Node 0 | Core 0 | Refresh | Wr Chgs | Wr All

start | AMD Hardware Debu... | 1:31 PM

AMD Hardware Debug Tool (AMD Internal Only)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
  - BTHB Code Flow
  - BTHB Control
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- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1	0	Legacy 32-bit Mode	BSP	DBReq	1024

Refresh

Auto Refresh

BTHB Control 1 | BTHB Data Viewer 1

Offset	95:92	91	90	89	88	87	86	85	84	83	82:80	79:64	63:00	Comments
	Tag	PG	PE	D	Interrupt Vector							Selector	Logical Address	
					VM	SM	SU	L	LMA	REX	Not Used			

When viewing buffered data, user can select a specified range and also filter what data to analyze.

Start Address	Start Address Type
0000000000000000	User Defined
Stop Address	User Defined
0000000000000000	Trace Buffer Base
	Trace Buffer Offset
	Trace Buffer Limit

Filters

0 Trace Start
1 Conditional Branch Bitmap
2 JMP, CALL, RET, SYSCALL, or SYSRET
3 Instruction Breakpoint, Exceptions
4 INTR, NMI, INT, INTO, BOUND, or INT3
5 IRET

Selector=

Apply Filter

Remove Filter

Node 0 | Core 0 | Refresh

start | AMD Hardware Debu... | 1:31 PM

AMD Hardware Debug Tool (AMD Internal Only)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
  - BTHB Code Flow
  - BTHB Control
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- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1	0	Legacy 32-bit Mode	BSP	DBReq	1024

Refresh

☑ Auto Refresh

BTHB Control 1 | **BTHB Data Viewer 1**

Offset	95:92	91	90	89	88	87	86	85	84	83	82:80	79:64	63:00	Comments
	Tag	PG	PE	D	Interrupt Vector							Selector	Logical Address	
					VM	SM	SU	L	LMA	REX	Not Used			

Start Address	Start Address Type
00000000000A0000	Trace Buffer Base
Stop Address	**Stop Address Type**
100	Number of Entries (+

Filters

0 Trace Start
1 Conditional Branch Bitmap
2 JMP, CALL, RET, SYSCALL, or SYSRET
3 Instruction Breakpoint, Exceptions
4 INTR, NMI, INT, INTO, BOUND, or INT3
5 IRET

Selector=

Apply Filter

Remove Filter

Node 0 | Core 0 | Refresh

start | AMD Hardware Debu... | 1:31 PM

AMD Hardware Debug Tool (AMD Internal Only)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
  - BTHB Code Flow
  - BTHB Control
  - BTHB Data View
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Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1	0	Legacy 32-bit Mode	BSP	DBReq	1024

Refresh

Auto Refresh

BTHB Control 1 | **BTHB Data Viewer 1**

Offset	95:92	91	90	89	88	87	86	85	84	83	82:80	79:64	63:00	Commer
	Tag	PG	PE	D	Interrupt Vector							Selector	Logical Address	
					VM	SM	SU	L	LMA	REX	Not Used			
0000000000000000	1	1	1	1	0	0	0	0	0	0			0000000080000000	Conditional Bra
000000000000000C	2	1	1	1	0	0	0	0	0	0		0008	00000000F74E3C66	JMP, CALL, RET, SYS
0000000000000018	1	1	1	1	0	0	0	0	0	0			0000000080000000	Conditional Bra
0000000000000024	2	1	1	1	0	0	0	0	0	0		0008	00000000F750186A	JMP, CALL, RET, SYS
0000000000000030	1	1	1	1	0	0	0	0	0	0			0000000070000000	Conditional Bra
000000000000003C	2	1	1	1	0	0	0	0	0	0		0008	00000000F750601F	JMP, CALL, RET, SYS
0000000000000048	1	1	1	1	0	0	0	0	0	0			0000000070000000	Conditional Bra
0000000000000054	2	1	1	1	0	0	0	0	0	0		0008	000000008051AF0C	JMP, CALL, RET, SYS
0000000000000060	1	1	1	1	0	0	0	0	0	0			0000000080000000	Conditional Bra
000000000000006C	2	1	1	1	0	0	0	0	0	0		0008	00000000F74E3C8D	JMP, CALL, RET, SYS
0000000000000078	1	1	1	1	0	0	0	0	0	0			0000000080000000	Conditional Bra
0000000000000084	2	1	1	1	0	0	0	0	0	0		0008	00000000F7506051	JMP, CALL, RET, SYS
0000000000000090	1	1	1	1	0	0	0	0	0	0			000000002F800000	Conditional Bra
000000000000009C	2	1	1	1	0	0	0	0	0	0		0008	00000000F750609F	JMP, CALL, RET, SYS
00000000000000A8	1	1	1	1	0	0	0	0	0	0			00000000A0000000	Conditional Bra
00000000000000B4	2	1	1	1	0	0	0	0	0	0		0008	000000008051AF6C	JMP, CALL, RET, SYS
00000000000000C0	1	1	1	1	0	0	0	0	0	0			0000000080000000	Conditional Bra
00000000000000CC	2	1	1	1	0	0	0	0	0	0		0008	00000000F74E3C44	JMP, CALL, RET, SYS
00000000000000D8	1	1	1	1	0	0	0	0	0	0			0000000080000000	Conditional Bra
00000000000000E4	2	1	1	1	0	0	0	0	0	0		0008	00000000F75060E2	JMP, CALL, RET, SYS

Start Address	Start Address Type
000000000000A0000	Trace Buffer Base
Stop Address	**Stop Address Type**
0000000000000100	Number of Entries (+

Filters

0 Trace Start
1 Conditional Branch Bitmap
2 JMP, CALL, RET, SYSCALL, or SYSRET
3 Instruction Breakpoint, Exceptions
4 INTR, NMI, INT, INTO, BOUND, or INT3
5 IRET

Selector=

Apply Filter

Remove Filter

Node 0 | Core 0 | Refresh

start | AMD Hardware Debu... | 1:32 PM

AMD Hardware Debug Tool (AMD Internal Only)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
  - BTHB Code Flow
  - BTHB Control
  - BTHB Data View
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Te
- I/O Ports
- Instruction Cache Arr
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1	0	Legacy 32-bit Mode	BSP	DBReq	1024

Refresh

Auto Refresh

BTHB Control 1 | BTHB Data Viewer 1 | **BTHB Code Flow 1**

Start Address	Start Address Type
0000000000000000	User Defined

Stop Address: 0000000000000000

User Defined
Trace Buffer Base
Trace Buffer Offset
Trace Buffer Limit

GDTR	000000008003F000	Target
LDTR	0000000000000000	Target
CR3	0000000000039000	Target

- Instruction Breakpoint, Exceptions
- INTR, NMI, INT, INTO, BOUND, or INT3
- System Management Interrupt
- Data Breakpoints
- Start Another Trace Process
- Conditional Branch Taken

Address	Opcodes	Mnemonic	Code	Size	BTHB Buffer Offset	Loc

CodeFlow is a more user-friendly view that interprets that buffered data into a code execution format.

Node 0 | Core 0 | Refresh

start | AMD Hardware Debu... | 1:32 PM

AMD Hardware Debug Tool (AMD Internal Only)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
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Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1	0	Legacy 32-bit Mode	BSP	DBReq	1024

Refresh

Auto Refresh

BTHB Control 1 | BTHB Data Viewer 1 | **BTHB Code Flow 1**

Start Address	Start Address Type			
00000000000A0000	Trace Buffer Base	GDTR	000000008003F000	Target
Stop Address	Stop Address Type	LDTR	0000000000000000	Target
0000000000000		CR3	[illegible]	Target

- Instruction Breakpoint, Exceptions
- INTR, NMI, INT, INTO, BOUND, or INT3
- System Management Interrupt
- Breakpoints
- Another Trace Process
- onditional Branch Taken

Addres	Size	BTHB Buffer Offset	Loc

Generating code flow instructions

Current Progress

76%

Overall Progress

46%

Status: Processing...

Estimated Remaining Time: 0 minutes 1 seconds

Cancel

Node 0 | Core 0 | Refresh

start | AMD Hardware Debu... | 1:33 PM

AMD Hardware Debug Tool (AMD Internal Only)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
  - BTHB Code Flow
  - BTHB Control
  - BTHB Data View
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- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1	0	Legacy 32-bit Mode	BSP	DBReq	1024

Refresh

Auto Refresh

BTHB Control 1 | BTHB Data Viewer 1 | **BTHB Code Flow 1**

Start Address	Start Address Type
00000000000A0000	Trace Buffer Base
Stop Address	**Stop Address Type**
0000000000000100	Number of Entries (+

GDTR	000000008003F000	Target
LDTR	0000000000000000	Target
CR3	0000000000039000	Target

- Instruction Breakpoint, Exceptions
- INTR, NMI, INT, INTO, BOUND, or INT3
- System Management Interrupt
- Data Breakpoints
- Start Another Trace Process
- Conditional Branch Taken

Address	Opcodes	Mnemonic	Code	Size	BTHB Buffer Offset
0008:00000000F74E3C66	C2 08 00	retnd	0008h	32	0000000000000024
0008:00000000F750186A	43	inc	ebx	32	
0008:00000000F750186B	83 C7 3C	add	edi,3ch	32	
0008:00000000F750186E	83 FB 02	cmp	ebx,02h	32	
0008:00000000F7501871	72 CE	jb	loc f7501841h	32	0000000000000030
0008:00000000F7501841	6A 01	push	byte 01h	32	
0008:00000000F7501843	8B CB	mov	ecx,ebx	32	
0008:00000000F7501845	58	pop	eax	32	
0008:00000000F7501846	D3 E0	shl	eax,cl	32	
0008:00000000F7501848	8B 4D FC	mov	ecx,[ebp-04h]	32	
0008:00000000F750184B	85 C1	test	ecx,eax	32	
0008:00000000F750184D	74 1B	jz	loc f750186ah	32	0000000000000030
0008:00000000F750186A	43	inc	ebx	32	
0008:00000000F750186B	83 C7 3C	add	edi,3ch	32	
0008:00000000F750186E	83 FB 02	cmp	ebx,02h	32	
0008:00000000F7501871	72 CE	jb	loc f7501841h	32	0000000000000030
0008:00000000F7501873	5F	pop	edi	32	
0008:00000000F7501874	5E	pop	esi	32	
0008:00000000F7501875	33 C0	xor	eax,eax	32	

Node 0 | Core 0 | Refresh

start | AMD Hardware Debu... | 1:35 PM

CONFIDENTIAL

4) Cache Arrays

HDT Features

- Cache Array Groups

CONFIDENTIAL

- Cache debug features
  - These features can be used to debug target cache arrays. All cache features are core based
  - Refer to BKDG for cache array definition
- Instruction Cache Arrays
  - Feature definition varies with target processor family and rev
  - Report target ICache of L1 cache
- Data Cache Arrays
  - Feature definition varies with target processor family and rev
  - Report target DCache of L1 cache
- L2 Cache Arrays
  - Feature definition varies with target processor family/rev, and target processor L2 cache size
  - Report target L2 cache

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
  - DCache Data Array
  - DCache Data Array (Detailed)
  - DCache L1 TLB A Array
  - DCache L1 TLB B Array
  - DCache L2 TLB Array
  - DCache Line Translator
  - DCache LRU Array
  - DCache Tag A Array
  - DCache Tag B Array
  - DCache Tag C Array
- Debug Utilities
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1					

Refresh

Auto Refresh

DCache Data Array 1

WAY	Index	Bytes 63:56	Bytes 55:48	Bytes 47:40	Bytes 39:32	Bytes 31:24
0	000	F000EF6FF000EF57	F000EF6FF000EF6F	F000EF6FF000EF6F	F000E987F000FEA5	F000E816F0007D38
0	001	0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000
0	002	0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000
0	003	0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000
0	004	0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000
1	000	FFFFFFFFFFFFFFFF	FFFFFFFFFFFFFFFF	FFFFFFFFFFFFFFFF	FFFFFFFFFFFFFFFF	FFFFFFFFFFFFFFFF
1	001	C000178AF000EFC7	F000F0A4F000FF53	F000FF53F000FE6E	F000E6F2F000E7A4	F000EFD2F000E82E
1	002	0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000
1	003	0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000
1	004	F000E816F000E816	F000E816F000E816	F000E816F000E816	F000E816F000E816	F000E816F000E816

Start Index: 0 Number of Indexes: 005

Way	0	1
Clear All	☑	☑

Node 0 Core 0 Refresh Wr Chgs Wr All

start AMD Hardware Debu... 3:38 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
  - DCache Data Array
  - DCache Data Array (Detailed)
  - DCache L1 TLB A Array
  - DCache L1 TLB B Array
  - DCache L2 TLB Array
  - DCache Line Translator
  - DCache LRU Array
  - DCache Tag A Array
  - DCache Tag B Array
  - DCache Tag C Array
- Debug Utilities
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- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1					

Refresh

Auto Refresh

DCache Data Array 1

WAY	Index	Bytes 63:56	Bytes 55:48	Bytes 47:40	Bytes 39:32	Bytes 31:24
0	000	F000EF6FF000EF57	F000EF6FF000EF6F	F000EF6FF000EF6F	F000E987F000FEA5	F000E816F0007D38
0	001	0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000
0	002	0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000
0	003	0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000
0	004	0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000

Start Index: 0 Number of Indexes: 005

Way	0	1
Clear All	☑	☐

Node 0 Core 0 Refresh Wr Chgs Wr All

start AMD Hardware Debu... 3:38 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
  - DCache Data Array
  - DCache Data Array (Detailed)
  - DCache L1 TLB A Array
  - DCache L1 TLB B Array
  - DCache L2 TLB Array
  - DCache Line Translator
  - DCache LRU Array
  - DCache Tag A Array
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Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1					

Refresh

Auto Refresh

DCache Data Array 1 | DCache Data Array (Detailed) 1

WAY	Index	Bank	SP	Data	P	EDD
0	000	0	0	F000E816F000E816	0	8D
0	000	1	0	F000E816F000E2C3	0	4C
0	000	2	0	F000FF54F000E816	0	96
0	000	3	0	F000E816F0007D38	0	82
0	000	4	0	F000E987F000FEA5	0	95
0	000	5	0	F000EF6FF000EF6F	0	8D
0	000	6	0	F000EF6FF000EF6F	0	8D
0	000	7	0	F000EF6FF000EF57	0	57
0	001	0	0	0000000000000000	0	0C
0	001	1	0	0000000000000000	0	0C
0	001	2	0	0000000000000000	0	0C
0	001	3	0	0000000000000000	0	0C
0	001	4	0	0000000000000000	0	0C
0	001	5	0	0000000000000000	0	0C
0	001	6	0	0000000000000000	0	0C
0	001	7	0	0000000000000000	0	0C
0	002	0	0	0000000000000000	0	0C
0	002	1	0	0000000000000000	0	0C
0	002	2	0	0000000000000000	0	0C
0	002	3	0	0000000000000000	0	0C
0	002	4	0	0000000000000000	0	0C
0	002	5	0	0000000000000000	0	0C
0	002	6	0	0000000000000000	0	0C
0	002	7	0	0000000000000000	0	0C
0	003	0	0	0000000000000000	0	0C

Start Index: 0 Number of Indexes: 005

Way	0	1
Clear All	☑	☐

Node 0 | Core 0 | Refresh | Wr Chgs | Wr All

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AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
  - DCache Data Array
  - DCache Data Array (Detailed)
  - DCache L1 TLB A Array
  - DCache L1 TLB B Array
  - DCache L2 TLB Array
  - DCache Line Translator
  - DCache LRU Array
  - DCache Tag A Array
  - DCache Tag B Array
  - DCache Tag C Array
- Debug Utilities
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- HyperTransport™ Technology
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- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1					

Refresh

Auto Refresh

DCache Data Array 1 | DCache Data Array (Detailed) 1 | **DCache L1 TLB A Array 1**

Index	SP	V	G	DGR	TPL	LinearTag	Cr3Tag	Wr	U	D	MT	RD	WD	TPH	PhysTag	Misc	EntryID
00	0	0	0	0	1	0000000F0	00	0	0	0	0	0	0	0	0000000	08	00
01	0	0	0	1	1	0000000AE	00	1	1	1	0	1	1	0	00000AE	08	01
02	0	0	0	1	1	0000000AE	00	1	1	1	0	1	1	0	00000AE	08	02
03	0	0	0	1	1	0000000AE	00	1	1	1	0	1	1	0	00000AE	08	03
04	0	0	0	1	0	0000000F5	00	1	1	1	0	1	0	0	00000F5	00	04

Start Index: 0 Number of Indexes: 05

Node 0 Core 0 Refresh Wr Chgs Wr All

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AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
  - DCache Data Array
  - DCache Data Array (Detailed)
  - DCache L1 TLB A Array
  - DCache L1 TLB B Array
  - DCache L2 TLB Array
  - DCache Line Translator
  - DCache LRU Array
  - DCache Tag A Array
  - DCache Tag B Array
  - DCache Tag C Array
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- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
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- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1					

Refresh

Auto Refresh

DCache Data Array 1 | DCache Data Array (Detailed) 1 | DCache L1 TLB A Array 1 | DCache Line Translator 1 | **DCache LRU Array 1**

Index	LRU
00	01
01	01
02	01
03	01
04	01
05	01
06	01
07	01
08	01
09	01
0A	01
0B	01
0C	01
0D	01
0E	01
0F	01

Start Index: 0 Number of Indexes: 10

Node 0 Core 0 Refresh Wr Chgs Wr All

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AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
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  - DCache L1 TLB A Array
  - DCache L1 TLB B Array
  - DCache L2 TLB Array
  - DCache Line Translator
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  - DCache Tag C Array
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Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1					

Refresh

Auto Refresh

DCache Data Array (Detailed) 1 | DCache L1 TLB A Array 1 | DCache Line Translator 1 | DCache LRU Array 1 | **DCache Tag A Array 1**

WAY	Index	SP	WB	SMC	V	Wr	SP0	SP1	P	Tag
0	000	0	1	0	1	1	1	0	0	0000000
0	001	0	1	0	1	1	1	0	1	0000010
0	002	0	1	0	1	1	1	0	1	0000008
0	003	0	1	0	1	1	1	0	1	0000008
0	004	0	1	0	1	1	1	0	1	0000010
1	000	0	0	0	1	1	0	0	1	00000E0
1	001	0	1	0	1	1	1	0	0	0000000
1	002	0	1	0	1	1	1	0	1	0000010
1	003	0	1	0	1	1	1	0	1	0000010
1	004	0	1	1	1	0	0	1	0	0000000

Start Index: 0 Number of Indexes: 005

Way	0	1
Clear All	☑	☑

Node 0 Core 0 Refresh Wr Chgs Wr All

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AMD Hardware Debug Tool (AMD Confidential)

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- APIC
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- Instruction Cache Arrays
  - ICache Bimodal Counter Array
  - ICache Branch Selector Array
  - ICache Branch Target Array
  - ICache Data Array
  - ICache Data Array (Detailed)
  - ICache L1 TLB Array
  - ICache L2 TLB Array
  - ICache Line Translator
  - ICache LRU Array
  - ICache Predecode Array
  - ICache Tag A Array
  - ICache Tag C Array
- JTAG Instructions
- L2 Cache Arrays
  - L2Cache Data Array
  - L2Cache Data Array (Detailed)
  - L2Cache ECC Scrub Register
  - L2Cache Line Translator
  - L2Cache Tag Array
- Memory Debuggers
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1					

Refresh

Auto Refresh

a Array 1 | L2Cache Data Array (Detailed) 2 | L2Cache ECC Scrub Register 1 | L2Cache Tag Array 1 | **ICache Bimodal Counter Array 1**

Index	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	C11	C12	C13	C14	C15
000	2	2	1	1	1	2	2	2	1	3	2	1	2	2	2	2
001	2	2	1	1	1	2	2	2	1	3	2	1	2	2	2	2
002	2	2	1	1	1	2	2	2	1	3	2	1	2	2	2	2
003	2	2	1	1	1	2	2	2	1	3	2	1	2	2	2	2
004	0	2	2	1	2	2	3	0	0	2	2	2	2	2	2	3
005	0	2	2	1	2	2	3	0	0	2	2	2	2	2	2	3
006	0	2	2	1	2	2	3	0	0	2	2	2	2	2	2	3
007	0	2	2	1	2	2	3	0	0	2	2	2	2	2	2	3
008	2	2	2	2	3	2	2	2	0	2	2	2	0	2	2	2
009	2	2	2	2	3	2	2	2	0	2	2	2	0	2	2	2
00A	2	2	2	2	3	2	2	2	0	2	2	2	0	2	2	2
00B	2	2	2	2	3	2	2	2	0	2	2	2	0	2	2	2
00C	2	2	2	0	3	2	2	2	2	3	0	2	2	2	2	2
00D	2	2	2	0	3	2	2	2	2	3	0	2	2	2	2	2
00E	2	2	2	0	3	2	2	2	2	3	0	2	2	2	2	2
00F	2	2	2	0	3	2	2	2	2	3	0	2	2	2	2	2

Start Index: 0 Number of Indexes: 010

Node 0 Core 0 Refresh Wr Chgs Wr All

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AMD Hardware Debug Tool (AMD Confidential)

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Feature Explorer

- APIC
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- HyperTransport™ Technology
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- Instruction Cache Arrays
  - ICache Bimodal Counter Array
  - ICache Branch Selector Array
  - ICache Branch Target Array
  - ICache Data Array
  - ICache Data Array (Detailed)
  - ICache L1 TLB Array
  - ICache L2 TLB Array
  - ICache Line Translator
  - ICache LRU Array
  - ICache Predecode Array
  - ICache Tag A Array
  - ICache Tag C Array
- JTAG Instructions
- L2 Cache Arrays
  - L2Cache Data Array
  - L2Cache Data Array (Detailed)
  - L2Cache ECC Scrub Register
  - L2Cache Line Translator
  - L2Cache Tag Array
- Memory Debuggers
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1					

Refresh

Auto Refresh

etailed) 2 | L2Cache ECC Scrub Register 1 | L2Cache Tag Array 1 | ICache Bimodal Counter Array 1 | **ICache Branch Selector Array 1**

WAY	Index	SP	M0	M1	M2	M3	M4	M5	M6	M7	M8	D1	D2	D3	B1Info	B1A	B2Info	B2A	B3Info	B3A
0	000	0	1	0	0	0	0	0	0	0	0	0	0	0	8	0	0	0	0	0
0	001	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0
0	002	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	003	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	004	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	005	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	006	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	007	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	008	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	009	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	00A	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	00B	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	00C	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	00D	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	00E	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	00F	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	001	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	002	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	003	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	004	0	1	0	0	0	0	0	0	1	0	0	0	0	8	0	8	1	0	0
1	005	0	0	0	0	0	0	1	0	0	0	0	0	0	D	0	D	0	D	0
1	006	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	007	0	0	0	1	0	0	0	1	0	0	0	0	0	A	0	E	0	A	0
1	008	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Start Index: 0 Number of Indexes: 010

Way	0	1
Clear All	☑	☑

Node 0 | Core 0 | Refresh | Wr Chgs | Wr All

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AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
  - L2Cache Data Array
  - L2Cache Data Array (Detailed)
  - L2Cache ECC Scrub Register
  - L2Cache Line Translator
  - L2Cache Tag Array
- Memory Debuggers
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1					

Refresh

Auto Refresh

L2Cache Data Array 1

WAY	Index	Bytes 63:56	Bytes 55:48	Bytes 47:40	Bytes 39:32	Bytes 31:24
0	000	0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000
0	001	0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000
1	000	0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000
1	001	0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000
2	000	0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000
2	001	C000178AF000EFC7	F000F0A4F000FF53	F000FF53F000FE6E	F000E6F2F000E7A4	F000EFD2F000E82E
3	000	0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000
3	001	0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000
4	000	0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000
4	001	0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000
5	000	FFFFFFFFFFFFFFFF	FFFFFFFFFFFFFFFF	FFFFFFFFFFFFFFFF	FFFFFFFFFFFFFFFF	FFFFFFFFFFFFFFFF
5	001	0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000
6	000	0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000
6	001	0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000
7	000	FFFFFFFFFFFFFFFF	FFFFFFFFFFFFFFFF	FFFFFFFFFFFFFFFF	FFFFFFFFFFFFFFFF	FFFFFFFFFFFFFFFF
7	001	0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000
8	000	0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000
8	001	0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000
9	000	FFFFFFFFFFFFFFFF	FFFFFFFFFFFFFFFF	FFFFFFFFFFFFFFFF	FFFFFFFFFFFFFFFF	FFFFFFFFFFFFFFFF
9	001	0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000
A	000	0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000
A	001	0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000
B	000	FFFFFFFFFFFFFFFF	FFFFFFFFFFFFFFFF	FFFFFFFFFFFFFFFF	FFFFFFFFFFFFFFFF	FFFFFFFFFFFFFFFF
B	001	0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000

Start Index: 0 Number of Indexes: 002

Way	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Clear All	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔

Node 0 Core 0 Refresh Wr Chgs Wr All

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5) Data, Instruction, and L2 Cache Line Translator

HDT Features

- Cache Line Translators

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- Display multiple cache array data corresponding to a DRAM address
  - DRAM address can be defined by Physical, Linear, Logical or Indexed format.
  - Automatically translate the address into cache way and index to retrieve multi cache array info for the input definition.
- Cache Line Translator features
  - ICache Line Translator
  - DCache Line Translator
  - L2Cache Line Translator

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
  - DCache Data Array
  - DCache Data Array (Detailed)
  - DCache L1 TLB A Array
  - DCache L1 TLB B Array
  - DCache L2 TLB Array
  - DCache Line Translator
  - DCache LRU Array
  - DCache Tag A Array
  - DCache Tag B Array
  - DCache Tag C Array
- Debug Utilities
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1					

Refresh

Auto Refresh

DCache Data Array 1 | DCache Data Array (Detailed) 1 | DCache L1 TLB A Array 1 | **DCache Line Translator 1**

Address F000:0000000000000ED82 **Addr Type** Index

Segment CS Sel **Offset** rIP + 0000000000000000

00000000000FED82 (Linear) = 0000000000FED82 (Physical)

DCache Tag A Array

WAY	Index	SP	WB	SMC	V	Wr	SP0	SP1	P	Tag
0	1B6	0	1	0	1	1	1	0	0	0000006
1	1B6	0	1	0	1	1	1	0	1	000000E

DCache Tag C Array

WAY	Index	SP	S	D	V	WB	L2	SP0	SP1	P	Tag
0	1B6	0	0	1	1	1		1	0	0	0000006
1	1B6	0	0	1	1	1		1	0	1	000000E

DCache Data Array

WAY	Index	Bytes 63:56	Bytes 55:48	Bytes 47:40	Bytes 39:32	Bytes 31:24
0	1B6	0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000
1	1B6	0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000

DCache L1 TLB A Array

Index	SP	V	G	DGR	TPL	LinearTag	Cr3Tag	Wr	U	D	MT	RD	WD	TPH	PhysTag	Misc	EntryID
00	0	0	0	0	1	0000000F0	00	0	0	0	0	0	0	0	0000000	08	00
01	0	0	0	1	1	0000000AE	00	1	1	1	0	1	1	0	00000AE	08	01
02	0	0	0	1	1	0000000AE	00	1	1	1	0	1	1	0	00000AE	08	02
03	0	0	0	1	1	0000000AE	00	1	1	1	0	1	1	0	00000AE	08	03
04	0	0	0	1	0	0000000F5	00	1	1	1	0	1	0	0	00000F5	00	04
05	0	0	0	1	0	0000000AF	00	1	1	1	0	1	1	1	00000AF	08	05
06	0	0	0	1	0	000000000	00	1	1	1	6	1	1	1	0000000	09	06
07	0	0	0	1	1	0000000FE	00	1	1	1	0	1	0	1	00000FE	00	07
08	0	0	0	1	0	0000000AF	00	1	1	1	0	1	1	1	00000AF	08	08
09	0	0	0	1	1	0000000AE	00	1	1	1	0	1	1	0	00000AE	08	09
0A	0	0	0	1	1	0000000FD	00	1	1	1	0	1	0	1	00000FD	00	0A
0B	0	0	0	1	1	0000000AE	00	1	1	1	0	1	1	0	00000AE	08	0B
0C	0	0	0	1	1	0000000AE	00	1	1	1	0	1	1	0	00000AE	08	0C

Node 0 | Core 0 | Refresh | Wr Chgs | Wr All

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AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
  - ICache Bimodal Counter Array
  - ICache Branch Selector Array
  - ICache Branch Target Array
  - ICache Data Array
  - ICache Data Array (Detailed)
  - ICache L1 TLB Array
  - ICache L2 TLB Array
  - ICache Line Translator
  - ICache LRU Array
  - ICache Predecode Array
  - ICache Tag A Array
  - ICache Tag C Array
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1					

Refresh

Auto Refresh

ICache Line Translator 2

Address F000:0000000000000ED82 Addr Type Index

Segment CS Sel Offset rIP + 0000000000000000

00000000000FED82 (Linear) = 00000000000FED82 (Physical)

ICache Tag A Array

WAY	Index	SP	State	V	VP	StP	TP	Tag
0	1B6	0	3	0	1	0	1	FFFFFFF
1	1B6	0	3	0	1	0	1	FFFFFFF

ICache Tag C Array

WAY	Index	SP	State	V	VP	StP	TP	Tag
0	1B6	0	3	0	1	0	1	FFFFFFF
1	1B6	0	3	0	1	0	1	FFFFFFF

ICache Data Array

WAY	Index	Bytes 63:56	Bytes 55:48	Bytes 47:40	Bytes 39:32	Bytes 31:24
0	1B6	FFFFFFFFFFFFFFFF	FFFFFFFFFFFFFFFF	FFFFFFFFFFFFFFFF	FFFFFFFFFFFFFFFF	FFFFFFFFFFFFFFFF
1	1B6	FFFFFFFFFFFFFFFF	FFFFFFFFFFFFFFFF	FFFFFFFFFFFFFFFF	FFFFFFFFFFFFFFFF	FFFFFFFFFFFFFFFF

ICache Predecode Array

WAY	Index	SP	EndBits	P
0	1B6	0	FFFFFFFFFFFFFFFF	1
1	1B6	0	FFFFFFFFFFFFFFFF	1

ICache Branch Selector Array

WAY	Index	SP	M0	M1	M2	M3	M4	M5	M6	M7	M8	D1	D2	D3	B1Info	B1A	B2Info	B2A	B3Info	B3A
0	6D8	0	1	1	1	1	1	1	1	1	1	1	1	1	F	1	F	1	F	1
1	6D8	0	1	1	1	1	1	1	1	1	1	1	1	1	F	1	F	1	F	1

ICache L1 TLB Array

Index	SP	V	G	DGR	TPL	LinearTag	Cr3Tag	Wr	U	D	MT	RD	WD	TPH	PhysTag	Misc	HC	L2P	EntryID
00	0	0	0	0	1	0000000F8	00	0	1	0	0	1	0	1	00000F8	0	0	0	00
01	0	0	0	0	1	0000000FE	00	0	1	0	0	1	0	1	00000FE	0	0	0	01
02	0	0	0	0	1	0000000A8	00	0	1	0	0	1	0	1	00000A8	0	0	0	02
03	0	0	0	0	0	0000000A9	00	0	1	0	0	1	0	0	00000A9	0	0	0	03

Node 0 Core 0 Refresh Wr Chgs Wr All

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AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
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- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
  - L2Cache Data Array
  - L2Cache Data Array (Detailed)
  - L2Cache ECC Scrub Register
  - L2Cache Line Translator
  - L2Cache Tag Array
- Memory Debuggers
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1					

Refresh

Auto Refresh

ICache Line Translator 2 | **L2Cache Line Translator 1**

Address F000:0000000000000ED82 **Addr Type** Index

Segment CS Sel **Offset** rIP + 0000000000000000

00000000000FED82 (Linear) = 0000000000FED82 (Physical)

L2 Tag Array

WAY	Index	REDUN	SP	SE	S	State	D	V	IxD	VP	TECC	Tag	LRU
0	3B6	0	0	0	0	6	1	1	0	1	09	00000BF	0FDB9753
1	3B6	0	0	0	0	6	1	1	0	1	20	000000F	0FDB9753
2	3B6	0	0	0	0	6	1	1	0	1	42	000004F	0FDB9753
3	3B6	0	0	0	0	0	0	0	0	0	21	0010187	0FDB9753
4	3B6	0	0	0	0	6	1	1	0	1	68	0000047	0FDB9753
5	3B6	0	0	0	0	0	0	0	0	0	0A	0010287	0FDB9753
6	3B6	0	0	0	0	6	1	1	0	1	6D	000003F	0FDB9753
7	3B6	0	0	0	0	0	0	0	0	0	62	0010387	0FDB9753
8	3B6	0	0	0	0	6	1	1	0	1	47	0000037	0FDB9753
9	3B6	0	0	0	0	0	0	0	0	0	0C	0010487	0FDB9753
A	3B6	0	0	0	0	6	1	1	0	1	6B	0000027	0FDB9753
B	3B6	0	0	0	0	0	0	0	0	0	64	0010587	0FDB9753
C	3B6	0	0	0	0	6	1	1	0	1	0C	000001F	0FDB9753
D	3B6	0	0	0	0	0	0	0	0	0	4F	0010687	0FDB9753
E	3B6	0	0	0	0	6	1	1	0	1	26	0000017	0FDB9753
F	3B6	0	0	0	0	6	1	1	0	1	23	00000B7	0FDB9753

L2 Data Array

WAY	Index	Bytes 63:56	Bytes 55:48	Bytes 47:40	Bytes 39:32	Bytes 31:24
0	3B6	0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000
1	3B6	0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000
2	3B6	0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000
3	3B6	0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000
4	3B6	0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000
5	3B6	FFFFFFFFFFFFFFFF	FFFFFFFFFFFFFFFF	FFFFFFFFFFFFFFFF	FFFFFFFFFFFFFFFF	FFFFFFFFFFFFFFFF
6	3B6	0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000

Node 0 Core 0 Refresh Wr Chgs Wr All

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6) Debug Utilities

HDT Features

- Debug Utilities

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- Breakpoints
  - Define hardware breakpoints.
  - Setup conditional breakpoint.
  - Setup advanced breakpoint functions, such as breakpoint on exception.
  - Define software breakpoints using INT3 instruction on DRAM.
- Cache Diagnostic Loader
  - A special utility for ICache and DCache diagnostic
- Event Analyzer
  - A full logical analyzer, similar to TLA.
  - A new design that can define criteria and event on any node or core.
  - User can define as many clauses and states as possible.
- ICache Disassembly
  - Debug instructions in ICache

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
  - Breakpoints
  - Cache Diagnostic Loader
  - Cache Line Translator
  - Event Analyzer
  - ICache Disassembly
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1					

Refresh

Auto Refresh

Breakpoints 1 | Cache Diagnostic Loader 1 | Cache Line Translator 1 | Event Analyzer 1 | ICache Disassembly 1 | Binary File Loader 1

Hardware Breakpoints

	Linear Address		Global Enabled	Transaction Type	Breakpoint Length	Reset BP
DR0	0000000000000000		G0	Instruction Fetc	Byte	Clear BP0
DR1	0000000000000000		G1	Instruction Fetc	Byte	Clear BP1
DR2	0000000000000000		G2	Instruction Fetc	Byte	Clear BP2
DR3	0000000000000000		G3	Instruction Fetc	Byte	Clear BP3

GD Redirect Advanced << Break On SMM Conditional BP << Write All upon Reset

Software Breakpoints:

Add

	Linear Address		Enabled	Action

Remove All

Refresh Wr Chgs Wr All

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4 available Hardware Breakpoints for user to configure.
First screen will cover most breakpoint cases.

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
  - Breakpoints
  - Cache Diagnostic Loader
  - Cache Line Translator
  - Event Analyzer
  - ICache Disassembly
- Download Tools
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- I/O Ports
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- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1					

Refresh

Auto Refresh

Breakpoints 1 | Cache Diagnostic Loader 1 | Cache Line Translator 1 | Event Analyzer 1 | ICache Disassembly 1 | Binary File Loader 1

Hardware Breakpoints

	Linear Address		Global Enabled	Transaction Type	Breakpoint Length	Local Enabled	BP Pin	Reset BP
DR0	0000000000000000		G0	Instruction Fetc	Byte	L0		Clear BP0
DR1	0000000000000000		G1	Instruction Fetc	Byte	L1		Clear BP1
DR2	0000000000000000		G2	Instruction Fetc	Byte	L2		Clear BP2
DR3	0000000000000000		G3	Instruction Fetc	Byte	L3		Clear BP3

GD Redirect Advanced >> Break On SMM Conditional BP << Write All upon Reset

DR7	00000400	DBG_CTL_MSR2	00000000
Global Exact Enabled	GE	Data Match BPs	Address Match Only
Local Exact Enabled	LE	3DNow! causes #DNA	3DNow
ExcpBP_RIP	0000000000000000	MMX causes #DNA	MMX
ExcpBP_RIP_MASK	0000000000000000	x86 causes #DNA	FPU
ExcpBP_Ctl	00000000	SSE causes #DNA	DSSE
Enable Except BP	XEN	Signature on BP	SBP
Excpt/Int Vector	0x00 - DE	Enter HDT Mode	EHM
DR0_Data_Match	0000000000000000	DebugStatus	00000000
DR0_Data_Mask	0000000000000000	DR6	FFFF0FF0
DR0_ADDR_MASK	00000000	CR4	00000000
McodeCtl	00000000		

Software Breakpoints:

Add

	Linear Address		Enabled	Action

Remove All

Node 0 Core 0 Refresh Wr Chgs Wr All

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AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

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  - Breakpoints
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- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1					

Refresh

Auto Refresh

Breakpoints 1 | Cache Diagnostic Loader 1 | Cache Line Translator 1 | Event Analyzer 1 | ICache Disassembly 1 | Binary File Loader 1

Hardware Breakpoints

	Linear Address		Global Enabled	Transaction Type	Breakpoint Length	Local Enabled	BP Pin	Reset BP
DR0	0000000000000000		G0	Instruction Fetc	Byte	L0		Clear BP0
DR1	0000000000000000		G1	Instruction Fetc	Byte	L1		Clear BP1
DR2	0000000000000000		G2	Instruction Fetc	Byte	L2		Clear BP2
DR3	0000000000000000		G3	Instruction Fetc	Byte	L3		Clear BP3

GD Redirect Advanced << Break On SMM Conditional BP >> Write All upon Reset

HDT_CFG	00000000
Conditional HDT Compare Reg Address	RAX
False Branch	Enter HDT
True Branch	Enter HDT
Enable Conditional HDT	CHDT_EN
Disable Snoops in HDT	SNP_DIS
CondHDT_Value	0000000000000000
CondHDT_Value_MASK	0000000000000000

Software Breakpoints:

Add | Linear Address | Enabled | Action

Core 0 Refresh Wr Chgs Wr All

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"Conditional BP" available to further filter condition triggered through Hardware Breakpoints. For example, user may specify to break on any I/O access to port 80, but user can further filter with "Conditional BP" to actually break if AL = 0x10.

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
  - Breakpoints
  - Cache Diagnostic Loader
  - Cache Line Translator
  - Event Analyzer
  - ICache Disassembly
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- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1					

Refresh

Auto Refresh

Breakpoints 1 | Cache Diagnostic Loader 1 | Cache Line Translator 1 | Event Analyzer 1 | ICache Disassembly 1 | Binary File Loader 1

Hardware Breakpoints

	Linear Address		Global Enabled	Transaction Type	Breakpoint Length	Local Enabled	BP Pin	Reset BP
DR0	0000000000000000		G0	Instruction Fetc	Byte	L0		Clear BP0
DR1	0000000000000000		G1	Instruction Fetc	Byte	L1		Clear BP1
DR2	0000000000000000		G2	Instruction Fetc	Byte	L2		Clear BP2
DR3	0000000000000000		G3	Instruction Fetc	Byte	L3		Clear BP3

GD Redirect Advanced << Break On SMM Conditional BP >> Write All upon Reset

HDT_CFG	00000000
Conditional HDT Compare Reg Address	RAX
False Branch	Enter HDT
True Branch	Enter HDT
Enable Conditional HDT	CHDT_EN
Disable Snoops in HDT	SNP_DIS
CondHDT_Value	0000000000000000
CondHDT_Value_MASK	0000000000000000

Software Breakpoints:

Add

Remove All

	Linear Address		Enabled	Action
1	0000000000000000			Remove

Node 0 Core 0 Refresh Wr Chgs Wr All

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AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
  - Breakpoints
  - Cache Diagnostic Loader
  - Cache Line Translator
  - Event Analyzer
  - ICache Disassembly
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1					

Refresh

Auto Refresh

Breakpoints 1 | Cache Diagnostic Loader 1 | Cache Line Translator 1 | Event Analyzer 1 | ICache Disassembly 1 | Binary File Loader 1

Diagnostic Path: Browse... Load Diagnostic

Diagnostic Arguments Run Diagnostic

This feature is available for customers to receive or write own diagnostic test suite to be downloaded and executed out of cache.

Node 0 Core 0

start AMD Hardware Debu... 3:47 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
  - Breakpoints
  - Cache Diagnostic Loader
  - Cache Line Translator
  - Event Analyzer
  - ICache Disassembly
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1					

Refresh

Auto Refresh

Breakpoints 1 | Cache Diagnostic Loader 1 | Cache Line Translator 1 | Event Analyzer 1 | ICache Disassembly 1 | Binary File Loader 1

Diagnostic Path:

Browse... Load Diagnostic

Run Diagnostic

Diagnostic Arguments

	Value
Arg 1	0000000000000000
Arg 2	0000000000000000
Arg 3	0000000000000000
Arg 4	0000000000000000
Arg 5	0000000000000000
Arg 6	0000000000000000
Arg 7	0000000000000000
Arg 8	0000000000000000

Node 0 Core 0

start AMD Hardware Debu... 3:47 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
  - Breakpoints
  - Cache Diagnostic Loader
  - Cache Line Translator
  - Event Analyzer
  - ICache Disassembly
- Download Tools
- HyperTransport™ Technology
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- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1					

Refresh

Auto Refresh

Breakpoints 1 | Cache Diagnostic Loader 1 | **Cache Line Translator 1** | Event Analyzer 1 | ICache Disassembly 1 | Binary File Loader 1

Address 0000000000000000 **Addr Type** Linear

Segment **Offset** +

Data Cache Instruction Cache L2 Cache

Translate

Node 0 Core 0

start AMD Hardware Debu... 3:47 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
  - Breakpoints
  - Cache Diagnostic Loader
  - Cache Line Translator
  - ET Event Analyzer
  - ICache Disassembly
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instruct...

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1					

Refresh

Auto Refresh

Breakpoints 1 | Cache Diagnostic Loader 1 | Cache Line Translator 1 | **Event Analyzer 1** | ICache Disassembly 1 | Binary File Loader 1

State 1	
If	TRUE
Then	Do Nothing

This feature is SOFTWARE-driven, and can be used for further filtering if and only if a HARDWARE breakpoint has been set and triggered. Therefore, this feature will not be triggered and the conditions in this feature will not be evaluated unless a HARDWARE breakpoint has been HIT!!

Current State : 1

Counter 1	Counter 2	Counter 3	Counter 4
0000000000000000	0000000000000000	0000000000000000	0000000000000000
Reset	Reset	Reset	Reset

Force HDT On

Polling DBRdy

Polling Delay : 0 ms

Enable

Reset All Counters

start AMD Hardware Debu... 3:47 PM

Event Analyzer (cont)

AMD

CONFIDENTIAL

- Comparison between Event Trigger and Conditional Breakpoint

Features	Controlled by	Functionality	Performance
Conditional Breakpoint	Processor micro-code	Limited GPR and CR2; no multi-states; Only apply for one core	Very high speed
Event Analyzer	Fully by HDT	Complete logical analysis definitions and full process report No boundary limitation between nodes and cores	Slow. Speed depends on HDT connector and software

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
  - Breakpoints
  - Cache Diagnostic Loader
  - Cache Line Translator
  - Event Analyzer
  - ICache Disassembly
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1					

Refresh

Auto Refresh

Breakpoints 1 | Cache Diagnostic Loader 1 | Cache Line Translator 1 | Event Analyzer 1 | ICache Disassembly 1 | Binary File Loader 1

Tag	00000FE	Line Index	1B6	Offset	02
Number Of Lines	020	Physical Address	00000000000FED82	CS:rIP	

Breakpoints

BP	Address	Opcodes	Mnemonic	Code	Size

Node 0 | Core 0 | Refresh | Wr Chgs

start | AMD Hardware Debu... | 3:48 PM

CONFIDENTIAL

7) Download Tools

HDT Features
- Download Tools

CONFIDENTIAL

- Binary File Loader
  - Export target memory buffer, either DRAM or PCI, to a binary file.
  - Import binary file of memory, ICache, DCache or L2 Cache buffer, and then load it to target.
  - Import binary microcode file to load it to target processor.
- Save Text Report
  - Retrieve target info/data and then generate a text file to report the result.
  - The feature covers
    - All registers
    - Memory and Disassembly
    - Cache info
    - PCI info

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
  - Binary File Loader
  - Save Text Reports
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1					

Refresh

Auto Refresh

Binary File Loader 2

Export target memory to binary file

Address	0000000000000000			Addr Type	Linear
Segment		Offset		+	
Num of Bytes	00000200	Phys Type	Auto		

Full Path File Name: Browse...

Execute

Node 0 Core 0

start AMD Hardware Debu... 3:49 PM

This feature is used to download/export data files to/from user's target system. User can specify action, address, and location of file.

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
  - Binary File Loader
  - Save Text Reports
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1					

Refresh

Auto Refresh

Binary File Loader 2

Export target memory to binary file

- Export target memory to binary file
- Import binary file to target memory
- Import binary file to ICache
- Import binary file to DCache
- Import binary file to L2Cache
- Import Microcode File

0000000000000000 Addr Type Linear

Offset +

ys Type Auto

Full Path File Name: Browse...

Execute

Node 0 Core 0

start AMD Hardware Debu... 3:49 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
  - Binary File Loader
  - Save Text Reports
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1					

Refresh

Auto Refresh

Binary File Loader 2 | Save Text Reports 2

GPR | GPR (Compact) | rIP Only 0 | MSR

Memory Dump — Columns per line 8

Address	0000000000000000	Addr Type	Linear
Segment		Offset	+
Num of Bytes	00000200	Phys Type	Auto
		Display Size	32 bits

Disassembly — Code Size: Auto

Address	0000000000000000	Addr Type	Linear
Segment		Offset	+
Num of Bytes	00000200	Phys Type	Auto

ICache | DCache | L2 Cache | Refresh On Save

Retrieves Data from open Cache Feature windows only

PCI Data — Starting Bus: 0 — Ending Bus: 255 — PCI Config Space

Full Path File Name: Browse...

Export Report

Node 0 | Core 0

start | AMD Hardware Debu... | 3:50 PM

This feature gives the user the ability to DUMP desired information, such as GPR, Disassembly, or PCI Config Space to a text file for later viewing and/or analysis

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Save As

Save in: trash

My Recent Documents
Desktop
My Documents
My Computer
My Network Places

Debug
hdt6
LinuxCpuFreqD
ListCtrlDemo
res
_CodingTest[1].doc
~$ntis_word.doc
cpudump.txt
cpuregdump.txt
ListCtrlDemo.zip
Mantis_word.doc
msrdump.MSR
MyPropertyCtrl.positions
w2k3sp1_1218_usa_x86fre_spcd.iso

File name: gprcompact
Save as type:
Save
Cancel

rating Mode | BSP/AP | #DB Status | L2 Size
Refresh
Auto Refresh

MSR
Columns per line 8
Addr Type Linear
Display Size 32 bits
Code Size: Auto
Addr Type Linear
Save
255
PCI Config Space
Browse...

Export Report

Node 0 Core 0

start
AMD Hardware Debu...
3:52 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
  - Binary File Loader
  - Save Text Reports
- HyperTransport™ Technolog
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1					

Refresh

Auto Refresh

Binary File Loader 2 | Save Text Reports 2

gprcompact - WordPad

File Edit View Insert Format Help Send

```
General Register (Compact)
rIP              rAX              rBX              rCX              rDX              rSP
000000000000ED82 000000000000622C 0000000000000000 0000000038005803 0000000006060000 000
```

For Help, press F1

Export Report

Node 0 Core 0

start AMD Hardware Debu... gprcompact - WordPad 3:53 PM

This example shows a text file dump of the GPR (General Purpose Registers).

CONFIDENTIAL

8) HyperTransport

HDT Features

- HyperTransport™ Technology

CONFIDENTIAL

- HyperTransport™ Memory Map
  - Debugger of target HyperTransport™ memory map buffer.
- HyperTransport™ Trace Control
  - Use a trace logic definition to filter which packets to monitor.
  - Define a trace buffer.
- HyperTransport™ Trace Data Viewer
  - Dump trace buffer from target.
  - Interpret the source and destination of each HyperTransport™ packet.
- HyperTransport™ Trace Registers
  - Standard register viewer to fully expose the registers for HyperTransport™ trace analysis.

AMD Hardware Debug Tool (AMD Internal Only)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Technology
  - HyperTransport™ Memory Map
  - HyperTransport™ Trace Control
  - HyperTransport™ Trace Data Viewer
  - HyperTransport™ Trace Registers
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1	0	Legacy 16-bit Mode	BSP	B0	1024

Refresh

☑ Auto Refresh

HyperTransport™ Trace Registers 2 | **HyperTransport™ Trace Control 2**

Trace Start and Capture Conditions	
If	[None]
Then	Start and Capture [None]
Trace Stop Conditions	
If	[None]
Then	Stop Tracing

User can filter which packets to monitor through the if/then statements for both the START and STOP conditions.

BIOS had a "Trace Buffer" option to allocate memory. A 64MB chunk was allocated. This base can be changed to a user-defined region to the flush 28-packet internal trace buffer.

View data from Address Range:

Start Address	Start Address Type
000000001B000000	Trace Buffer Base
Stop Address	**Stop Address Type**
0000000000000100	Number of Bytes (+)

Start Trace | Analyze Data | Advanced Setup | HyperTransport™ Node 0 | Refresh | Wr Chgs | Wr All

start | D:\trash | AMD Hardware Debu... | 2:10 PM

AMD Hardware Debug Tool (AMD Internal Only)

File Edit View Features HDT Windows Help

User selects what causes/starts a trace-buffering session.

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ T
  - HyperTranspor
  - HyperTranspor
  - HyperTranspor
  - HyperTranspor
- I/O Ports
- Instruction Cache A
- JTAG Instructions
- L2 Cache Arrays
- Memory Debugger
- PCI Configuration
- Processor Register

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1	0	Legacy 16-bit Mode	BSP	B0	1024

Refresh

☑ Auto Refresh

Clause Definition

If

Item	+/-
	Remove
	Add

- Anything
- Timestamp Counter Rollover
- Machine Check Error
- Performance Monitor Event 3
- Performance Monitor Event 2
- Performance Monitor Event 1

Then Start and Capture

Item	+/-
	Remove
	Add

OK Cancel

View data from Address Range:

Start Address	Start Address Type
000000001B000000	Trace Buffer Base
Stop Address	**Stop Address Type**
0000000000000100	Number of Bytes (+)

Start Trace | Analyze Data | Advanced Setup

HyperTransport™ Node 0 | Refresh | Wr Chgs | Wr All

start | D:\trash | AMD Hardware Debu... | 2:10 PM

AMD Hardware Debug Tool (AMD Internal Only)

File Edit View Features HDT Windows Help

User selects what type of packets to capture.

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ T
  - HyperTranspor
  - HyperTranspor
  - HyperTranspor
  - HyperTranspor
- I/O Ports
- Instruction Cache A
- JTAG Instructions
- L2 Cache Arrays
- Memory Debugger
- PCI Configuration
- Processor Register

Node										
0	SH_B0/2-claw-754	0	0	1	0	Legacy 16-bit Mode	BSP	B0	1024	

Refresh

☑ Auto Refresh

Clause Definition

If

	Item	+/-
	Anything	Remove
		Add

Then Start and Capture

	Item	+/-
		Remove
		Add

- ALL
- Data Associated with SrcPtr/DstPtr Commands
- All Commands to DstPtr[4:0]
- All Commands to SrcPtr[4:0]
- Command Trigger 0
- Command Trigger 1

OK Cancel

View data from Address Range:

Start Address	Start Address Type
000000001B000000	Trace Buffer Base
Stop Address	**Stop Address Type**
0000000000000100	Number of Bytes (+)

Start Trace | Analyze Data | Advanced Setup | HyperTransport™ Node 0 | Refresh | Wr Chgs | Wr All

start | D:\trash | AMD Hardware Debu... | 2:10 PM

AMD Hardware Debug Tool (AMD Internal Only)

Clause Definition

If

Item	+/-
	Remove
	Add

- Performance Monitor Event 2
- Performance Monitor Event 1
- Performance Monitor Event 0
- DBREQ assertion
- Command Trigger 0
- Command Trigger 1

Then Stop Tracing

OK | Cancel

User selects what causes/stops a trace-buffering session.

Refresh

Auto Refresh

Link 1, HT Link 2)
k 2)

Processor Registers

View data from Address Range:

Start Address	Start Address Type
000000001B000000	Trace Buffer Base
Stop Address	**Stop Address Type**
0000000000000100	Number of Bytes (+)

Start Trace | Analyze Data | Advanced Setup | HyperTransport™ Node 0 | Refresh | Wr Chgs | Wr All

start | D:\trash | AMD Hardware Debu... | 2:11 PM

AMD Hardware Debug Tool (AMD Internal Only)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Technology
  - HyperTransport™ Memory Map
  - HyperTransport™ Trace Control
  - HyperTransport™ Trace Data Viewer
  - HyperTransport™ Trace Registers
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debu
- PCI Con
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1	0	Legacy 16-bit Mode	BSP	B0	1024

Refresh

☑ Auto Refresh

HyperTransport™ Trace Registers 2 | **HyperTransport™ Trace Control 2**

Trace Start and Capture Conditions	
If	Anything
Then	Start and Capture All Commands to SrcPtr[4:0] (System Request Interface, Memory Controller, HT Link 0, HT Link 1, HT Link 2) And All Commands to DstPtr[4:0] (System Request Interface, Memory Controller, HT Link 0, HT Link 1, HT Link 2) And Data Associated with SrcPtr/DstPtr Commands
Trace Stop Conditions	
If	DBREQ assertion
Then	Stop Tracing

After making selection, press "Wr Chngs" or "Write All" to submit changes.

View data from Address Range:

Start Address	Start Address Type
000000001B000000	Trace Buffer Base
Stop Address	**Stop Address Type**
0000000000000100	Number of Bytes (+)

Start Trace | Analyze Data | Advanced Setup | HyperTransport™ Node 0 | Refresh | Wr Chgs | Wr All

start | D:\trash | AMD Hardware Debu... | 2:12 PM

AMD Hardware Debug Tool (AMD Internal Only)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Technology
  - HyperTransport™ Memory Map
  - HyperTransport™ Trace Control
  - HyperTransport™ Trace Data Viewer
  - HyperTransport™ Trace Registers
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1	0	Legacy 16-bit Mode	BSP	B0	1024

Refresh

☑ Auto Refresh

HyperTransport™ Trace Registers 2 | **HyperTransport™ Trace Control 2**

Trace Start and Capture Conditions	
If	Anything
Then	Start and Capture All Commands to SrcPtr[4:0] (System Request Interface, Memory Controller, HT Link 0, HT Link 1, HT Link 2) And All Commands to DstPtr[4:0] (System Request Interface, Memory Controller, HT Link 0, HT Link 1, HT Link 2) And Data Associated with SrcPtr/DstPtr Commands
Trace Stop Conditions	
If	DBREQ assertion
Then	Stop Tracing

Use color-coding as visual aid to what has been written / modified
Or press "Refresh" to retrieve most recent.

View data from Address Range:

Start Address	Start Address Type
000000001B000000	Trace Buffer Base
Stop Address	**Stop Address Type**
0000000000000100	Number of Bytes (+)

Start Trace | Analyze Data | Advanced Setup | HyperTransport™ Node 0 | Refresh | Wr Chgs | Wr All

start | D:\trash | AMD Hardware Debu... | 2:12 PM

AMD Hardware Debug Tool (AMD Internal Only)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Technology
  - HyperTransport™ Memory Map
  - HyperTransport™ Trace Control
  - HyperTransport™ Trace Data Viewer
  - HyperTransport™ Trace Registers
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1	0	Legacy 16-bit Mode	BSP	B0	1024

Refresh

☑ Auto Refresh

HyperTransport™ Trace Registers 2 | **HyperTransport™ Trace Control 2**

Trace Start and Capture Conditions	
If	Anything
Then	Start and Capture All Commands to SrcPtr[4:0] (System Request Interface, Memory Controller, HT Link 0, HT Link 1, HT Link 2) And All Commands to DstPtr[4:0] (System Request Interface, Memory Controller, HT Link 0, HT Link 1, HT Link 2) And Data Associated with SrcPtr/DstPtr Commands
Trace Stop Conditions	
If	DBREQ assertion
Then	Stop Tracing

Pressing "Start Trace" will enable the correct bits in the "Start Control" register to prepare to start the buffering.

View data from Address Range:

Start Address	Start Address Type
000000001B000000	Trace Buffer Base
Stop Address	**Stop Address Type**
0000000000000100	Number of Bytes (+)

Start Trace | Analyze Data | Advanced Setup | HyperTransport™ Node 0 | Refresh | Wr Chgs | Wr All

start | D:\trash | AMD Hardware Debu... | 2:14 PM

AMD Hardware Debug Tool (AMD Internal Only)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Technology
  - HyperTransport™ Memory Map
  - HyperTransport™ Trace Control
  - HyperTransport™ Trace Data Viewer
  - HyperTransport™ Trace Registers
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1	0	Legacy 16-bit Mode	BSP	B0	1024

Refresh

☑ Auto Refresh

HyperTransport™ Trace Registers 2 | HyperTransport™ Trace Control 2

Register	Offset	Value
Time Stamp Counter Low	000000B0	8A386CFC
Time Stamp Counter High	000000B4	0000000E
Trace Buffer Base/Limit Address	000000B8	001E001B
Trace Buffer Address Pointer	000000BC	006C0000
Trace Control	000000C0	00100001
Trace Start	000000C4	00000000
Trace Stop	000000C8	00800000
Trace Capture	000000CC	9F1F0000
Trigger Event 0 Command Low	000000D0	00000000
Trigger Event 0 Command High	000000D4	00000000
Trigger Event 0 Mask Low	000000D8	00000000
Trigger Event 0 Mask High	000000DC	00000000
Trigger Event 1 Command Low	000000E0	00000000
Trigger Event 1 Command High	000000E4	00000000
Trigger Event 1 Mask Low	000000E8	00000000

Pressing "Start Trace" modified these bits.
User can right click on the value and view the subfield details.
The selections from the previous screen also modifies the appropriate registers.

NB_CFG	NB_CFG	Transaction Control
☐ Disable MCT-SRI Bypass	☐ Disable SRI-MCT Bypass	☐ Sequence ID source node enable

Start Now | Stop Now | HyperTransport™ Node 0 | Refresh | Wr Chgs | Wr All

start | D:\trash | AMD Hardware Debu... | 2:21 PM

AMD Hardware Debug Tool (AMD Internal Only)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Technology
  - HyperTransport™ Memory Map
  - HyperTransport™ Trace Control
  - HyperTransport™ Trace Data Viewer
  - HyperTransport™ Trace Registers
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1	0	Legacy 16-bit Mode	BSP	B0	1024

Refresh

☑ Auto Refresh

HyperTransport™ Trace Registers 2 | HyperTransport™ Trace Control 2

Register	Offset	Value
Time Stamp Counter Low	000000B0	ABB2B9CC
Time Stamp Counter High	000000B4	00000048
Trace Buffer Base/Limit Address	000000B8	001E001B
Trace Buffer Address Pointer	000000BC	006C0000
Trace Control	000000C0	00100001
Trace Start	000000C4	00000000
Trace Stop	000000C8	00800000
Trace Capture	000000CC	9F1F0000
Trigger Event 0 Command Low		
Trigger Event 1 Mask Low	000000E8	00000000
Trigger Event 1 Mask High	000000EC	00000000

NB_CFG	NB_CFG	Transaction Control
☐ Disable MCT-SRI Bypass	☐ Disable SRI-MCT Bypass	☐ Sequence ID source node enable

Start Now | Stop Now | HyperTransport™ Node 0 | Refresh | Wr Chgs | Wr All

Pressing "Start Now" STARTS the actual buffering.

start | D:\trash | AMD Hardware Debu... | 2:22 PM

AMD Hardware Debug Tool (AMD Internal Only)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Technology
  - HyperTransport™ Memory Map
  - HyperTransport™ Trace Control
  - HyperTransport™ Trace Data Viewer
  - HyperTransport™ Trace Registers
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1	0	Legacy 16-bit Mode	BSP	B0	1024

Refresh

☑ Auto Refresh

HyperTransport™ Trace Registers 2 | HyperTransport™ Trace Control 2

Register	Offset	Value
Time Stamp Counter Low	000000B0	40862332
Time Stamp Counter High	000000B4	00000051
Trace Buffer Base/Limit Address	000000B8	001E001B
Trace Buffer Address Pointer	000000BC	006C0043
Trace Control	000000C0	00100001
Trace Start	000000C4	00000000
Trace Stop	000000C8	00800000
Trace Capture	000000CC	9F1F0000
Trigger Event 0 Command Low	000000D0	00000000
Trigger Event 0 Command High	000000D4	00000000
Trigger Event 0 Mask Low	000000D8	00000000
Trigger Event 0 Mask High	000000DC	00000000

NB_CFG	NB_CFG	Transaction Control
☐ Disable MCT-SRI Bypass	☐ Disable SRI-MCT Bypass	☐ Sequence ID source node enable

Start Now | Stop Now | HyperTransport™ Node 0 | Refresh | Wr Chgs | Wr All

To verify that flushing of trace buffer is happening, user can press the "Refresh" button and see that the "Trace Buffer Address Pointer" is incrementing.

start | D:\trash | AMD Hardware Debu... | 2:22 PM

AMD Hardware Debug Tool (AMD Internal Only)

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- Data Cache Arrays
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  - HyperTransport™ Memory Map
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  - HyperTransport™ Trace Data Viewer
  - HyperTransport™ Trace Registers
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1	0	Legacy 16-bit Mode	BSP	B0	1024

Refresh

☑ Auto Refresh

HyperTransport™ Trace Registers 2 | HyperTransport™ Trace Control 2

Register	Offset	Value
Time Stamp Counter Low	000000B0	CB12A746
Time Stamp Counter High	000000B4	00000055
Trace Buffer Base/Limit Address	000000B8	001E001B
Trace Buffer Address Pointer	000000BC	006C0058
Trace Control	000000C0	00100001
Trace Start	000000C4	00000000
Trace Stop	000000C8	00800000
Trace Capture	000000CC	9F1F0000
Trigger Event 0 Command Low	000000D0	00000000
Trigger Event 0 Command High	000000D4	00000000
Trigger Event 0 Mask Low	000000D8	00000000

NB_CFG	NB_CFG	Transaction Control
☐ Disable MCT-SRI Bypass	☐ Disable SRI-MCT Bypass	☐ Sequence ID source node enable

Start Now | Stop Now | HyperTransport™ Node 0 | Refresh | Wr Chgs | Wr All

Press the "Stop Now" button to stop the buffering.

start | D:\trash | AMD Hardware Debu... | 2:22 PM

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- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1	0	Legacy 16-bit Mode	BSP	B0	1024

Refresh

☑ Auto Refresh

HyperTransport™ Trace Registers 2 | **HyperTransport™ Trace Control 2**

Trace Start and Capture Conditions	
If	[None]
Then	Start and Capture All Commands to SrcPtr[4:0] (System Request Interface, Memory Controller, HT Link 0, HT Link 1, HT Link 2) And All Commands to DstPtr[4:0] (System Request Interface, Memory Controller, HT Link 0, HT Link 1, HT Link 2) And Data Associated with SrcPtr/DstPtr Commands
Trace Stop Conditions	
If	DBREQ assertion
Then	Stop Tracing

Go back to the "Trace Control" page, and press "Analyze Data" to view a breakdown of the captured packets.

View data from Address Range

Start Address	Start Address Type
000000001B000000	Trace Buffer Base
Stop Address	**Stop Address Type**
0000000000000010	Number of Bytes (+)

Start Trace | Analyze Data | Advanced Setup | HyperTransport™ Node 0 | Refresh | Wr Chgs | Wr All

start | D:\trash | AMD Hardware Debu... | 2:22 PM

AMD Hardware Debug Tool (AMD Confidential)

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  - HyperTransport™
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  - I/O Access
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- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1	0	Legacy 32-bit Mode	BSP	DBReq	1024

Refresh

☑ Auto Refresh

HyperTransport™ Trace Control 1 | HyperTransport™ Trace Registers 1 | I/O Access 1 | **HyperTransport™ Trace Data Viewer 2**

Physical Address	Node	Quadword	Ctrl Byte	Type	Src->Dest	Route Info	Command Type	Addr
000000001B000008	00	5F35535F00000000	A6	DAT	SRI-->HT0		data= 5F35535F00000000	
000000001B000010	00	00000025C06C7960	03	TSC				
000000001B000018	00	0003B65843C00611	35	CwD	HT0-->SRI	U6.0.0	Cmd=RdSized(Coherent, Normal, Byte, Non-posted)	3B6584C
000000001B000020	00	00000025C06C92A6	03	TSC				
000000001B000088	00	0003B6580000C630	A5	CwD	SRI-->HT0	U6.0	Cmd=RdResponse	
000000001B000090	00	00000025C06C9338	03	TSC				
000000001B000098	00	5F35535F00000000	A6	DAT	SRI-->HT0		data= 5F35535F00000000	
000000001B0000A0	00	00000025C06C9339	03	TSC				
000000001B0000B8	00	0003B65843C00611	35	CwD	HT0-->SRI	U6.0.0	Cmd=RdSized(Coherent, Normal, Byte, Non-posted)	3B6584C
000000001B0000C8	00	00000025C06CAC86	03	TSC				
000000001B000138	00	0003B6580000C630	A5	CwD	SRI-->HT0	U6.0	Cmd=RdResponse	
000000001B000148	00	00000025C06CAD4D	03	TSC				
000000001B000150	00	5F35535F00000000	A6	DAT	SRI-->HT0		data= 5F35535F00000000	
000000001B000158	00	00000025C06CAD5C	03	TSC				
000000001B000160	00	0003B65843C00611	35	CwD	HT0-->SRI	U6.0.0	Cmd=RdSized(Coherent, Normal, Byte, Non-posted)	3B6584C
000000001B000168	00	00000025C06CC6A6	03	TSC				
000000001B0001D0	00	0003B6580000C630	A5	CwD	SRI-->HT0	U6.0	Cmd=RdResponse	
000000001B0001D8	00	00000025C06CC734	03	TSC				
000000001B0001E0	00	5F35535F00000000	A6	DAT	SRI-->HT0		data= 5F35535F00000000	
000000001B0001E8	00	00000025C06CC735	03	TSC				

Start Address

000000001B000000

Stop Address

0000000000000200

User Defined
Trace Buffer Base
Trace Buffer Offset
Trace Buffer Limit
Number of Bytes (+)
Number of Bytes (-)
Number of Bytes (+)

Filters

0 Text Filter
1 Add Timestamps
2 Merge ALL by Adjusted Timestamps (A
3 Merge ALL by Timestamps (ALL only)
4 Filter by Command (needs input)

Filter Input

Apply Filter

Remove Filter

HyperTransport™ Node 0

Refresh

start | D:\trash | AMD Hardware Debu... | 5:00 PM

HyperTransport Trace Mode Setup

CONFIDENTIAL

Bit Definitions

Bit	Name	Function
31–8	Reserved	**Reserved (RO)** All bits in this field must be cleared to 0 for normal system operation.
7–0	TmStmpHi	**Time Stamp High (RW)** Bits 39:32 of the time stamp counter

11.5.3 Trace Mode Address Registers

The DRAM address range to be used for the Trace Buffer is specified via the Trace Buffer Base/Limit Address Register. The current address which will be used to store the next Trace Buffer record is specified by the Trace Buffer Address Pointer Register. The Trace Buffer Address Register should be loaded with a value between the Trace Buffer Base/Limit (typically equal to the base address) prior to enabling Trace Mode. It is then updated by Trace Mode hardware as trace records are written to the Trace Buffer.

The addresses specified by these registers must be normalized to the system address and hence should be greater than the base address for the node in question defined via the DRAM address maps (See "Function 1: Address Map" on page 66.). During trace collection normal memory references must be prevented from accessing the Trace Buffer. This may be achieved by setting the DRAM limit in the DRAM Address Map to be less than the amount of DRAM physically present on the node by an amount equal to the region to be reserved for the Trace Buffer. The Trace Buffer Base Address should then be set to be above the corresponding DRAM Address Map limit address for the node.

The example below shows the DRAM Address Map (See "Function 1: Address Map" on page 66.) and Trace Buffer address settings for a 2-node system with 256M of DRAM on each node and for which a 64M Trace Buffer region has been reserved for tracing traffic on node 1.

DRAM Base 0 : 0M
DRAM Limit 0 : 255M
DRAM Base 1 : 256M
DRAM Limit 1 : 447M
Trace Buffer Base (node 1) : 448M
Trace Buffer Limit (node 1) : 511M
Trace Buffer Pointer (node 1) : 448M

Trace Buffer Base/Limit Address — **Function 2 Offset B8h**

	Bits 31–16	Bits 15–0
Bit	TrcBufDramLimit[39:24]	TrcBufDramBase[39:24]
Reset		
R/W	RW	RW

Bit	Name	Function
3–2	Reserved	**Reserved (RO)** All bits in this field must be cleared to 0 for normal system operation.
1	StopCmd1	Stop on Command Trigger 1 (RW)
0	StopCmd0	Stop on Command Trigger 0 (RW)

11.5.7 Trace Capture Register

The Trace Capture Register is used to specify what traffic to capture when Trace Mode is in an active state (after an event specified in the Trace Start Register and before an event specified in the Trace Stop Register. Multiple capture criteria may be specified.

There are two principal types of capture events - capture by route or capture by packet type. Commands which match certain routing criteria can be captured by using a combination of source and destination pointers (TrcCmdSrcPtr[4:0]/TrcCmdDstPtr[4:0]). A command packet routed from XBAR source port n to XBAR destination port m will be captured if the appropriate bits n and m are both set in the source and destination pointers respectively. Multiple bits can be set in either pointer to capture traffic from multiple source ports and/or to multiple destination ports.

Commands can be captured by packet type by using the Trigger Event Command/Mask registers. Commands which match the trigger events can be captured as can responses or probes issued on behalf of the matching commands.

For both capture types (capture by route or capture by packet type) the data associated with a command can also be captured by setting the appropriate data capture bits.

Trace Capture — **Function 2 Offset CCh**

	31	30–29	Bits 28–24	23–21	20–16	15–14	13	12	11–10	9	8	7–6	5	4	3–2	1	0
Bit		Rsrvd		Rsrvd		Rsrvd			Rsrvd			Rsrvd			Rsrvd		
Reset	0	0	0 0 0 0 0 0 0 0	0 0 0	0 0 0 0 0	0 0	0	0	0 0	0	0	0 0	0	0	0 0	0	0
R/W		RW	RO RW	RO	RW	RO	RW	RW	RO	RW	RW	RO	RW	RW	RO	RW	RW

Bit Definitions

Bit	Name	Function
31	TrcDatSrcDst	**Trace Data Associated with SrcPtr/DstPtr Commands (RW)**
30–29	Reserved	**Reserved (RO)** All bits in this field must be cleared to 0 for normal system operation.

CONFIDENTIAL

9) I/O Ports

HDT Features

- I/O Ports

CONFIDENTIAL

- I/O Access
  - Tool to access target I/O ports (i.e. read and write to specified ports)

AMD Hardware Debug Tool (AMD Confidential)

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Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1					

Refresh

Auto Refresh

I/O Access 3

Port (Hex)	0080
Value (Hex)	AA
Access Size	8

	R/W	Port	Access	Value
1	R	80	8	AA

Refresh Wr All

start AMD Hardware Debu... 5:50 PM

This feature allows the user to READ or WRITE to any I/O ports. In this example, the value 0xAA was read from port 80. Pressing "Write All" submits changes. Pressing "Refresh" acts as a READ from the port specified in the "Port (Hex)" field.

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Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1					

Refresh

Auto Refresh

I/O Access 3

Port (Hex)	0080
Value (Hex)	CC
Access Size	8

	R/W	Port	Access	Value
1	W	80	8	CC
2	R	80	8	AA

Most recent RESULTS are shown on top of history stack.
In this example, a 0xCC was written to port 80.

Refresh WrAll

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AMD Hardware Debug Tool (AMD Confidential)

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Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1					

Refresh

Auto Refresh

I/O Access 3

Port (Hex)	0080
Value (Hex)	CC
Access Size	8

	R/W	Port	Access	Value
1	R	80	8	CC
2	W	80	8	CC
3	R	80	8	AA

Pressing "Refresh" does a READ

Refresh Wr All

start AMD Hardware Debu... 5:51 PM

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10) Memory Debuggers

HDT Features

- Memory Debuggers

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- A feature group to debug target memory control and buffer
- Memory Dump
  - User can specify target memory buffer using different address, format, memory type, PCI, DRAM, etc.
  - Dump or modify target memory buffer.
  - Various display formats.
- Disassembly
  - Disassemble target buffer to instructions.
  - User can set breakpoint on instructions.
  - Ability to automatically track target instruction changes.
  - Define SoftICE likely hot key as default. User can change hot key definition.

HDT Features

- Memory Debuggers (cont)

CONFIDENTIAL

- DRAM Address Translator
  - Translate Linear, Logical or Indexed address to physical address based on current target data.
  - Translation pages involved is displayed.
  - Memory type is displayed.
  - Physical to Linear address translation will be developed in future version.
- Target Memory Search
  - Search target memory buffer.
  - Define criteria using either opcode or string.
  - Complete memory buffer definition.

AMD Hardware Debug Tool (AMD Confidential)

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  - CPU Registers
  - Debug Registers
  - FPU Registers
  - Last Branch Registers
  - MCA Registers
  - Model Specific Registers
  - MTRR Registers
  - Performance Registers
  - Program Registers
  - Segment Registers
  - SEM Registers
  - Single MSR
  - SSE Registers
  - TR & SMM Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1					

Refresh

☑ Auto Refresh

Disassembly 1

Address	0000000000000000	Addr Type	Linear
Segment		Offset	+
Num of Bytes	00000200	Phys Type	Auto

Breakpoints

☐ Auto Track CS:rIP

BP	Address	Opcodes	Mnemonic	Code	Size

Node 0 | Core 0 | Refresh | Wr Chgs

CPU Registers 1

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  - Segment Registers
  - SEM Registers
  - Single MSR
  - SSE Registers
  - TR & SMM Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1					

Refresh

☑ Auto Refresh

Disassembly 1

Address	0000000000000000	Addr Type	Linear
Segment		Offset	+
Num of Bytes	00000200	Phys Type	Auto

Physical
Linear
Logical
Index
CS:rIP
SS:RSP

Breakpoints

☐ Auto Track CS:rIP

BP	Address	Opcodes	Mnemonic	Code	Size

User can select Address Type or some predefined addresses that automatically populate address fields.

Node 0 | Core 0 | Refresh | Wr Chgs

CPU Registers 1

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  - Performance Registers
  - Program Registers
  - Segment Registers
  - SEM Registers
  - Single MSR
  - SSE Registers
  - TR & SMM Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1					

Refresh

☑ Auto Refresh

Disassembly 1

Address	F000:000000000000E05B			Addr Type	Index
Segment	CS Sel	Offset	rIP	+	0000000000000000
Num of Bytes	00000200	Phys Type	Auto		

Breakpoints

☐ Auto Track CS:rIP

BP	Address	Opcodes	Mnemonic	Code

Cache DRAM
UnC DRAM
WrtBk DRAM
PCI Bus Mem
Auto

User can select Target Memory Type to access.

Node 0 | Core 0 | Refresh | Wr Chgs

CPU Registers 1

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Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1					

Refresh

Auto Refresh

Disassembly 1

Address: F000:000000000000E05B

Addr Type: Index

Segment: CS Sel

Offset: rIP + 0000000000000000

Num of Bytes: 00000200

Phys Type: Auto

Breakpoints

Auto Track CS:rIP

BP	Address	Opcodes	Mnemonic	Code	Size
	F000:000000000000E05B	EA 60 E0 00 F0	jmp	f000:e060h	16
	F000:000000000000E060	8E EA	mov	gs,dx	16
	F000:000000000000E062	66 8B C8	mov	ecx,eax	16
	F000:000000000000E065	B0 A0	mov	al,a0h	16
	F000:000000000000E067	E6 80	out	80h,al	16
	F000:000000000000E069	B0 80	mov	al,80h	16
	F000:000000000000E06B	E6 70	out	70h,al	16
	F000:000000000000E06D	FA	cli		16
	F000:000000000000E06E	FC	cld		16
	F000:000000000000E06F	8C C8	mov	ax,cs	16
	F000:000000000000E071	8E D0	mov	ss,ax	16
	F000:000000000000E073	66 8B D9	mov	ebx,ecx	16
	F000:000000000000E076	66 B8 6C C0 00 80	mov	eax,8000c06ch	16
	F000:000000000000E07C	BA F8 0C	mov	dx,0cf8h	16
	F000:000000000000E07F	66 EF	out	dx,eax	16
	F000:000000000000E081	83 C2 04	add	dx,04h	16
	F000:000000000000E084	66 ED	in	eax,dx	16
	F000:000000000000E086	8A C8	mov	cl,al	16
	F000:000000000000				16

Selecting "Auto Track CS:rIP" will automatically move the "Yellow Arrow" to the most current line of code.

Node: 0, Core: 0

Node 0 Core 0 Refresh Wr Chgs

CPU Registers 1

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AMD Hardware Debug Tool (AMD Confidential)

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User can also Right-Click on address value to manually step through the disassembly window, insert breakpoints, etc..

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  - Segment Registers
  - SEM Registers
  - Single MSR
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  - TR & SMM Registers

Auto Refresh

Disassembly 1

Address	F000:000000000000E05B			Addr Type	Index
Segment	CS Sel	Offset	rIP	+	0000000000000000
Num of Bytes	00000200	Phys Type	Auto		

Breakpoints

Auto Track CS:rIP

BP	Address	Opcodes	Mnemonic	Code	Size
	F000:000000000000E05B	EA 60 E0 00 F0	jmp	f000:e060h	16
	F000:		mov	gs,dx	16
	F000:		mov	ecx,eax	16
	F000:		mov	al,a0h	16
	F000:		out	80h,al	16
	F000:		mov	al,80h	16
	F000:		out	70h,al	16
	F000:		cli		16
	F000:		cld		16
	F000:		mov	ax,cs	16
	F000:		mov	ss,ax	16
	F000:		mov	ebx,ecx	16
	F000:	0 00 80	mov	eax,8000c06ch	16
	F000:		mov	dx,0cf8h	16
	F000:		out	dx,eax	16
	F000:		add	dx,04h	16
	F000:		in	eax,dx	16
	F000:		mov	cl,al	16
	F000:		or	al,10h	16
	F000:		out	dx,eax	16
	F000:000000000000E08C	66 B8 C0 00 00 80	mov	eax,800000c0h	16
	F000:000000000000E092	83 EA 04	sub	dx,04h	16

Copy
Paste
Find...
Load Ctrl+O
Save As ... Ctrl+S
Print Ctrl+P
✔ Display Opcode Column Alt+F3
Insert HW Breakpoint F9
Enable HW Breakpoint Ctrl+F9
Insert SW Breakpoint Shift+F9
Enable SW Breakpoint Ctrl+Shift+F9
Step Into (Single Step) F8
Step Over Alt+F10
Jump rIP to Next Row
Run to Cursor F7
Properties

Node: 0, Core: 0
Cursor Addr = F000:000000000000E05B = 00000000000FE05B (Phys)
UC/IO@Basic

Node 0 | Core 0 | Refresh | Wr Chgs

CPU Registers 1

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AMD Hardware Debug Tool (AMD Confidential)

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  - Performance Registers
  - Program Registers
  - Segment Registers
  - SEM Registers
  - Single MSR
  - SSE Registers
  - TR & SMM Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1					

Refresh

Auto Refresh

Disassembly 1

Address: F000:000000000000E060 | Addr Type: Index | Breakpoints

Segment: CS Sel | Offset: rIP | + 0000000000000000 | Auto Track CS:rIP

Num of Bytes: 00000200 | Phys Type: Auto

BP	Address	Opcodes	Mnemonic	Code	Size
	F000:000000000000E05B	EA 60 E0 00 F0	jmp	f000:e060h	16
	F000:000000000000E060	8E EA	mov	gs,dx	16
	F000:000000000000E062	66 8B C8	mov	ecx,eax	16
	F000:000000000000E065	B0 A0	mov	al,a0h	16
	F000:000000000000E067	E6 80	out	80h,al	16
	F000:000000000000E069	B0 80	mov	al,80h	16
	F000:000000000000E06B	E6 70	out	70h,al	16
	F000:000000000000E06D	FA	cli		16
	F000:000000000000E06E	FC	cld		16
	F000:000000000000E06F	8C C8	mov	ax,cs	16
	F000:000000000000E071	8E D0	mov	ss,ax	16
	F000:000000000000E073	66 8B D9	mov	ebx,ecx	16
	F000:000000000000E076	66 B8 6C C0 00 80	mov	eax,8000c06ch	16
	F000:000000000000E07C	BA F8 0C	mov	dx,0cf8h	16
	F000:000000000000E07F	66 EF	out	dx,eax	16
	F000:000000000000E081	83 C2 04	add	dx,04h	16
	F000:000000000000E084	66 ED	in	eax,dx	16
	F000:000000000000E086	8A C8	mov	cl,al	16
	F000:000000000000E088	0C 10	or	al,10h	16
	F000:000000000000E08A	66 EF	out	dx,eax	16
	F000:000000000000E08C	66 B8 C0 00 00 80	mov	eax,800000c0h	16
	F000:000000000000E092	83 EA 04	sub	dx,04h	16

Node: 0, Core: 0
Cursor Addr = F000:000000000000E060 = 00000000000FE060 (Phys)
UC/IO@Basic

Node 0 | Core 0 | Refresh | Wr Chgs

CPU Registers 1

start | AMD Hardware Debu... | HDT6Overview.ppt | DebugPresentation_I... | 10:01 AM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
  - Disassembly
  - DRAM Address Translator
  - Memory Dump
  - Target Memory Search
- PCI Configuration
- Processor Registers
  - CPU Registers
  - Debug Registers
  - FPU Registers
  - Last Branch Registers
  - MCA Registers
  - Model Specific Registers
  - MTRR Registers
  - Performance Registers
  - Program Registers
  - Segment Registers
  - SEM Registers
  - Single MSR
  - SSE Registers
  - TR & SMM Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1					

Refresh

☑ Auto Refresh

Disassembly 1 | DRAM Address Translator 1

Address	F000:000000000000E060			Addr Type	Index
Segment	CS Sel	Offset	rIP	+	0000000000000000

Legacy 16-bit Mode

☐ EFER.LMA ☐ CR4.PSE ☐ CR0.PG ☐ CR4.PAE

	Base	Offset	Table Entry
	No page table information available		

00000000000FE060 (Linear) = 00000000000FE060 (Physical)

Node 0 | Core 0 | Refresh

CPU Registers 1

start | AMD Hardware Debu... | HDT6Overview.ppt | DebugPresentation_I... | 10:02 AM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
  - Disassembly
  - DRAM Address Translator
  - Memory Dump
  - Target Memory Search
- PCI Configuration
- Processor Registers
  - CPU Registers
  - Debug Registers
  - FPU Registers
  - Last Branch Registers
  - MCA Registers
  - Model Specific Registers
  - MTRR Registers
  - Performance
  - Program Regi
  - Segment Registers
  - SEM Registers
  - Single MSR
  - SSE Registers
  - TR & SMM Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1	0	Legacy 32-bit Mode	BSP	DBReq	1024

Refresh

☑ Auto Refresh

DRAM Address Translator 1 | Target Memory Search 1 | Disassembly 1 | CPU Registers 1 | Memory Dump 1

Address	0008:00000000806B2FAA		Addr Type	Index	
Segment	CS Sel	Offset	rIP	+	0000000000000000

4-Mbyte Page Translation - Non-PAE Paging Legacy-Mode

☐ EFER.LMA ☑ CR4.PSE ☑ CR0.PG ☐ CR4.PAE

	Base	Offset	Table Entry
Page-Directory Table	0000000000039000	0000000000000804	0003E163004001E3
4 Mbyte Physical Page	0000000000400000	00000000002B2FAA	00000000006B2FAA (Phys Addr)

Under "DRAM Address Translator", the new implementation does a FULL address translation. In this example, we're in Legacy 32-bit Mode.

00000000806B2FAA (Linear) = 00000000006B2FAA (Physical)

Segment Base Address = 0000000000000000, Phys Addr Len = 40 bits

Node 0 | Core 0 | Refresh

start | AMD Hardware Debu... | HDT6Overview.ppt | DebugPresentation_I... | 10:17 AM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
  - Disassembly
  - DRAM Address Translator
  - Memory Dump
  - Target Memory Search
- PCI Configuration
- Processor Registers
  - CPU Registers
  - Debug Registers
  - FPU Registers
  - Last Branch Registers
  - MCA Registers
  - Model Specific Registers
  - MTRR Registers
  - Performance Registers
  - Program Registers
  - Segment Registers
  - SEM Registers
  - Single MSR
  - SSE Registers
  - TR & SMM Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1					

Refresh

☑ Auto Refresh

Disassembly 1 | DRAM Address Translator 1 | **Memory Dump 1**

Address	F000:0000000000000E060		**Addr Type**	Index	
Segment	CS Sel	**Offset**	rIP	+	0000000000000000
Num of Bytes	00000200	**Phys Type**	Auto	**Display Size**	16 bits

Fill Memory

☐ Auto Track SS:rSP

☐ Dump Phys Mem

F000:0000000000000E060	EA8E	8B66	B0C8	E6A0	B080	E680	FA70	8CFC	. ê f . È ° æ . ° . æ p ü
F000:0000000000000E070	8EC8	66D0	D98B	B866	C06C	8000	F8BA	660C	È . Ð f . Ù f ¸ l À . . ° ø
F000:0000000000000E080	83EF	04C2	ED66	C88A	100C	EF66	B866	00C0	ï . Â . f í . È . . f ï f .
F000:0000000000000E090	8000	EA83	6604	83EF	06C2	24EC	0CF0	EE08	. . . ê . f ï . Â . ì $ ð .
F000:0000000000000E0A0	B866	0874	8000	F8BA	660C	83EF	04C2	01B8	f ¸ t . . . ° ø . f ï . Â .
F000:0000000000000E0B0	EF0E	C0B8	8340	04EA	EF66	C283	EC06	F024	. ï ¸ À @ . ê . f ï . Â . ì
F000:0000000000000E0C0	F6EE	10C1	850F	0013	8B66	BAC3	0EF0	EF66	î ö Á . . . . . f . Ã ° ð .
F000:0000000000000E0D0	3366	BAC0	0EF4	EF66	0BEB	BA90	0EF4	ED66	f 3 À ° ô . f ï ë . . ° ô .
F000:0000000000000E0E0	0B66	66C3	66EF	CB8B	04B2	ECB6	C68A	72E6	f . Ã f ï f . Ë ² . ¶ ì . Æ
F000:0000000000000E0F0	C18A	73E6	C166	08C9	C6FE	CAFE	EE75	BF66	. Á æ s f Á É . þ Æ þ Ê u ¿
F000:0000000000000E100	203A	9C5A	B866	0001	0000	A20F	EF24	003C	: Z . f ¸ . . . . . ¢ $ <
F000:0000000000000E110	840F	000F	013C	840F	0015	403C	840F	004F	. . . . < . . . . . < @ . .
F000:0000000000000E120	8AE9	6600	21B9	0110	0FC0	0C32	0F10	6630	é . . f ¹ ! . . À . 2 . . .
F000:0000000000000E130	1FB9	0110	0FC0	8032	10CA	300F	B966	1022	¹ . . . À . 2 . Ê . . 0 f ¹
F000:0000000000000E140	C001	320F	0D66	0400	0108	300F	B966	1023	. À . 2 f . . . . . 0 f ¹
F000:0000000000000E150	C001	320F	CA80	0F20	6630	D4B8	00C3	BA80	. À . 2 . Ê . . 0 f ¸ Ô Ã .
F000:0000000000000E160	0CF8	EF66	C283	6604	02B8	7100	6602	66EF	ø . f ï . Â . f ¸ . . q . f
F000:0000000000000E170	90B8	00C2	BA80	0CF8	EF66	C283	6604	0CED	¸ . Â . . ° ø . f ï . Â . f
F000:0000000000000E180	6608	24EF	66F7	66EF	22B9	0110	0FC0	6632	. f ï $ ÷ f ï f ¹ " . . À .
F000:0000000000000E190	000D	0004	0F00	6630	D4B8	00C3	BA80	0CF8	. . . . . 0 f ¸ Ô Ã . . ° ø
F000:0000000000000E1A0	EF66	C283	6604	01B8	0D00	6600	66EF	D8B8	f ï . Â . f ¸ . . . . . f ï f
F000:0000000000000E1B0	00C3	BA80	0CF8	EF66	C283	6604	00B8	0000	Ã . . ° ø . f ï . Â . f ¸ . .
F000:0000000000000E1C0	6600	66EF	94B8	00C0	BA80	0CF8	EF66	C283	. f ï f . . À . . ° ø . f ï

Node: 0, Core: 0

Node 0 | Core 0 | Refresh | Wr Chgs

CPU Registers 1

start | AMD Hardware Debu... | HDT6Overview.ppt | DebugPresentation_I... | 10:03 AM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features

User can find the current Target Memory Type at the bottom of the windows.

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
  - Disassembly
  - DRAM Address Translator
  - Memory Dump
  - Target Memory Search
- PCI Configuration
- Processor Registers
  - CPU Registers
  - Debug Registers
  - FPU Registers
  - Last Branch Registers
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  - Model Specific Registers
  - MTRR Registers
  - Performance Registers
  - Program Registers
  - Segment Registers
  - SEM Registers
  - Single MSR
  - SSE Registers
  - TR & SMM Registers

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1					

Refresh

Auto Refresh

DRAM Address Translator 1 | Memory Dump 1

Address: F000:000000000000E060 | Addr Type: Index | Fill Memory

Segment: CS Sel | Offset: rIP | + 0000000000000000

Num of Bytes: 00000200 | Phys Type: Auto | Display Size: 16 bits

Auto Track SS:rSP

Dump Phys Mem

F000:000000000000E060	EA8E	8B66	B0C8	E6A0	B080	E680	FA70	8CFC	. ê f . È ° æ . ° . æ p ü
F000:000000000000E070	8EC8	66D0	D98B	B866	C06C	8000	F8BA	660C	È . Ð f . Ù f ¸ l À . . ° ø
F000:000000000000E080	83EF	04C2	ED66	C88A	100C	EF66	B866	00C0	ï . Â . f í . È . . f ï f .
F000:000000000000E090	8000	EA83	6604	83EF	06C2	24EC	0CF0	EE08	. . . ê . f ï . Â . ì $ ð .
F000:000000000000E0A0	B866	0874	8000	F8BA	660C	83EF	04C2	01B8	f ¸ t . . . ° ø . f ï . Â .
F000:000000000000E0B0	EF0E	C0B8	8340	04EA	EF66	C283	EC06	F024	. ï ¸ À @ . ê . f ï . Â . ì
F000:000000000000E0C0	F6EE	10C1	850F	0013	8B66	BAC3	0EF0	EF66	î ö Á . . . . . f . Ã ° ð

Node: 0, Core: 0
Cursor Addr = F000:000000000000E060 = 00000000000FE060 (Phys)
UC/IO@Basic

Node 0 | Core 0 | Refresh | Wr Chgs

Disassembly 1 | CPU Registers 1

Address: F000:000000000000E060 | Addr Type: Index | Breakpoints

Segment: CS Sel | Offset: rIP | + 0000000000000000

Num of Bytes: 00000200 | Phys Type: Auto

Auto Track CS:rIP

BP	Address	Opcodes	Mnemonic	Code	Size
	F000:000000000000E05B	EA 60 E0 00 F0	jmp	f000:e060h	16
	F000:000000000000E060	8E EA	mov	gs,dx	16
	F000:000000000000E062	66 8B C8	mov	ecx,eax	16
	F000:000000000000E065	B0 A0	mov	al,a0h	16
	F000:000000000000E067	E6 80	out	80h,al	16
	F000:000000000000E069	B0 80	mov	al,80h	16

Node: 0, Core: 0
Cursor Addr = F000:000000000000E060 = 00000000000FE060 (Phys)
UC/IO@Basic

Node 0 | Core 0 | Refresh | Wr Chgs

start | AMD Hardware Debu... | HDT6Overview.ppt | DebugPresentation_I... | 10:04 AM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT

User can do a pattern search within a specified memory region.
In this example, searching for 0x66 starting at CS:rIP

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
  - Disassembly
  - DRAM Address Translator
  - Memory Dump
  - Target Memory Search
- PCI Configuration
- Processor Registers
  - CPU Registers
  - Debug Registers
  - FPU Registers
  - Last Branch Registers
  - MCA Registers
  - Model Specific Registers
  - MTRR Registers
  - Performance Registers
  - Program Registers
  - Segment Registers
  - SEM Registers
  - Single MSR
  - SSE Registers
  - TR & SMM Registers

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1					

Refresh

☑ Auto Refresh

DRAM Address Translator 1 | Memory Dump 1 | **Target Memory Search 1** | Disassembly 1 | CPU Registers 1

Address	F000:0000000000E060			**Addr Type**	Index
Segment	CS Sel	**Offset**	rIP	+	0000000000000000
Num of Bytes	00000200	**Phys Type**	Auto	**Display Size**	32 bits

Open Feature
- (•) Disassembly
- ( ) Memory Dump

Search Data

(•) Opcode (in Hex)	66
( ) String	

Search Result

Address	Disassembly
F000:0000000000E062	Show
F000:0000000000E073	Show
F000:0000000000E076	Show
F000:0000000000E07F	Show
F000:0000000000E084	Show
F000:0000000000E08A	Show
F000:0000000000E08C	Show
F000:0000000000E095	Show
F000:0000000000E0A0	Show
F000:0000000000E0A9	Show
F000:0000000000E0B8	Show
F000:0000000000E0C8	Show
F000:0000000000E0CE	Show
F000:0000000000E0D0	Show
F000:0000000000E0D6	Show
F000:0000000000E0DE	Show
F000:0000000000E0E0	Show
F000:0000000000E0E3	Show
F000:0000000000E0E5	Show
F000:0000000000E0F4	Show
F000:0000000000E0FE	Show

Node 0 | Core 0 | Refresh

start | AMD Hardware Debu... | HDT6Overview.ppt | DebugPresentation_I... | 10:06 AM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
  - Disassembly
  - DRAM Address Translator
  - Memory Dump
  - Target Memory Search
- PCI Configuration
- Processor Registers
  - CPU Registers
  - Debug Registers
  - FPU Registers
  - Last Branch Registers
  - MCA Registers
  - Model Specific Registers
  - MTRR Registers
  - Performance Registers
  - Program Registers
  - Segment Registers
  - SEM Registers
  - Single MSR
  - SSE Registers
  - TR & SMM Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1					

Refresh

Auto Refresh

DRAM Address Translator 1 | **Target Memory Search 1** | Disassembly 1 | CPU Registers 1 | Memory Dump 1

Address	F000:0000000000000E060			**Addr Type**	Index
Segment	CS Sel	**Offset**	rIP	+	0000000000000000
Num of Bytes	00000200	**Phys Type**	Auto	**Display Size**	32 bits

Open Feature

- Disassembly
- Memory Dump

Search Data

- Opcode (in Hex) 66
- String

Search Result

Address	Memory Dump
F000:0000000000000E062	Show
F000:0000000000000E073	Show
F000:0000000000000E076	Show
F000:0000000000000E07F	Show
F000:0000000000000E084	Show
F000:0000000000000E08A	
F000:0000000000000E0	
F000:0000000000000	
F000:0000000000000	
F000:0000000000000E	
F000:0000000000000E0B8	
F000:0000000000000E0C8	Show
F000:0000000000000E0CE	Show
F000:0000000000000E0D0	Show
F000:0000000000000E0D6	Show
F000:0000000000000E0DE	Show
F000:0000000000000E0E0	Show
F000:0000000000000E0E3	Show
F000:0000000000000E0E5	Show
F000:0000000000000E0F4	Show
F000:0000000000000E0FE	Show

Node 0 | Core 0 | Refresh

User can switch between showing "Disassembly" or "Memory Dump" View after pressing the "Show" button.

start | AMD Hardware Debu... | HDT6Overview.ppt | DebugPresentation_I... | 10:07 AM

CONFIDENTIAL

11) PCI Configuration

HDT Features
- PCI Configuration

CONFIDENTIAL

- PCI Device Search
  - Scans a specified range of buses (0-255) and returns all PCI devices found.
- PCI Configuration Space
  - Dumps a standard PCI configuration space for a device.
  - Users can modify the target PCI Config registers.
  - The extended space for PCI-Express will be developed in the future.
- PCI Configuration Registers
  - Displays PCI Config registers for a PCI device in a user-friendly format.
  - Users can access subfield definition of each register.
  - Users can modify the target PCI Config registers.

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
  - PCI Configuration Registers
  - PCI Configuration Space
  - PCI Device Search
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1					

Refresh

Auto Refresh

PCI Device Search 1

Vendor Name	VID	DID	Rev	Bus	Dev	Fun	Description	Space	Register
Advanced Micro Devices	1022	7454	13	0	0	0	AMD-8151™ System Controller	BCS	Show
Advanced Micro Devices	1022	7455	13	0	1	0	AMD-8151™ AGP Bridge	BCS	Show
Advanced Micro Devices	1022	7460	07	0	6	0	AMD-8111™ PCI	BCS	Show
Advanced Micro Devices	1022	7468	05	0	7	0	AMD-8111™ LPC	BCS	Show
Advanced Micro Devices	1022	7469	03	0	7	1	AMD-8111™ IDE	BCS	Show
Advanced Micro Devices	1022	746A	02	0	7	2	AMD-8111™ SMBus 2.0	BCS	Show
Advanced Micro Devices	1022	746B	05	0	7	3	AMD-8111™ ACPI	BCS	Show
Advanced Micro Devices	1022	746D	03	0	7	5	AMD-8111™ AC97 Audio	BCS	Show
Advanced Micro Devices	1022	1100	00	0	24	0	HyperTransport™ Technology Config	BCS	Show
Advanced Micro Devices	1022	1101	00	0	24	1	Address Map	BCS	Show
Advanced Micro Devices	1022	1102	00	0	24	2	DRAM Controller/HyperTransport™ Trace Mode	BCS	Show
Advanced Micro Devices	1022	1103	00	0	24	3	Misc Control	BCS	Show
NVIDIA Corporation	10DE	0028	11	1	0	0	NV5 [Riva TnT2]	BCS	Show
Advanced Micro Devices	1022	7464	0B	2	0	0	AMD-8111™ USB	BCS	Show
Advanced Micro Devices	1022	7464	0B	2	0	1	AMD-8111™ USB	BCS	Show
3Com Corporation	10B7	9200	74	2	6	0	3c905C-TX/TX-M [Tornado]	BCS	Show

User can scan system for PCI devices.
In this example only scanning buses 0-10.

Buses to Scan 0-10 Refresh Append To List

start AMD Hardware Debu... Microsoft PowerPoint ... 5:57 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
  - PCI Configuration Registers
  - PCI Configuration Space
  - PCI Device Search
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1					

Refresh

Auto Refresh

PCI Device Search 1

Vendor Name	VID	DID	Rev	Bus	Dev	Fun	Description	Space	Register
Advanced Micro Devices	1022	7454	13	0	0	0	AMD-8151™ System Controller	BCS	Show
Advanced Micro Devices	1022	7455	13	0	1	0	AMD-8151™ AGP Bridge	BCS	Show
Advanced Micro Devices	1022	7460	07	0	6	0	AMD-8111™ PCI	BCS	Show
Advanced Micro Devices	1022	7468	05	0	7	0	AMD-8111™ LPC	BCS	Show
Advanced Micro Devices	1022	7469	03	0	7	1	AMD-8111™ IDE	BCS	Show
Advanced Micro Devices	1022	746A	02	0	7	2	AMD-8111™ SMBus 2.0	BCS	Show
Advanced Micro Devices	1022	746B	05	0	7	3	AMD-8111™ ACPI	BCS	Show
Advanced Micro Devices	1022	746D	03	0	7	5	AMD-8111™ AC97 Audio	BCS	Show
Advanced Micro Devices	1022	1100	00	0	24	0	HyperTransport™ Technology Config	BCS	Show
Advanced Micro Devices	1022	1101	00	0	24	1	Address Map	BCS	Show
Advanced Micro Devices	1022	1102	00	0	24	2	DRAM Controller/HyperTransport™ Trace Mode	BCS	Show
Advanced Micro Devices	1022	1103	00	0	24	3	Misc Control	BCS	Show
NVIDIA Corporation	10DE	0028	11	1	0	0	NV5 [Riva TnT2]	BCS	Show
Advanced Micro Devices	1022	7464	0B	2	0	0	AMD-8111™ USB	BCS	Show
Advanced Micro Devices	1022	7464	0B	2	0	1	AMD-8111™ USB	BCS	Show
3Com Corporation	10B7	9200	74	2	6	0	3c905C-TX/TX-M [Tornado]	BCS	Show

Buses to Scan 0-10 Refresh Append To List

Pressing "Show" for selected device will give a user-friendly view of its PCI Configuration Space. Most, if not all, fields will be separated and labeled.

start AMD Hardware Debu... Microsoft PowerPoint ... 5:57 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

This is the resulting view, which is more user-friendly than the next view, which is primarily a memory dump of the configuration space. Also, the user can easily view other devices.

- Debug
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
  - PCI Configuration Registers
  - PCI Configuration Space
  - PCI Device Search
- Processor Registers

Register	Offset	Value
Vendor ID	00000000	1022
Device ID	00000002	1100
Command	00000004	0000
Status	00000006	0010
Revision ID	00000008	00
Program Interface	00000009	00
Subclass Code	0000000A	00
Base Class Code	0000000B	06
Cache Line Size	0000000C	00
Latency Timer	0000000D	00
Header Type	0000000E	80
BIST	0000000F	00
Base Address Register 0	00000010	00000000
Base Address Register 1	00000014	00000000
Base Address Register 2	00000018	00000000
Base Address Register 3	0000001C	00000000
Base Address Register 4	00000020	00000000
Base Address Register 5	00000024	00000000
CardBus CIS Pointer	00000028	00000000
Subsystem Vendor ID	0000002C	00
Subsystem ID	0000002E	00
Expansion Rom Base Address	00000030	00000000
Capabilities Pointer	00000034	80
Interrupt Line	0000003C	00
Interupt Pin	0000003D	00
Min Grant	0000003E	00
Max Latency	0000003F	00
Routing Table Node 0	00000040	00010101
Routing Table Node 1	00000044	00010101
Routing Table Node 2	00000048	00010101

Refresh | Wr Chgs | Wr All | Bus 0 | Dev 24 | Func 0

start | AMD Hardware Debu... | Microsoft PowerPoint ... | 5:58 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
  - PCI Configuration Registers
  - PCI Configuration Space
  - PCI Device Search
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1					

Refresh

Auto Refresh

PCI Device Search 1 | PCI Configuration Registers 2 | PCI Device Search 2 | **PCI Configuration Space 1**

HyperTransport™ Technology Config

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	22	10	00	11	00	00	10	00	00	00	00	06	00	00	80	00
1	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
2	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
3	00	00	00	00	80	00	00	00	00	00	00	00	00	00	00	00
4	01	01	01	00	01	01	01	00	01	01	01	00	01	01	01	00
5	01	01	01	00	01	01	01	00	01	01	01	00	01	01	01	00
6	00	00	00	00	E4	00	00	00	0F	8C	00	0F	3C	00	00	00
7	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
8	08	00	01	21	20	00	11	11	22	05	75	80	02	00	00	00
9	56	04	51	02	00	00	FF	00	07	00	00	00	00	00	00	00
A	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
B	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
C	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
D	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
E	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
F	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00

View of PCI Configuration Space in memory dump-type view

Refresh | Wr Chgs | Wr All | Bus 0 | Dev 24 | Func 0 | Display Size 8

start | AMD Hardware Debu... | Microsoft PowerPoint ... | 6:00 PM

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12) Processor Registers

HDT Features

- Processor Registers

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- All processor configuration registers (GPRs and MSRs) are defined in this feature group.
- User can copy, paste and find data in cells.
- User can set one or all cell value(s) to zero.
- User use separate window to view and set subfield and bit map for a register value.
- User can set different data display type.
- User can import or export feature data from or to a register binary file.

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
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  - FPU Registers
  - Last Branch Registers
  - MCA Registers
  - Model Specific Registers
  - MTRR Registers
  - Performance Registers
  - Program Registers
  - Segment Registers
  - SEM Registers
  - Single MSR
  - SSE Registers
  - TR & SMM Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1					

Refresh

Auto Refresh

CPU Registers 2

Name	Value
rAX	00000000FFDFFC50
rBX	00000000FFDFF000
rCX	000000000000007E
rDX	0000000083FD44BC
rSP	0000000080539544
rBP	0000000080539550
rSI	0000000080541DA0
rDI	0000000080542000
rFLAG	0000000000000213
rIP	00000000806B2FAA
CR0	8001003B
CR2	00000000E1519000
CR3	0000000000039000
CR4	000006D8
CR8	00000000
R8	0000000000000000
R9	0000000000000000
R10	0000000000000000
R11	0000000000000000
R12	0000000000000000
R13	0000000000000000
R14	0000000000000000
R15	0000000000000000

Node 0 | Core 0 | Refresh | Wr Chgs | Wr All

start | AMD Hardware Debu... | Microsoft PowerPoint ... | 6:04 PM

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File Edit View Features HDT Windows Help

Feature Explorer

- APIC
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  - Segment Registers
  - SEM Registers
  - Single MSR
  - SSE Registers
  - TR & SMM Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1					

Refresh

Auto Refresh

CPU Registers 2 | **Model Specific Registers 1**

Name	Value
Machine Check Addr	00000007A017FEA5
Machine Check Type	0000000000000000
TSC	000000BB2BF890EE
APICBASE	00000000FEE00900
EBL_CR_POWERON	0000000000000000
PatchLevel	0000000000000023
MTRRcap	0000000000000508
SYSENTER_CS	0000000000000008
SYSENTER_ESP	0000000000000000
SYSENTER_EIP	000000008052D480
MCG_CAP	0000000000000105
MCG_STAT	0000000000000000
MCG_CTL	000000000000001F
DBGCTLMSR	0000000000000001
LastBranchFromIP	000000008051801D
LastBranchToIP	00000000806B2FA8
LastIntFromIP	000000008053 4D80
LastIntToIP	000000008053 4FCC
MTRRphysBase0	0000000000000006
MTRRphysMask0	000000FFE0000800
MTRRphysBase1	0000000000000000
MTRRphysMask1	0000000000000000
MTRRphysBase2	0000000000000000
MTRRphysMask2	0000000000000000
MTRRphysBase3	0000000000000000
MTRRphysMask3	0000000000000000
MTRRphysBase4	0000000000000000
MTRRphysMask4	0000000000000000
MTRRphysBase5	0000000000000000
MTRRphysMask5	0000000000000000
MTRRphysBase6	0000000000000000

Node 0 | Core 0 | Refresh | Wr Chgs | Wr All

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File Edit View Features HDT Windows Help

Feature Explorer

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  - Single MSR
  - SSE Registers
  - TR & SMM Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1					

Refresh

Auto Refresh

CPU Registers 2 | Model Specific Registers 1 | MTRR Registers 1 | **TR _SMM Registers 1**

	Selector	Base	Limit	Attribute
GDTR		000000008003F000	000003FF	0082
LDTR	0000	0000000000000000	0000FFFF	0000
IDTR		000000008003F400	000007FF	0082
TR	0028	0000000080042000	000020AB	0089
SMM		000A0000		

Node 0 | Core 0 | Refresh | Wr Chgs | Wr All

start | AMD Hardware Debu... | Microsoft PowerPoint ... | 6:05 PM

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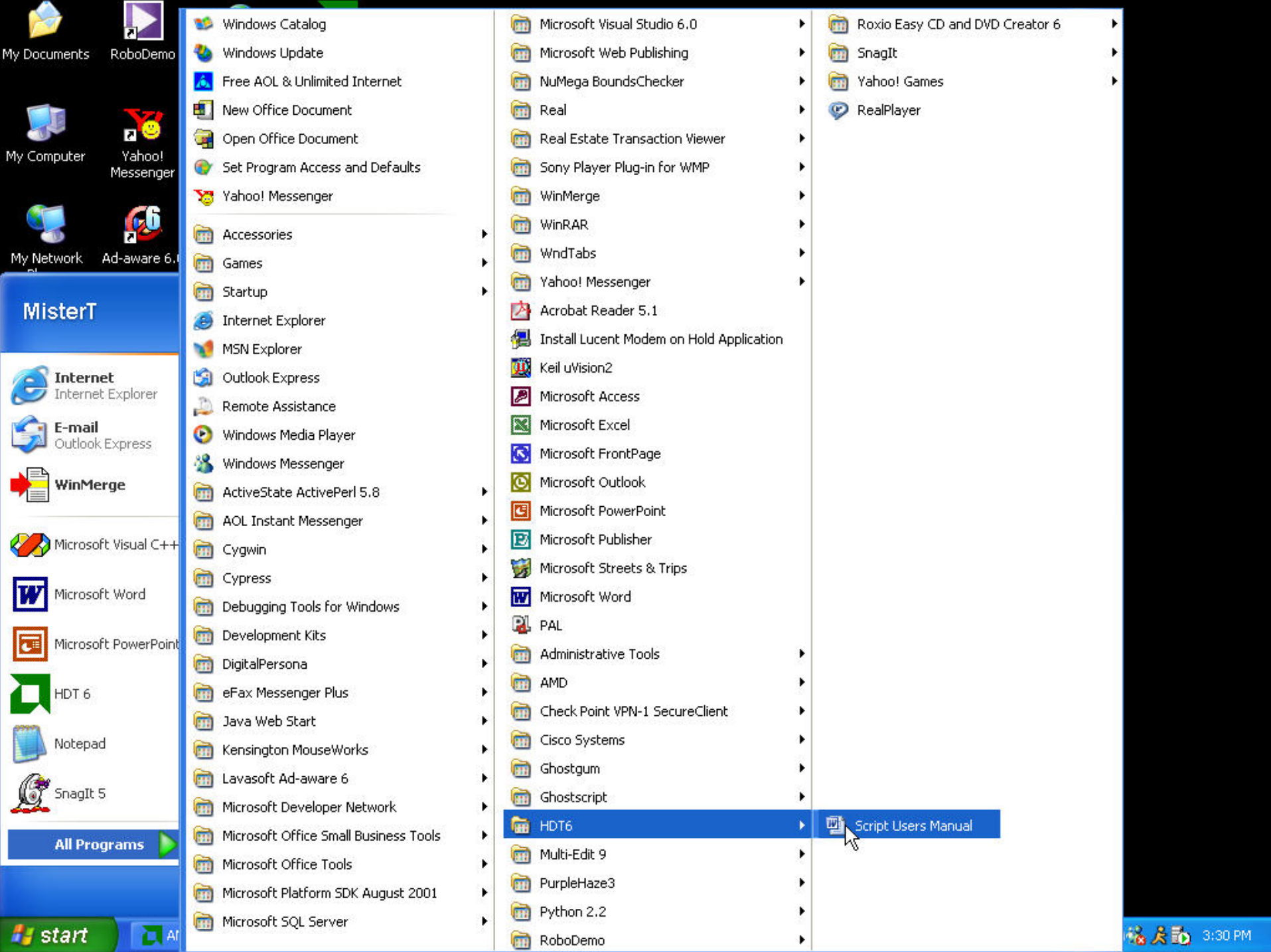
13) Script Console


My Documents
RoboDemo
My Computer
Yahoo! Messenger
My Network
Ad-aware 6.
MisterT
Internet
Internet Explorer
E-mail
Outlook Express
WinMerge
Microsoft Visual C++
Microsoft Word
Microsoft PowerPoint
HDT 6
Notepad
SnagIt 5
All Programs
start
Windows Catalog
Windows Update
Free AOL & Unlimited Internet
New Office Document
Open Office Document
Set Program Access and Defaults
Yahoo! Messenger
Accessories
Games
Startup
Internet Explorer
MSN Explorer
Outlook Express
Remote Assistance
Windows Media Player
Windows Messenger
ActiveState ActivePerl 5.8
AOL Instant Messenger
Cygwin
Cypress
Debugging Tools for Windows
Development Kits
DigitalPersona
eFax Messenger Plus
Java Web Start
Kensington MouseWorks
Lavasoft Ad-aware 6
Microsoft Developer Network
Microsoft Office Small Business Tools
Microsoft Office Tools
Microsoft Platform SDK August 2001
Microsoft SQL Server
Microsoft Visual Studio 6.0
Microsoft Web Publishing
NuMega BoundsChecker
Real
Real Estate Transaction Viewer
Sony Player Plug-in for WMP
WinMerge
WinRAR
WndTabs
Yahoo! Messenger
Acrobat Reader 5.1
Install Lucent Modem on Hold Application
Keil uVision2
Microsoft Access
Microsoft Excel
Microsoft FrontPage
Microsoft Outlook
Microsoft PowerPoint
Microsoft Publisher
Microsoft Streets & Trips
Microsoft Word
PAL
Administrative Tools
AMD
Check Point VPN-1 SecureClient
Cisco Systems
Ghostgum
Ghostscript
HDT6
Multi-Edit 9
PurpleHaze3
Python 2.2
RoboDemo
Roxio Easy CD and DVD Creator 6
SnagIt
Yahoo! Games
RealPlayer
Script Users Manual
3:30 PM

ScriptingUsersManual.rtf - Microsoft Word

File Edit View Insert Format Tools Table Window Help Send

Type a question for help

50% Company Name Times New Roman 30

Final Show

AMD Confidential – Advanced Information

User's Manual for Scripting Features

Hardware Debug Tool

Version 1.3

July, 31th 2003

Advanced Micro Devices

AMD Confidential – Advanced Information

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Draw AutoShapes

Page 1 Sec 1 1/81 At 0.9" Ln 1 Col 1 REC TRK EXT OVR English (U.S

Start D:\amd\GlobaServices\h... AMD HDT for AMD Opter... Workspace 0 ScriptingUsersManual... 2:37 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Show Console

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Technology
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- Instruction Cache Arrays
- JTAG Instructions
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  - Program Registers
  - Segment Registers
  - SEM Registers
  - Single MSR
  - SSE Registers
  - TR & SMM Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	0	n/a	n/a	n/a	n/a	n/a

Refresh

Auto Refresh

Script Console

Console History

>

start AMD Hardware Debu... D:\trash Microsoft PowerPoint ... 3:28 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Load

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Technology
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- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
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  - SSE Registers
  - TR & SMM Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	0	n/a	n/a	n/a	n/a	n/a

Refresh

Auto Refresh

Script Console

Console History

>

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AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
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  - Performance Registers
  - Program Registers
  - Segment Registers
  - SEM Registers
  - Single MSR
  - SSE Registers
  - TR & SMM Registers

Status Info

Run

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	0	n/a	n/a	n/a	n/a	n/a

Refresh

Auto Refresh

Script Console

Console History

>

start AMD Hardware Debu... D:\trash Microsoft PowerPoint ... 3:29 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Record On

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
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- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers
  - CPU Registers
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  - Segment Registers
  - SEM Registers
  - Single MSR
  - SSE Registers
  - TR & SMM Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	0	n/a	n/a	n/a	n/a	n/a

Refresh

☑ Auto Refresh

Script Console

Console History

>

start AMD Hardware Debu... D:\trash Microsoft PowerPoint ... 3:29 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
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  - MTRR Registers
  - Performance Registers
  - Program Registers
  - Segment Registers
  - SEM Registers
  - Single MSR
  - SSE Registers
  - TR & SMM Registers

Status Info

Record Off

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP	Status	L2 Size
0	SH_B0/2-claw-754	0	0	0	n/a	n/a	n/a	n/a	n/a

Refresh

Auto Refresh

Script Console

Console History

>

start AMD Hardware Debu... D:\trash Microsoft PowerPoint ... 3:29 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
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- Memory Debuggers
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	0	n/a	n/a	n/a	n/a	n/a

Refresh

☑ Auto Refresh

Script Console

Console | History

```
>$numCpus = 0;

>hdtPerl::get_number_cpus \$numCpus;

>hdtPerl::write_console "Cpus = $numCpus\n";
Cpus = 1

>
```

start | AMD Hardware Debu... | D:\trash | Microsoft PowerPoint ... | 3:16 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
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- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	0	n/a	n/a	n/a	n/a	n/a

Refresh

☑ Auto Refresh

Script Console

Console History

```
$numCpus = 0;hdtPerl::get_number_cpus \$numCpus;hdtPerl::write_console "Cpus = $numCpus\n";
```

start | AMD Hardware Debu... | D:\trash | Microsoft PowerPoint ... | 3:18 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	0	n/a	n/a	n/a	n/a	n/a

Refresh

☑ Auto Refresh

Script Console

Console History

```
$numCpus = 0;hdtPerl::get_number_cpus \$numCpus;hdtPerl::write_console "Cpus = $numCpus\n";
```

Copy Ctrl+C
Select All Ctrl+A
Print History
Save History
Save History As
Clear History
Start Recording
Stop Recording

start | AMD Hardware Debu... | D:\trash | Microsoft PowerPoint ... | 3:19 PM

Agenda

CONFIDENTIAL

- Introduction to HDT
- Hardware Requirements
- HDT Protocol / Internals
- Exploring the Work Area
- HDT Features
- Practical HDT Scenarios / Examples
- Q&A

Practical HDT Scenarios/Examples

CONFIDENTIAL

1) Debugging from the Boot Vector
2) Using Breakpoints
3) Using Event Trigger

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1) Debugging from the Boot Vector

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Debugging from the Boot Vector Summary

1. Boot/Start Target
2. HDT ON
3. Assert DBReq
4. Warm Reset the Target (Still in HDT Mode)
5. Deassert DBReq
6. Single Step (From line IP to FFF0h)
7. Single Step (Hunt for Southbridge)
8. Single Step (1st jump to boot code)

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Enter HDT debug mode

Feature Explorer

- APIC
- BTHE Debuggers
- Data Cache Arrays
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  - Single MSR
  - SSE Registers
  - TR & SMM Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	0	n/a	n/a	n/a	n/a	n/a

Refresh

Auto Refresh

CPU Registers 2

Name	Value
rAX	0000000000000000
rBX	0000000000000000
rCX	0000000000000000
rDX	0000000000000F40
rSP	0000000000000000
rBP	0000000000000000
rSI	0000000000000000
rDI	0000000000000000
rFLAG	0000000000000002
rIP	00000000000089EF
CR0	00000010
CR2	0000000000000000
CR3	0000000000000000
CR4	00000000
CR8	00000000
R8	0000000000000000
R9	0000000000000000
R10	0000000000000000
R11	0000000000000000

Node 0 Core 0 Refresh Wr Chgs Wr All

After starting/bringing up target system (Step 1), press "HDT ON" (Step 2) to enter HDT Mode.

start AMD Hardware Debu... HDT6Overview.ppt DebugPresentation_I... 1:24 PM

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File Edit View Features HDT Windows Help

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  - Single MSR
  - SSE Registers
  - TR & SMM Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1	0	Legacy 32-bit Mode	BSP	DBReq	1024

Refresh

☑ Auto Refresh

CPU Registers 2

Name	Value
rAX	00000000FFDFFC50
rBX	00000000FFDFF000
rCX	000000000000BC47
rDX	00000000F3DD9102
rSP	00000000805395
rBP	00000000805395
rSI	0000000080541DA0
rDI	0000000080542000
rFLAG	0000000000000217
rIP	00000000806B2FAA
CR0	8001003B
CR2	00000000BF8B08CF
CR3	0000000000039000
CR4	000006D9
CR8	00000000
R8	0000000000000000
R9	0000000000000000
R10	0000000000000000
R11	0000000000000000
R12	0000000000000000
R13	0000000000000000
R14	0000000000000000
R15	0000000000000000

Press "Refresh" to verify that in HDT Mode.

Node 0 | Core 0 | Refresh | Wr Chgs | Wr All

start | AMD Hardware Debu... | HDT6Overview.ppt | DebugPresentation_I... | 1:25 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Assert target DBReq

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debugge
- PCI Configuratio
- Processor Registe
  - CPU Registers
  - Debug Registers
  - FPU Registers
  - Last Branch Registers
  - MCA Registers
  - Model Specific Registers
  - MTRR Registers
  - Performance Registers
  - Program Registers
  - Segment Registers
  - SEM Registers
  - Single MSR
  - SSE Registers
  - TR & SMM Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1	0	Legacy 32-bit Mode	BSP	DBReq	1024

Refresh

Auto Refresh

CPU Registers 2

Name	Value
rAX	00000000FFDFFC50
rBX	00000000FFDFF000
rCX	[illegible]
CR0	8001003B
CR2	00000000BF8B08CF
CR3	0000000000039000
CR4	000006D9
CR8	00000000
R8	0000000000000000
R9	0000000000000000
R10	0000000000000000
R11	0000000000000000
R12	0000000000000000
R13	0000000000000000
R14	0000000000000000
R15	0000000000000000

Press "DBRQ ASRT" (Step 3) asserting the DBReq Signal on the target processor. Then, WARM Reset the target system (Step 4), resulting in the microcode sampling the DBRQ line and halting as a result.

Node 0 | Core 0 | Refresh | Wr Chgs | Wr All

start | AMD Hardware Debu... | HDT6Overview.ppt | DebugPresentation_I... | 1:25 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Assert target DBReq

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  - Model Specific Registers
  - MTRR Registers
  - Performance Registers
  - Program Registers
  - Segment Registers
  - SEM Registers
  - Single MSR
  - SSE Registers
  - TR & SMM Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	1	0	1	0	Legacy 32-bit Mode	BSP	DBReq	1024

Refresh

☑ Auto Refresh

CPU Registers 2

Name	Value
rAX	00000000FFDFFC50
rBX	00000000FFDFF000
rCX	000000000000BC47
rDX	00000000F3DD9102
rSP	
rIP	00000000806B2FAA
CR0	8001003B
CR2	00000000BF8B08CF
CR3	0000000000039000
CR4	000006D9
CR8	00000000
R8	0000000000000000
R9	0000000000000000
R10	0000000000000000
R11	0000000000000000
R12	0000000000000000
R13	0000000000000000
R14	0000000000000000
R15	0000000000000000

Node 0 | Core 0 | Refresh | Wr Chgs | Wr All

User can verify that "DBReq" signal is asserted through "Status Info" window.

start | AMD Hardware Debu... | HDT6Overview.ppt | DebugPresentation_I... | 1:25 PM

AMD Hardware Debug Tool (AMD Confidential)

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Deassert target DBReq

Feature Explorer

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- Debug Utilities
- Download Tools
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- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configu
- Processor Reg
  - CPU Registers
  - Debug Registers
  - FPU Registers
  - Last Branch Registers
  - MCA Registers
  - Model Specific Registers
  - MTRR Registers
  - Performance Registers
  - Program Registers
  - Segment Registers
  - SEM Registers
  - Single MSR
  - SSE Registers
  - TR & SMM Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1	1	Compatible 16-bit Mode	BSP	B0	1024

Refresh

Auto Refresh

CPU Registers 2

Name	Value
rAX	00000000FFDFFC50
rBX	00000000FFDFF000
rCX	000000000000BC47
rDX	00000000F3DD9102
rSP	0000000080539544
rBP	
rIP	00000000806B2FAA
CR0	8001003B
CR2	00000000BF8B08CF
CR3	0000000000039000
CR4	000006D9
CR8	00000000
R8	0000000000000000
R9	0000000000000000
R10	0000000000000000
R11	0000000000000000
R12	0000000000000000
R13	0000000000000000
R14	0000000000000000
R15	0000000000000000

Press "DBRQ DSRT" (Step 5) to De-assert target DBReq.
This is more of a protocol step to bring state.

Node 0 Core 0 Refresh Wr Chgs Wr All

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AMD Hardware Debug Tool (AMD Confidential)

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Feature Explorer

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- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configu
- Processor Reg
  - CPU Registers
  - Debug Registers
  - FPU Registers
  - Last Branch Registers
  - MCA Registers
  - Model Specific Registers
  - MTRR Registers
  - Performance Registers
  - Program Registers
  - Segment Registers
  - SEM Registers
  - Single MSR
  - SSE Registers
  - TR & SMM Registers

Status Info

Single Step Instruction at Architectural CS:rIP

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw 754	0	0	1	1	Compatible 16-bit Mode	BSP	B0	1024

Refresh

Auto Refresh

CPU Registers 2

Name	Value
rAX	00000000FFDFFC50
rBX	00000000FFDFF000
rCX	000000000000BC47
rDX	00000000F3DD9102
rSP	0000000080539544
rBP	
rIP	00000000806B2FAA
CR0	8001003B
CR2	00000000BF8B08CF
CR3	0000000000039000
CR4	000006D9
CR8	00000000
R8	0000000000000000
R9	0000000000000000
R10	0000000000000000
R11	0000000000000000
R12	0000000000000000
R13	0000000000000000
R14	0000000000000000
R15	0000000000000000

Press "SING STEP" for the 1st time (Step 6) to get a RESET VECTOR.

Node 0 | Core 0 | Refresh | Wr Chgs | Wr All

start | AMD Hardware Debu... | HDT6Overview.ppt | DebugPresentation_I... | 1:29 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers
  - CPU Registers
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  - FPU Registers
  - Last Branch Registers
  - MCA Registers
  - Model Specific Registers
  - MTRR Registers
  - Performance Registers
  - Program Registers
  - Segment Registers
  - SEM Regist
  - TR & SMM Registers

Status Info

Single Step Instruction at Architectural CS:rIP

Node					SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1	1	Compatible 16-bit Mode	BSP	B0	1024

Refresh

Auto Refresh

CPU Registers 2

Name	Value
rAX	0000000000000000
rBX	0000000000000000
rCX	0000000000000000
rDX	0000000000000F40
rSP	0000000000000000
rBP	0000000000000000
rSI	0000000000000000
rDI	0000000000000000
rFLAG	0000000000000002
rIP	0000000000000FFF0
CR0	60000010
CR2	0000000000000000
CR3	0000000000000000
CR4	00000000
CR8	00000000
R8	0000000000000000
R13	0000000000000000
R14	0000000000000000
R15	0000000000000000

Remember to press "Refresh" to retrieve target information after Single Stepping.

Node 0 | Core 0 | Refresh | Wr Chgs | Wr All

start | AMD Hardware Debu... | HDT6Overview.ppt | DebugPresentation_I... | 1:30 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Ca
- M
- PCI Co
- Processor Registers
  - CPU Registers
  - Debug Registers
  - FPU Registers
  - Last Branch Registers
  - MCA Registers
  - Model Specific Registers
  - MTRR Registers
  - Performance Registers
  - Program Registers
  - Segment Registers
  - SEM Registers
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  - SSE Registers
  - TR & SMM Registers

Status Info

Single Step Instruction at Architectural CS:rIP

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1	1	Compatible 16-bit Mode	BSP	B0	1024

Refresh

Auto Refresh

CPU Registers 2

Name	Value
rAX	0000000000000000
rBX	0000000000000000
rCX	0000000000000000
rIP	000000000000FFF0
CR0	60000010
CR2	0000000000000000
CR3	0000000000000000
CR4	00000000
CR8	00000000
R8	0000000000000000
R9	0000000000000000
R10	0000000000000000
R11	0000000000000000
R12	0000000000000000
R13	0000000000000000
R14	0000000000000000
R15	0000000000000000

Press "SING STEP" for the 2nd time (Step 7). Remember that this is a hardware step, in which the processor hunts for an attached Southbridge. rIP will not change!

Node 0 | Core 0 | Refresh | Wr Chgs | Wr All

start | AMD Hardware Debu... | HDT6Overview.ppt | DebugPresentation_I... | 1:30 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

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- JTAG Instructions
- L2 Cache Arrays
- Memory D
- PCI C
- Processor
  - CPU Registers
  - Debug Registers
  - FPU Registers
  - Last Branch Registers
  - MCA Registers
  - Model Specific Registers
  - MTRR Registers
  - Performance Registers
  - Program Registers
  - Segment Registers
  - SEM Registers
  - Single MSR
  - SSE Registers
  - TR & SMM Registers

Status Info

Single Step Instruction at Architectural CS:rIP

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-cla 754	0	0	1	1	Compatible 16-bit Mode	BSP	B0	1024

Refresh

Auto Refresh

CPU Registers 2

Name	Value
rAX	0000000000000000
rBX	0000000000000000
rCX	0000000000000000
rDX	0000000000000F40
rIP	0000000000000E05B
CR0	60000010
CR2	0000000000000000
CR3	0000000000000000
CR4	00000000
CR8	00000000
R8	0000000000000000
R9	0000000000000000
R10	0000000000000000
R11	0000000000000000
R12	0000000000000000
R13	0000000000000000
R14	0000000000000000
R15	0000000000000000

Press "SING STEP" for the 3rd and last time (Step 8) to go to the first instruction.

Node 0 Core 0 Refresh Wr Chgs Wr All

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  - Disassembly
  - DRAM Address Translator
  - Memory Dump
  - Target Memory Search
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1	1	Compatible 16-bit Mode	BSP	B0	1024

Refresh

Auto Refresh

CPU Registers 2

Name	Value
rAX	0000000
rBX	000000
rCX	0000000000
rDX	0000000000000F40
rSP	0000000000000000
rBP	0000000000000000
rSI	0000000000000000
rDI	0000000000000000
rFLAG	0000000000000002
rIP	000000000000E05B
CR0	60000010

Node 0 Core 0 Refresh Wr Chgs Wr All

Scenario: Once at BOOT VECTOR, user can bring up a Disassembly window and walk through his/her own code.

Disassembly 2

Address F000:000000000000E05B Addr Type Index

Segment CS Sel Offset rIP + 0000000000000000

Num of Bytes 00000200 Phys Type Auto

Breakpoints

Auto Track CS:rIP

BP	Address	Opcodes	Mnemonic	Code	Size
	F000:000000000000E05B	EA 60 E0 00 F0	jmp	f000:e060h	16
	F000:000000000000E060	8E EA	mov	gs,dx	16
	F000:000000000000E062	66 8B C8	mov	ecx,eax	16
	F000:000000000000E065	B0 A0	mov	al,a0h	16
	F000:000000000000E067	E6 80	out	80h,al	16
	F000:000000000000E069	B0 80	mov	al,80h	16

Node: 0, Core: 0

Node 0 Core 0 Refresh Wr Chgs

start AMD Hardware Debu... HDT6Overview.ppt DebugPresentation_I... 1:31 PM

AMD Hardware Debug Tool (AMD Confidential)

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Single Step Instruction at Architectural CS:rIP

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- Memory Debuggers
  - Disassembly
  - DRAM Address Translator
  - Memory Dump
  - Target Memory Search
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1	1	Compatible 16-bit Mode	BSP	B0	1024

Refresh

Auto Refresh

CPU Registers 2

Name	Value
rAX	0000000000000000
rBX	0000000000000000
rCX	0000000000000000
rDX	0000000000000F40
rSP	0000000000000000
rBP	0000000000000000
rSI	0000000000000000
rDI	0000000000000000
rFLAG	0000000000000002
rIP	000000000000E05B
CR0	60000010

Node 0 Core 0 Refresh Wr Chgs Wr All

Scenario: User can Single Step through code and go line by line

Disassembly 2

Address F000:000000000000E060 Addr Type Index

Segment CS Sel Offset rIP + 0000000000000000

Num of Bytes 00000200 Phys Type Auto

Breakpoints

Auto Track CS:rIP

BP	Address	Opcodes	Mnemonic	Code	Size
	F000:000000000000E05B	EA 60 E0 00 F0	jmp	f000:e060h	16
	F000:000000000000E060	8E EA	mov	gs,dx	16
	F000:000000000000E062	66 8B C8	mov	ecx,eax	16
	F000:000000000000E065	B0 A0	mov	al,a0h	16
	F000:000000000000E067	E6 80	out	80h,al	16
	F000:000000000000E069	B0 80	mov	al,80h	16

Node: 0, Core: 0

Node 0 Core 0 Refresh Wr Chgs

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AMD Hardware Debug Tool (AMD Confidential)

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  - Memory Dump
  - Target Memory Search
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1	1	Compatible 16-bit Mode	BSP	B0	1024

Refresh

☑ Auto Refresh

CPU Registers 2

Name	Value
rAX	0000000000000000
rBX	0000000000000000
rCX	0000000000000000
rDX	0000000000000F40
rSP	0000000000000000
rBP	0000000000000000
rSI	0000000000000000
rDI	0000000000000000
rFLAG	0000000000000002
rIP	000000000000E060
CR0	60000010

Scenario: Don't forget to press "Refresh" to update registers.

Node 0 | Core 0 | Refresh | Wr Chgs | Wr All

Disassembly 2

Address	F000:000000000000E060	Addr Type	Index
Segment	CS Sel	Offset	rIP + 0000000000000000
Num of Bytes	00000200	Phys Type	Auto

Breakpoints

☑ Auto Track CS:rIP

BP	Address	Opcodes	Mnemonic	Code	Size
	F000:000000000000E05B	EA 60 E0 00 F0	jmp	f000:e060h	16
➡	F000:000000000000E060	8E EA	mov	gs,dx	16
	F000:000000000000E062	66 8B C8	mov	ecx,eax	16
	F000:000000000000E065	B0 A0	mov	al,a0h	16
	F000:000000000000E067	E6 80	out	80h,al	16
	F000:000000000000E069	B0 80	mov	al,80h	16

Node: 0, Core: 0

Node 0 | Core 0 | Refresh | Wr Chgs

start | AMD Hardware Debu... | HDT6Overview.ppt | DebugPresentation_I... | 1:32 PM

AMD Hardware Debug Tool (AMD Confidential)

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Single Step Instruction at Architectural CS:rIP

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  - Target Memory Search
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBREQ	Core	DBRDY	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1	1	Compatible 16-bit Mode	BSP	B0	1024

Refresh

Auto Refresh

CPU Registers 2

Name	Value
rAX	0000000000000000
rBX	0000000000000000
rCX	0000000000000000
rDX	0000000000000F40
rSP	0000000000000000
rBP	0000000000000000
rSI	0000000000000000
rDI	0000000000000000
rFLAG	0000000000000002
rIP	000000000000E060
CR0	60000010

Node 0 Core 0 Refresh Wr Chgs Wr All

Disassembly 2

Address	F000:000000000000E062	Addr Type	Index
Segment	CS Sel	Offset	rIP + 0000000000000000
Num of Bytes	00000200	Phys Type	Auto

Breakpoints

Auto Track CS:rIP

BP	Address	Opcodes	Mnemonic	Code	Size
	F000:000000000000E05B	EA 60 E0 00 F0	jmp	f000:e060h	16
	F000:000000000000E060	8E EA	mov	gs,dx	16
➡	F000:000000000000E062	66 8B C8	mov	ecx,eax	16
	F000:000000000000E065	B0 A0	mov	al,a0h	16
	F000:000000000000E067	E6 80	out	80h,al	16
	F000:000000000000E069	B0 80	mov	al,80h	16

Node: 0, Core: 0

Node 0 Core 0 Refresh Wr Chgs

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CONFIDENTIAL

Debugging from the Boot Vector Summary

1. Boot/Start Target
2. HDT ON
3. Assert DBReq
4. Warm Reset the Target (Still in HDT Mode)
5. Deassert DBReq
6. Single Step (From line IP to FFF0h)
7. Single Step (Hunt for Southbridge)
8. Single Step (1st jump to boot code)

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2) Using Breakpoints

AMD Hardware Debug Tool (AMD Confidential)

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  - Event Analyzer
  - ICache Disassembly
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- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1	1	Compatible 16-bit Mode	BSP	B0	1024

Refresh

☑ Auto Refresh

Breakpoints 2

Hardware Breakpoints

	Linear Address		Global Enabled	Transaction Type	Breakpoint Length	Reset BP
DR0	0000000000000080		☑ G0	I/O Read Write	Byte	Clear BP0
DR1	0000000000000000		☐ G1	Instruction Fetc	Byte	Clear BP1
DR2	0000000000000000		☐ G2	Instruction Fetc	Byte	Clear BP2
DR3	0000000000000000		☐ G3	Instruction Fetc	Byte	Clear BP3

☑ GD ☑ Redirect Advanced << Break On SMM Conditional BP << ☐ Write All upon Reset

Software Breakpoints:

Add | Linear Address | Enabled | Action

Remove All

Node 0 Core 0 Refresh Wr Chgs Wr All

User has 4 Hardware Breakpoints to use.

1) Global Enabled – Enables/Disables current breakpoint
2) GD – Breaks into HDT if any access to Debug Registers (DR0-DR7)

3) Redirect – User MUST check this so that when breakpoint is triggered control is "redirected" into HDT.

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  - Cache Line Translator
  - ET Event Analyzer
  - ICache Disassembly
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1	1	Compatible 16-bit Mode	BSP	B0	1024

Refresh

☑ Auto Refresh

Breakpoints 2

Hardware Breakpoints

	Linear Address		Global Enabled	Transaction Type	Breakpoint Length	Reset BP
DR0	0000000000000080		☑ G0	I/O Read Write	Byte	Clear BP0
DR1	0000000000000000		☐ G1	Instruction Fetc	Byte	Clear BP1
DR2	0000000000000000		☐ G2	Instruction Fetc	Byte	Clear BP2
DR3	0000000000000000		☐ G3	Instruction Fetc	Byte	Clear BP3

☑ GD ☑ Redirect Advanced << Break On SMM Conditional BP << ☐ Write All upon Reset

Software Breakpoints:

Add

	Linear Address		Enabled	Action

Remove All

To submit changes, user presses "Wr Chgs" or "Wr All".
For Scenario 1, a breakpoint is set to trigger on any I/O access to port 0x80

Node 0 Core 0 Refresh Wr Chgs Wr All

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AMD Hardware Debug Tool (AMD Confidential)

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Resume operation at current state

Feature Explorer

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- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
  - Disassembly
  - DRAM Addr
- PCI Configura
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1	0	Legacy 16-bit Mode	BSP	B0	1024

Refresh

Auto Refresh

Breakpoints 2

Hardware Breakpoints

	Linear Address		Global Enabled	Transaction Type	Breakpoint Length	Reset BP
DR0	0000000000000080		G0	I/O Read Write	Byte	Clear BP0
DR1	0000000000000000		G1	Instruction Fetc	Byte	Clear BP1
DR2	0000000000000000		G2	Instruction Fetc	Byte	Clear BP2
DR3	0000000000000000		G3	Instruction Fetc	Byte	Clear BP3

GD Redirect Advanced << Break On SMM Conditional BP << Write All upon Reset

Software Breakpoints:

Add Linear Ad

Remove All

Node 0 Core 0 Refresh Wr Chgs Wr All

Once breakpoint is set and written, Exit HDT and wait for breakpoint to get triggered.

Breakpoint is triggered! I/O Access at port 0x80.

Addr Type Index

Segment CS:cs Offset rIP - 0000000000000010

Num of Bytes 00000200 Phys Type Auto

Breakpoints

Auto Track CS:rIP

BP	Address	Opcodes	Mnemonic	Code	Size
	F000:000000000000E065	B0 A0	mov	al,a0h	16
	F000:000000000000E067	E6 80	out	80h,al	16
	F000:000000000000E069	B0 80	mov	al,80h	16
	F000:000000000000E06B	E6 70	out	70h,al	16
	F000:000000000000E06D	FA	cli		16
	F000:000000000000E06E	FC	cld		16

Node: 0, Core: 0

Node 0 Core 0 Refresh Wr Chgs

start AMD Hardware Debu... HDT6Overview.ppt DebugPresentation_I... 1:40 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Resume operation at current state

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
  - Breakpoints
  - Cache Diagnostic Loader
  - Cache Line Translator
  - Event Analyzer
  - ICache Disassembly
- Download Tools
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- I/O Ports
- Instruction Cache Arrays
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- Memory Debuggers
  - Disassembly
  - DRAM Address Translator
  - Memory Dump
  - Target Memory Search
- PCI Configuration
- Processor Registers

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1	0	Legacy 16-bit Mode	BSP	B0	1024

Refresh

Auto Refresh

Breakpoints 2

Hardware Breakpoints

	Linear Address	Global Enabled	Transaction Type	Breakpoint Length	Reset BP
DR0	0000000000000080	G0	I/O Read Write	Byte	Clear BP0
DR1	0000000000000CF8	G1	I/O Read Write	Byte	Clear BP1
DR2	0000000000000000	G2	Instruction Fetc	Byte	Clear BP2
DR3	0000000000000000	G3	Instruction Fetc	Byte	Clear BP3

GD Redirect Advanced << Break On SMM Conditional BP << Write All upon Reset

Software Breakpoints:

Add | Linear Address | Enabled | Action

Remove All

Scenario 2: Breakpoint set to trigger on any access to "Configuration Address Register". Then Exit HDT, allowing system to run.

Disassembly 3

Address F000:

Segment CS Sel Offset rIP

Num of Bytes 00000200 Phys Type Auto

Auto Track CS:rIP

BP	Address	Opcodes	Mnemonic	Code	Size
	F000:000000000000E065	B0 A0	mov	al,a0h	16
	F000:000000000000E067	E6 80	out	80h,al	16
	F000:000000000000E069	B0 80	mov	al,80h	16
	F000:000000000000E06B	E6 70	out	70h,al	16
	F000:000000000000E06D	FA	cli		16
	F000:000000000000E06E	FC	cld		16

Node: 0, Core: 0

Node 0 Core 0 Refresh Wr Chgs

start AMD Hardware Debu... HDT6Overview.ppt DebugPresentation_I... 1:46 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

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- Debug Utilities
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  - Cache Diagnostic Loader
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- L2 Cache Arrays
- Memory Debuggers
  - Disassembly
  - DRAM Address Translator
  - Memory Dump
  - Target Memory Search
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1	0	Legacy 16-bit Mode	BSP	B1	1024

Refresh ☑ Auto Refresh

Breakpoints 2

Hardware Breakpoints

	Linear Address	Global Enabled	Transaction Type	Breakpoint Length	Reset BP
DR0	0000000000000080	☑ G0	I/O Read Write	Byte	Clear BP0
DR1	0000000000000CF8	☑ G1	I/O Read Write	Byte	Clear BP1
DR2	0000000000000000	☐ G2	Instruction Fetc	Byte	Clear BP2
DR3	0000000000000000	☐ G3	Instruction Fetc	Byte	Clear BP3

☑ GD ☑ Redirect Advanced << Break On SMM Conditional BP << ☐ Write All upon Reset

Software Breakpoints:

Add

Remove All

Node 0 Core 0 Refresh Wr Chgs Wr All

Scenario 2: View Disassembly to see where in code "Configuration Address Register" is accessed.

Disassembly 3

Address	F000:000000000000E071	Addr Type	Index
Segment	CS Sel	Offset	rIP - 0000000000000010
Num of Bytes	00000200	Phys Type	Auto

Breakpoints ☑ Auto Track CS:rIP

BP	Address	Opcodes	Mnemonic	Code	Size
	F000:000000000000E076	66 B8 6C C0 00 80	mov	eax,8000c06ch	16
	F000:000000000000E07C	BA F8 0C	mov	dx,0cf8h	16
	F000:000000000000E07F	66 EF	out	dx,eax	16
➡	F000:000000000000E081	83 C2 04	add	dx,04h	16
	F000:000000000000E084	66 ED	in	eax,dx	16
	F000:000000000000E086	8A C8	mov	cl,al	16

Node: 0, Core: 0

Node 0 Core 0 Refresh Wr Chgs

start AMD Hardware Debu... HDT6Overview.ppt DebugPresentation_I... 1:47 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

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  - Memory Dump
  - Target Memory Search
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1	0	Legacy 16-bit Mode	BSP	B1	1024

Refresh

Auto Refresh

There are alternative ways to set breakpoints.
User can Right-Click in Disassembly window and view options.

DR0	0000000000000080	G0			
DR1	0000000000000CF8	G1	I/O Read Write	Byte	Clear BP1
DR2	0000000000000000	G2	Instruction Fetc	Byte	Clear BP2
DR3	0000000000000000	G3	Instruction Fetc	Byte	Clear BP3

GD Redirect Advanced << Break On SMM Conditional BP << Write All upon Reset

Enabled Action

Node 0 Core 0 Refresh Wr Chgs Wr All

Copy
Paste
Find...
Load Ctrl+O
Save As ... Ctrl+S
Print Ctrl+P
Display Opcode Column Alt+F3
Insert HW Breakpoint F9
Enable HW Breakpoint Ctrl+F9
Insert SW Breakpoint Shift+F9
Enable SW Breakpoint Ctrl+Shift+F9
Step Into (Single Step) F8
Step Over Alt+F10
Jump rIP to Next Row
Run to Cursor F7
Properties

0000000E071 Addr Type Index Breakpoints
rIP - 0000000000000010 Auto Track CS:rIP
Auto

Opcodes	Mnemonic	Code	Size
F8 0C	mov	dx,0cf8h	16
EF	out	dx,eax	16
C2 04	add	dx,04h	16
ED	in	eax,dx	16
C8	mov	cl,al	16
F000:000000000000E088 0C 10	or	al,10h	16

Node: 0, Core: 0
Cursor Addr = F000:000000000000E088 = 00000000000FE088 (Phys)
UC/IO@Basic

Node 0 Core 0 Refresh Wr Chgs

start AMD Hardware Debu... HDT6Overview.ppt DebugPresentation_I... 1:48 PM

AMD Hardware Debug Tool (AMD Confidential)

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  - Disassembly
  - DRAM Address Translator
  - Memory Dump
  - Target Memory Search
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1	0	Legacy 16-bit Mode	BSP	B1	1024

Refresh ☑ Auto Refresh

Breakpoints 2

Hardware Breakpoints

	Linear Address	Global Enabled	Transaction Type	Breakpoint Length	Reset BP
DR0	0000000000000080	☑ G0	I/O Read Write	Byte	Clear BP0
DR1	0000000000000CF8	☑ G1	I/O Read Write	Byte	Clear BP1
DR2	00000000000FE088	☑ G2	Instruction Fetc	Byte	Clear BP2
DR3	0000000000000000	☐ G3	Instruction Fetc	Byte	Clear BP3

☑ GD ☑ Redirect Advanced << Break On SMM Conditional BP << ☐ Write All upon Reset

Software Breakpoints:

Add | Linear Address | Enabled | Action

Remove All

Node 0 Core 0 Refresh Wr Chgs Wr All

Disassembly 3

Address F000:000000000000E071 Addr Type Index

Segment CS Sel Offset rIP - 0000000000000010

Num of Bytes 00000200 Phys Type Auto

Breakpoints ☑ Auto Track CS:rIP

BP	Address	Opcodes	Mnemonic	Code	Size
	F000:000000000000E07C	BA F8 0C	mov	dx,0cf8h	16
	F000:000000000000E07F	66 EF	out	dx,eax	16
➡	F000:000000000000E081	83 C2 04	add	dx,04h	16
	F000:000000000000E084	66 ED	in	eax,dx	16
	F000:000000000000E086	8A C8	mov	cl,al	16
●	F000:000000000000E088	0C 10	or	al,10h	16

Node: 0, Core: 0
Cursor Addr = F000:000000000000E088 = 00000000000FE088 (Phys)
UC/IO@Basic

Node 0 Core 0 Refresh Wr Chgs

start | AMD Hardware Debu... | HDT6Overview.ppt | DebugPresentation_I... | 1:49 PM

AMD Hardware Debug Tool (AMD Confidential)

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- JTAG Instructions
- L2 Cache Arrays
- Memory Deb
  - Target Memory
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1	0	Legacy 16-bit Mode	BSP	B1	1024

Refresh ☑ Auto Refresh

Breakpoints 2

Hardware Breakpoints

	Linear Address	Global Enabled	Transaction Type	Breakpoint Length	Reset BP
DR0	0000000000000080	☑ G0	I/O Read Write	Byte	Clear BP0
DR1	0000000000000CF8	☑ G1	I/O Read Write	Byte	Clear BP1
DR2	00000000000FE088	☑ G2	Instruction Fetc	Byte	Clear BP2
DR3	00000000000FE08C	☑ G3	Instruction Fetc	Byte	Clear BP3

☑ GD ☑ Redirect Advanced << Break On SMM Conditional BP << ☐ Write All upon Reset

Software Breakpoints:

Add | Linear Address | Enabled | Action

Node 0 Core 0 Refresh Wr Chgs Wr All

User can enter address manually. In this scenario, a breakpoint is set a few instructions down. Press "Wr Chgs" to submit changes.

Breakpoints

☑ Auto Track CS:rIP

BP	Address	Opcodes	Mnemonic	Code	Size
	F000:000000000000E07C	BA F8 0C	mov	dx,0cf8h	16
	F000:000000000000E07F	66 EF	out	dx,eax	16
	F000:000000000000E081	83 C2 04	add	dx,04h	16
	F000:000000000000E084	66 ED	in	eax,dx	16
	F000:000000000000E085	8A C8	mov	cl,al	16
●	F000:000000000000E087	0C 10	or	al,10h	16
	F000:000000000000E089	66 EF	out	dx,eax	16
	F000:000000000000E08C	66 B8 C0 00 00 80	mov	eax,800000c0h	16
	F000:000000000000E092	83 EA 04	sub	dx,04h	16

Node: 0, Core: 0
Cursor Addr = F000:000000000000E08C = 00000000000FE08C (Phys)
UC/IO@Basic

Node 0 Core 0 Refresh Wr Chgs

start | AMD Hardware Debu... | HDT6Overview.ppt | DebugPresentation_I... | 1:50 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Resume operation at current state

Feature Explorer

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- Mem
  - Disa
  - DRAM Addres
  - Memory Dump
  - Target Memory Search
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1	0	Legacy 16-bit Mode	BSP	B1	1024

Refresh ☑ Auto Refresh

Breakpoints 2

Hardware Breakpoints

	Linear Address	Global Enabled	Transaction Type	Breakpoint Length	Reset BP
DR0	0000000000000080	☑ G0	I/O Read Write	Byte	Clear BP0
DR1	000000000000CF8	☑ G1	I/O Read Write	Byte	Clear BP1
DR2	00000000000FE088	☑ G2	Instruction Fetc	Byte	Clear BP2
DR3	00000000000FE08C	☑ G3	Instruction Fetc	Byte	Clear BP3

☑ GD ☑ Redirect Advanced << Break On SMM Conditional BP << ☐ Write All upon Reset

Core 0 Refresh Wr Chgs Wr All

Red bullet indicates breakpoint has been set.
Exiting HDT to trigger subsequent breakpoints.

Addr Type Index Breakpoints

Segment CS Sel Offset rIP - 0000000000000010

Num of Bytes 00000200 Phys Type Auto ☑ Auto Track CS:rIP

BP	Address	Opcodes	Mnemonic	Code	Size
	F000:000000000000E07C	BA F8 0C	mov	dx,0cf8h	16
	F000:000000000000E07F	66 EF	out	dx,eax	16
➡	F000:000000000000E081	83 C2 04	add	dx,04h	16
	F000:000000000000E084	66 ED	in	eax,dx	16
	F000:000000000000E086	8A C8	mov	cl,al	16
●	F000:000000000000E088	0C 10	or	al,10h	16
	F000:000000000000E08A	66 EF	out	dx,eax	16
●	F000:000000000000E08C	66 B8 C0 00 00 80	mov	eax,800000c0h	16
	F000:000000000000E092	83 EA 04	sub	dx,04h	16

Node: 0, Core: 0
Cursor Addr = F000:000000000000E08C = 00000000000FE08C (Phys)
UC/IO@Basic

Node 0 Core 0 Refresh Wr Chgs

start AMD Hardware Debu... HDT6Overview.ppt DebugPresentation_I... 1:51 PM

AMD Hardware Debug Tool (AMD Confidential)

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  - Disassembly
  - DRAM Address Translator
  - Memory Dump
  - Target Memory Search
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1	0	Legacy 16-bit Mode	BSP	B2	1024

Refresh ☑ Auto Refresh

Breakpoints 2

Hardware Breakpoints

	Linear Address		Global Enabled	Transaction Type	Breakpoint Length	Reset BP
DR0	0000000000000080		☑ G0	I/O Read Write	Byte	Clear BP0
DR1	0000000000000CF8		☑ G1	I/O Read Write	Byte	Clear BP1
DR2	00000000000FE088		☑ G2	Instruction Fetc	Byte	Clear BP2
DR3	00000000000FE08C		☑ G3	Instruction Fetc	Byte	Clear BP3

☑ GD ☑ Redirect Advanced << Break On SMM Conditional BP << ☐ Write All upon Reset

Software Breakpoints:

Add

	Linear Address		Enabled	Action

Node 0 Core 0 Refresh Wr Chgs Wr All

Disassembly 3

Address	F000:000000000000E078		Addr Type	Index	
Segment	CS Sel	Offset	rIP	-	0000000000000010
Num of Bytes	00000200	Phys Type	Auto		

Breakpoints

☑ Auto Track CS:rIP

BP	Address	Opcodes	Mnemonic	Code	Size
	F000:000000000000E07C	BA F8 0C	mov	dx,0cf8h	16
	F000:000000000000E07F	66 EF	out	dx,eax	16
	F000:000000000000E081	83 C2 04	add	dx,04h	16
	F000:000000000000E084	66 ED	in	eax,dx	16
	F000:000000000000E086	8A C8	mov	cl,al	16
	F000:000000000000E088	0C 10	or	al,10h	16
	F000:000000000000E08A	66 EF	out	dx,eax	16
	F000:000000000000E08C	66 B8 C0 00 00 80	mov	eax,800000c0h	16
	F000:000000000000E092	83 EA 04	sub	dx,04h	16

Node: 0, Core: 0
Cursor Addr = F000:000000000000E08C = 00000000000FE08C (Phys)
UC/IO@Basic

Node 0 Core 0 Refresh Wr Chgs

start AMD Hardware Debu... HDT6Overview.ppt DebugPresentation_I... 1:51 PM

CONFIDENTIAL

3) Using Event Trigger

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

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- Memory Debuggers
- PCI Configuration
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Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	1	0	1	0	Legacy 16-bit Mode	BSP	B0	1024

Refresh

☑ Auto Refresh

Breakpoints 1 | Event Analyzer 2

Hardware Breakpoints

	Linear Address		Global Enabled	Transaction Type	Breakpoint Length	Reset BP
DR0	0000000000000080		☑ G0	I/O Read Write	Byte	Clear BP0
DR1	0000000000000000		☐ G1	Instruction Fetc	Byte	Clear BP1
DR2	0000000000000000		☐ G2	Instruction Fetc	Byte	Clear BP2
DR3	0000000000000000		☐ G3	Instruction Fetc	Byte	Clear BP3

☑ GD ☑ Redirect Advanced << Break On SMM Conditional BP << ☐ Write All upon Reset

Software Breakpoints:

Add

	Linear Address		Enabled	Action

Remove All

Node 0 Core 0 Refresh Wr Chgs Wr All

Disassembly 1 | CPU Registers 1

Address	F000:000000000000E081	Addr Type	Index
Segment	CS Sel	Offset	rIP + 0000000000000000
Num of Bytes	00000200	Phys Type	Auto

Breakpoints

☑ Auto Track CS:rIP

BP	Address	Opcodes	Mnemonic	Code	Size
➡	F000:000000000000E081	83 C2 04			16
	F000:000000000000E084				
	F000:000000000000E				
	F000:0000000000				
	F000:0000000000				

Node: 0, Core: 0

Node 0 Core 0 Refresh Wr Chgs

Using the previous example of triggering on port 80h, we'll create something similar to a post card.

start | AMD Hardware Debu... | D:\trash | 1:54 PM

AMD Hardware Debug Tool (AMD Confidential)

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- Memory Debuggers
- PCI Configuration
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Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	1	0	1	0	Legacy 16-bit Mode	BSP	B0	1024

Refresh

☑ Auto Refresh

Breakpoints 1 | Event Analyzer 2

Hardware Breakpoints

	Linear Address		Global Enabled	Transaction Type	Breakpoint Length	Reset BP
DR0	0000000000000080		☑ G0	I/O Read Write	Byte	Clear BP0
DR1	0000000000000000		☐ G1	Instruction Fetc	Byte	Clear BP1
DR2	0000000000000000		☐ G2	Instruction Fetc	Byte	Clear BP2
DR3	0000000000000000		☐ G3	Instruction Fetc	Byte	Clear BP3

☑ GD ☑ Redirect Advanced << Break On SMM Conditional BP << ☐ Write All upon Reset

Software Breakpoints:

Add

	Linear Address		Enabled	Action

Remove All

Node 0 Core 0 Refresh Wr Chgs Wr All

Disassembly 1

Breakpoints

Track CS:rIP

				Size
				16
F000:000000000000E081		in	eax,dx	16
F000:000000000000E086	8A C8	mov	cl,al	16
F000:000000000000E088	0C 10	or	al,10h	16
F000:000000000000E08A	66 EF	out	dx,eax	16

Node: 0, Core: 0

Node 0 Core 0 Refresh Wr Chgs

Reminder: After making any changes, press "Wr Chgs" for those changes to take effect. Press "Refresh" anytime to retrieve TRUE current settings.

start | AMD Hardware Debu... | D:\trash | 1:55 PM

AMD Hardware Debug Tool (AMD Confidential)

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- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers

If: selects the condition to compare against.
"TRUE" means "ALWAYS".
Then: So, for this "TRUE" condition, the "THEN" or "ELSE" case will always be executed.

Breakpoints 1 | Event Analyzer 2

State 1	
If	TRUE
Then	Do Nothing

Current State : 1

Counter 1	Counter 2	Counter 3	Counter 4
0000000000000000	0000000000000000	0000000000000000	0000000000000000
Reset	Reset	Reset	Reset

Force HDT On
Polling DBRdy
Polling Delay : 0 ms
Enable
Reset All Counters

Disassembly 1 | CPU Registers 1

Address	F000:000000000000E081	Addr Type	Index
Segment	CS Sel	Offset	rIP + 0000000000000000
Num of Bytes	00000200	Phys Type	Auto

Breakpoints
Auto Track CS:rIP

BP	Address	Opcodes	Mnemonic	Code	Size
	F000:0000000000000000				16

Reminder: Event Analyzer is a post-processing, HDT software-driven feature. User will now select what steps to take once any access to port 80h causes the system to get in HDT Mode.

Node 0 | Core 0 | Refresh | Wr Chgs

start | AMD Hardware Debu... | D:\trash | 1:55 PM

AMD Hardware Debug Tool (AMD Confidential)

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- Memory Debuggers
- PCI Configuration
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Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	1	0	1	0	Legacy 16-bit Mode	BSP	B0	1024

Refresh

Auto Refresh

Breakpoints 1 | Event Analyzer 2

State 1			
If	TRUE		
Then	Do Nothing		

Current State : 1

Counter 1	Counter 2	Counter 3	Counter 4
0000000000000000	0000000000000000	0000000000000000	0000000000000000
Reset	Reset	Reset	Reset

Force HDT On

Polling DBRdy

Polling Delay : 0 ms

Enable

Reset All Counters

Disassembly 1 | CPU Registers 1

Address	F000:000000000000E081			Addr Type	Index
Segment	CS Sel	Offset	rIP	+	0000000000000000
Num of Bytes	00000200	Phys Type	Auto		

Breakpoints

Auto Track CS:rIP

BP	Address	Opcodes	Mnemonic	Code	Size
	F000:000000000000E081	83 C2 04	add	dx,04h	16
	F000:000000000000E084	66 ED	in	eax,dx	16
	F000:000000000000E086	8A C8	mov	cl,al	16
	F000:000000000000E088	0C 10	or	al,10h	16
	F000:000000000000E08A	66 EF	out	dx,eax	16

Node: 0, Core: 0

Node 0 | Core 0 | Refresh | Wr Chgs

start | AMD Hardware Debu... | D:\trash | 1:55 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

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- JTAG In
- L2 Cach
- Memory
- PCI Con
- Process

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	1	0	1	0	Legacy 16-bit Mode	BSP	B0	1024

Refresh

Auto Refresh

In this example, we're going to increment a "software" counter to keep track of how many times there are accesses to port 80h..

	0	0	TRUE			Rem	Add

Then

Node	Core	Action	Reg/Addr	Item	Data	Mask		
0	0	Do Nothing					Rem	Add

Enter HDT for All
Exit HDT for All
Exit Resume for All
Exit RIP for All
Go to State
Increment Counter

OK Cancel

F000:000000000000E081	83 C2 04	add	dx,04h	16
F000:000000000000E084	66 ED	in	eax,dx	16
F000:000000000000E086	8A C8	mov	cl,al	16
F000:000000000000E088	0C 10	or	al,10h	16
F000:000000000000E08A	66 EF	out	dx,eax	16

Node: 0, Core: 0

Node 0 Core 0 Refresh Wr Chgs

start AMD Hardware Debu... D:\trash 1:56 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
  - Bre
  - Cac
  - Cac
  - ET Eve
  - ICa
- Downlo
- HyperT
- I/O Por
- Instructi
- JTAG In
- L2 Cach
- Memory
- PCI Con
- Process

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	1	0	1	0	Legacy 16-bit Mode	BSP	B0	1024

Refresh

☑ Auto Refresh

Clause Definition

If

	Node	Core	Item	
	0	0	TRUE	Add

User can "Add" (a new row will be added) multiple conditions and "Remove" any incorrect conditions

Then

Node	Core	Action	Reg/Addr	Item	Data	Mask		
0	0	Increment Counter	1				Rem	Add

OK Cancel

F000:000000000000E081	83 C2 04	add	dx,04h	16
F000:000000000000E084	66 ED	in	eax,dx	16
F000:000000000000E086	8A C8	mov	cl,al	16
F000:000000000000E088	0C 10	or	al,10h	16
F000:000000000000E08A	66 EF	out	dx,eax	16

Node: 0, Core: 0

Node 0 Core 0 Refresh Wr Chgs

start AMD Hardware Debu... D:\trash 1:56 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
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- HyperT
- I/O Por
- Instructi
- JTAG In
- L2 Cach
- Memory
- PCI Con
- Process

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	1	0	1	0	Legacy 16-bit Mode	BSP	B0	1024

Refresh

Auto Refresh

For this example, all accesses to port 80h will be written to a user-specified file with information that users can select from (on next page).

Rem Add

Then

Node	Core	Action	Reg/Addr	Item	Data	Mask		
0	0	Increment Counter	1				Rem	Add
0	0	Do Nothing					Rem	Add

Stop
Write to File
Write to GPR
Write to SRB
Write to MSR
Write to I/O (Byte)

OK Cancel

F000:000000000000E081	83 C2 04	add	dx,04h	16
F000:000000000000E084	66 ED	in	eax,dx	16
F000:000000000000E086	8A C8	mov	cl,al	16
F000:000000000000E088	0C 10	or	al,10h	16
F000:000000000000E08A	66 EF	out	dx,eax	16

Node: 0, Core: 0

Node 0 Core 0 Refresh Wr Chgs

start AMD Hardware Debu... D:\trash 1:57 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

Form1

GPR | GPR (Compact) | rIP Only 0 | MSR

Memory Dump — Columns per line 8

Address	0000000000000000	Addr Type	Linear
Segment		Offset	+
Num of Bytes	00000200	Phys Type	Auto
		Display Size	32 bits

Disassembly — Code Size: Auto

Address	0000000000000000	Addr Type	Linear
Segment		Offset	+
Num of Bytes	00000200	Phys Type	Auto

ICache | DCache | L2 Cache | Refresh On Save

Retrieves Data from open Cache Feature windows only

PCI Data — Starting Bus: 0 — Ending Bus: 255 — PCI Config Space

Full Path File Name: — Browse...

OK | Cancel

Size | Refresh | Auto Refresh

Mask | Rem | Add

Node 0 | Core 0 | Refresh | Wr Chgs

start | AMD Hardware Debu... | D:\trash | Form1 | 1:57 PM

User can select what type of information to store with each access to port 80h. GPR(Compact) is a small subset of the general-purpose registers. User can also write PCI-Config Space, MSRs, etc.

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

Form1

GPR GPR (Co

Memory Dump

Address

Segment

Num of Bytes 000002

Disassembly

Address

Segment

Num of Bytes 000002

ICache DCache

Retrieves Data from open Cach

PCI Data Starti

Full Path File Name:

OK Cancel

Save As

Save in: trash

My Recent Documents

Desktop

My Documents

My Computer

My Network Places

Debug
hdt6
LinuxCpuFreqD
ListCtrlDemo
res
_CodingTest[1].doc
~$ntis_word.doc
armsdbapi.zip
cpudump.txt
cpuregdump.txt
david.bat
david.txt
gprcompact
ListCtrlDemo.zip
Mantis_word.doc
msrdump.MSR
MyPropertyCtrl.positions
w2k3sp1_1218_usa_x86fre_spcd.iso

File name: port80access.txt

Save as type:

Save

Cancel

Refresh

Auto Refresh

Rem Add

F000:000000000000E084	66 ED	in	eax,dx	16
F000:000000000000E086	8A C8	mov	cl,al	16
F000:000000000000E088	0C 10	or	al,10h	16
F000:000000000000E08A	66 EF	out	dx,eax	16

Node: 0, Core: 0

Node 0 Core 0 Refresh Wr Chgs

start AMD Hardware Debu... D:\trash Form1 1:58 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

Form1

GPR | GPR (Compact) | rIP Only 0 | MSR

Memory Dump — Columns per line 8

Address	0000000000000000	Addr Type	Linear
Segment		Offset	+
Num of Bytes	00000200	Phys Type	Auto
		Display Size	32 bits

Disassembly — Code Size: Auto

Address	0000000000000000	Addr Type	Linear
Segment		Offset	+
Num of Bytes	00000200	Phys Type	Auto

ICache | DCache | L2 Cache | Refresh On Save

Retrieves Data from open Cache Feature windows only

PCI Data — Starting Bus: 0 — Ending Bus: 255 — PCI Config Space

Full Path File Name: D:\trash\port80access.txt — Browse...

OK | Cancel

Size | Refresh | Auto Refresh

Mask | Rem | Add

F000:000000000000E084	66 ED	in	eax,dx	16
F000:000000000000E086	8A C8	mov	cl,al	16
F000:000000000000E088	0C 10	or	al,10h	16
F000:000000000000E08A	66 EF	out	dx,eax	16

Node: 0, Core: 0

Node 0 | Core 0 | Refresh | Wr Chgs

start | AMD Hardware Debu... | D:\trash | Form1 | 1:58 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
  - Bre
  - Cac
  - Cac
  - ET Eve
  - ICa
- Downlo
- HyperT
- I/O Por
- Instructi
- JTAG In
- L2 Cach
- Memory
- PCI Con
- Process

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	1	0	1	0	Legacy 16-bit Mode	BSP	B0	1024

Refresh

☑ Auto Refresh

Clause Definition

If

	Node	Core	Item	Reg/Addr	Oper	Match Item	Match Reg/Addr	Mask		
	0	0	TRUE						Rem	Add

Then

Node	Core	Action	Reg/Addr	Item	Data	Mask		
0	0	Increment Counter	1				Rem	Add
0	0	Write to File	D:\trash\port80access.txt				Rem	Add
0	0	Do Nothing					Rem	Add

OK Cancel

F000:000000000000E081	83 C2 04	add	dx,04h	16
F000:000000000000E084	66 ED	in	eax,dx	16
F000:000000000000E086	8A C8	mov	cl,al	16
F000:000000000000E088	0C 10	or	al,10h	16
F000:000000000000E08A	66 EF	out	dx,eax	16

Node: 0, Core: 0

Node 0 Core 0 Refresh Wr Chgs

start AMD Hardware Debu... D:\trash 1:58 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	1	0	1	0	Legacy 16-bit Mode	BSP	B0	1024

Refresh

☑ Auto Refresh

Finally, for this example, after collecting the necessary information for this ONE instance, user would need to "Exit" HDT to allow the system to run.

Clause Definition

Then

Node	Core	Action	Reg/Addr	Item	Data	Mask		
0	0	Increment Counter	1				Rem	Add
0	0	Write to File	D:\trash\port80access.txt				Rem	Add
0	0	Do Nothing					Rem	Add

Do Nothing
Enter HDT for All
Exit HDT for All
Exit Resume for All
Exit RIP for All
Go to State

OK Cancel

F000:000000000000E081	83 C2 04	add	dx,04h	16
F000:000000000000E084	66 ED	in	eax,dx	16
F000:000000000000E086	8A C8	mov	cl,al	16
F000:000000000000E088	0C 10	or	al,10h	16
F000:000000000000E08A	66 EF	out	dx,eax	16

Node: 0, Core: 0

Node 0 Core 0 Refresh Wr Chgs

start AMD Hardware Debu... D:\trash 1:59 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
  - Breakpoints
  - Cache Diagnostic Loader
  - Cache Line Translator
  - Event Analyzer
  - ICache Disassembly
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers

Status Info

Node	
0	SH_Bu

User can review conditions that were selected.

Breakpoints 1 | **Event Analyzer 2**

State 1	
If	TRUE
Then	Increment Counter 1 AND Write to File D:\trash\port80access.txt (Node = 0, Core = 0) AND Exit HDT for All Empty

Current State : 1

Counter 1	Counter 2	Counter 3	Counter 4
0000000000000000	0000000000000000	0000000000000000	0000000000000000
Reset	Reset	Reset	Reset

Force HDT On

Polling DBRdy

Polling Delay : 0 ms

Enable

Reset All Counters

Disassembly 1 | CPU Registers 1

Address	F000:000000000000E081		**Addr Type**	Index	
Segment	CS Sel	**Offset**	rIP	+	0000000000000000
Num of Bytes	00000200	**Phys Type**	Auto		

Breakpoints

Auto Track CS:rIP

BP	Address	Opcodes	Mnemonic	Code	Size
	F000:000000000000E081	83 C2 04	add	dx,04h	16
	F000:000000000000E084	66 ED	in	eax,dx	16
	F000:000000000000E086	8A C8	mov	cl,al	16
	F000:000000000000E088	0C 10	or	al,10h	16
	F000:000000000000E08A	66 EF	out	dx,eax	16

Node: 0, Core: 0

Node 0 | Core 0 | Refresh | Wr Chgs

start | AMD Hardware Debu... | D:\trash | 1:59 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
  - Breakpoints
  - Cache Diagnostic Loader
  - Cache Line Translator
  - Event Analyzer
  - ICache Disassembly
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	1	0	1	0	Legacy 16-bit Mode	BSP	B0	1024

Refresh

Auto Refresh

Breakpoints 1 | Event Analyzer 2

If	TRUE
Then	Increment Counter 1 And Empty

Pressing "Enable" will Exit HDT.

Current State : 1

Counter 1	Counter 2	Counter 3	Counter 4
0000000000000000	0000000000000000	0000000000000000	0000000000000000
Reset	Reset	Reset	Reset

Force HDT On

Polling DBRdy

Polling Delay : 10 ms

Enable

Reset All Counters

Disassembly 1 | CPU Registers 1

Address	F000:000000000000E081	Addr Type	Index
Segment	CS Sel	Offset	rIP + 0000000000000000
Num of Bytes	00000200	Phys Type	Auto

Breakpoints

Auto Track CS:rIP

BP	Address	Opcodes	Mnemonic	Code	Size
	F000:000000000000E081	83 C2 04	add	dx,04h	16
	F000:000000000000E084	66 ED	in	eax,dx	16
	F000:000000000000E086	8A C8	mov	cl,al	16
	F000:000000000000E088	0C 10	or	al,10h	16
	F000:000000000000E08A	66 EF	out	dx,eax	16

Node: 0, Core: 0

Node 0 | Core 0 | Refresh | Wr Chgs

start | AMD Hardware Debu... | D:\trash | 2:00 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
  - Breakpoints
  - Cache Diagnostic Loader
  - Cache Line Translator
  - Event Analyzer
  - ICache Disassembly
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1	0	Legacy 16-bit Mode	BSP	B0	1024

Refresh

Auto Refresh

Breakpoints 1 | Event Analyzer 2

State 1			
If	TRUE	T	
Then	Increment Counter 1 AND Write to File D:\trash\port80access.txt (Node = 0, Core = 0) AND Exit HDT for All Empty		

Current State : 1

Counter 1		Counter 4
000000000000000C	00000	00000000000000
Reset		Reset

Force HDT On

Polling DBRdy

Polling Delay 20 ms Disable

Reset All Counters

Event Analyzer Timer

Elapsed time: 24 seconds

Disable

Disassembly 1 | CPU Registers 1

Address	F000:0000000000006224			Addr Type	Index
Segment	CS Sel	Offset	rIP	+	0000000000000000
Num of Bytes	00000200	Phys Type	Auto		

Breakpoints

Auto Track CS:rIP

BP	Address	Opcodes	Mnemonic	Code	Size
	F000:000000000000E615	BC 1B E6	mov	sp,e61bh	16
	F000:000000000000E618	E9 00 02	jmp	loc e81bh	16
	F000:000000000000E61B	1D E6 0B	sbb	ax,0be6h	16
	F000:000000000000E61E	F6 74 41	div	byte [si+41h]	16
	F000:000000000000E621	8B DE	mov	bx,si	16

Node: 0, Core: 0

Node 0 Core 0 Refresh Wr Chgs

start AMD Hardware Debu... D:\trash 2:28 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debug
- Data Cache A
- Debug Utilities
  - Breakpoir

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size	Refresh

D:\trash

File Edit View Favorites Tools Help

Back Search Folders

port80access.txt - Notepad

File Edit Format View Help Send

```
General Register (Compact)
rIP              rAX              rBX              rCX              rDX              rSP              rBP
000000000000E067 00000000000000A0 0000000000000000 0000000000000000 0000000000000F40 0000000000000000 000000000000000C
000000000000E069 00000000000000A0 0000000000000000 0000000000000000 0000000000000F40 0000000000000000 000000000000000C
000000000000E1EF 00000000FEE001A2 0000000000000824 000000000000001B 0000000000000000 0000000000000000 000000000000000C
000000000000E26C 00000000FEE009AA 0000000000000824 000000000000001B 0000000000000000 0000000000000000 000000000000000C
000000000000E278 0000000000000FAB 0000000000000824 0000000000000000 00000000078BFBFF 000000000000E274 000000000000000C
000000000000E292 00000000000000A4 0000000000000000 000000000000017B 0000000000000000 000000000000E280 000000000000000C
000000000000E2A6 00000000000004A5 0000000000000824 00000000C0010048 0000000000000000 000000000000E2A2 000000000000000C
000000000000E2AD 00000000000061A6 0000000000000824 00000000C0010000 000000000000002E 000000000000E2A2 000000000000000C
000000000000E89D 00000000000061CF 0000000000000824 00000000C0010000 000000000000E522 000000000000E895 000000000000000C
000000000000E8A1 00000000000061CF 0000000000000824 00000000C0010000 000000000000E522 000000000000E895 000000000000000C
000000000000E33C 0000000080003BC0 000000000000E32B 00000000C0013B43 0000000000000CFF 000000000000D7DB 000000000000000C
000000000000E615 00000000800FFC1 000000000000E32B 00000000C0010000 0000000000000090 000000000000E5FE 000000000000000C
000000000000006224 00000000000000C1 0000000000000000 0000000000000000 0000000000000080 000000000000E660 000000000000000C
000000000000E799 000000000000000C 000000000000F0000 0000000000000000 0000000000004000 000000000000E00 000000000002000C
000000000000E7D2 000000000000CDC3 000000000000F0000 0000000000000000 0000000000004000 000000000000E00 000000000002000C
000000000000E801 00000000000050C5 0000000000189B25 00000000008F9318 0000000000023000 0000000000000DFE 000000000002000C
00000000000082C0 0000000016161601 000000000018EE1A 00000000C0010001 0000000016161616 0000000000000EFE 000000000020100
```

Text file output of accesses to port 80h.

start AMD Hardware Debu... D:\trash port80access.txt - N... 2:30 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
  - Breakpoints
  - Cache Diagnostic Loader
  - Cache Line Translator
  - Event Analyzer
  - ICache Disassembly
- Download Tools
- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	1	0	Legacy 16-bit Mode	BSP	B0	1024

Refresh

Auto Refresh

Breakpoints 1 | Event Analyzer 2

Hardware Breakpoints

	Linear Address	Global Enabled	Transaction Type	Breakpoint Length	Reset BP
DR0	0000000000000CF8	G0	I/O Read Write	Byte	Clear BP0
DR1	0000000000000000	G1	Instruction Fetc	Byte	Clear BP1
DR2	0000000000000000	G2	Instruction Fetc	Byte	Clear BP2
DR3	0000000000000000	G3	Instruction Fetc	Byte	Clear BP3

GD Redirect Advanced << Break On SMM Conditional BP << Write All upon Reset

Software Breakpoints:

Add | Linear Address | Enabled | Action

Remove All

Node 0 Core 0 Refresh Wr Chgs Wr All

Disassembly 1 | CPU Registers 1

Address F000:0000000000000E095 Addr Type Index

Segment CS Sel Offset rIP + 0000000000000000

Breakpoints

Auto Track CS:rIP

F000:0000000000000E09A ... 16

Node: 0, Core: 0

Node 0 Core 0 Refresh Wr Chgs

start AMD Hardware Debu... D:\trash 2:40 PM

Another practical example would be to trigger on all accesses to the Config Address Register and dump register contents into a file to see when and what is being written.

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
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  - Cache Line Translator
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  - ICache Disassembly
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- HyperTransport™ Technology
- I/O Ports
- Instruction Cache Arrays
- JTAG Instructions
- L2 Cache Arrays
- Memory Debuggers
- PCI Configuration
- Processor Registers

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	0	n/a	n/a	n/a	n/a	n/a

Refresh

Auto Refresh

Breakpoints 1 | Event Analyzer 2

State 1			
If	TRUE	T	
Then	Increment Counter 1 AND Write to File D:\trash\ConfigAddressPortAccess.txt (Node = 0, Core = 0) AND Exit HDT for All Empty		

Current State : 1

Counter 1		Counter 4
000000000000000C	00000	00000000000000
Reset		Reset

Force HDT On

Polling DBRdy

Polling Delay 20 ms

Disable

Reset All Counters

Event Analyzer Timer

Elapsed time: 34 seconds

Disable

Disassembly 1 | CPU Registers 1

Address	F000:000000000000D9B4			Addr Type	Index
Segment	CS Sel	Offset	rIP	+	0000000000000000
Num of Bytes	00000200	Phys Type	Auto		

Breakpoints

Auto Track CS:rIP

BP	Address	Opcodes	Mnemonic	Code	Size
	F000:000000000000D9B4	83 C2 04	add	dx,04h	16
	F000:000000000000D9B7	66 8B C3	mov	eax,ebx	16
	F000:000000000000D9BA	66 EF	out	dx,eax	16
	F000:000000000000D9BC	66 B8 01 00 00 00	mov	eax,00000001h	16
	F000:000000000000D9C2	0F A2	cpuid		16

Node: 0, Core: 0

Node 0 | Core 0 | Refresh | Wr Chgs

start | AMD Hardware Debu... | D:\trash | 2:42 PM

AMD Hardware Debug Tool (AMD Confidential)

File Edit View Features HDT Windows Help

Feature Explorer

- APIC
- BTHB Debuggers
- Data Cache Arrays
- Debug Utilities
  - Breakpoints

Status Info

Node	CPU Name	DBReq	Core	DBRdy	SMM	Operating Mode	BSP/AP	#DB Status	L2 Size
0	SH_B0/2-claw-754	0	0	0	n/a	n/a	n/a	n/a	n/a

Refresh

Auto Refresh

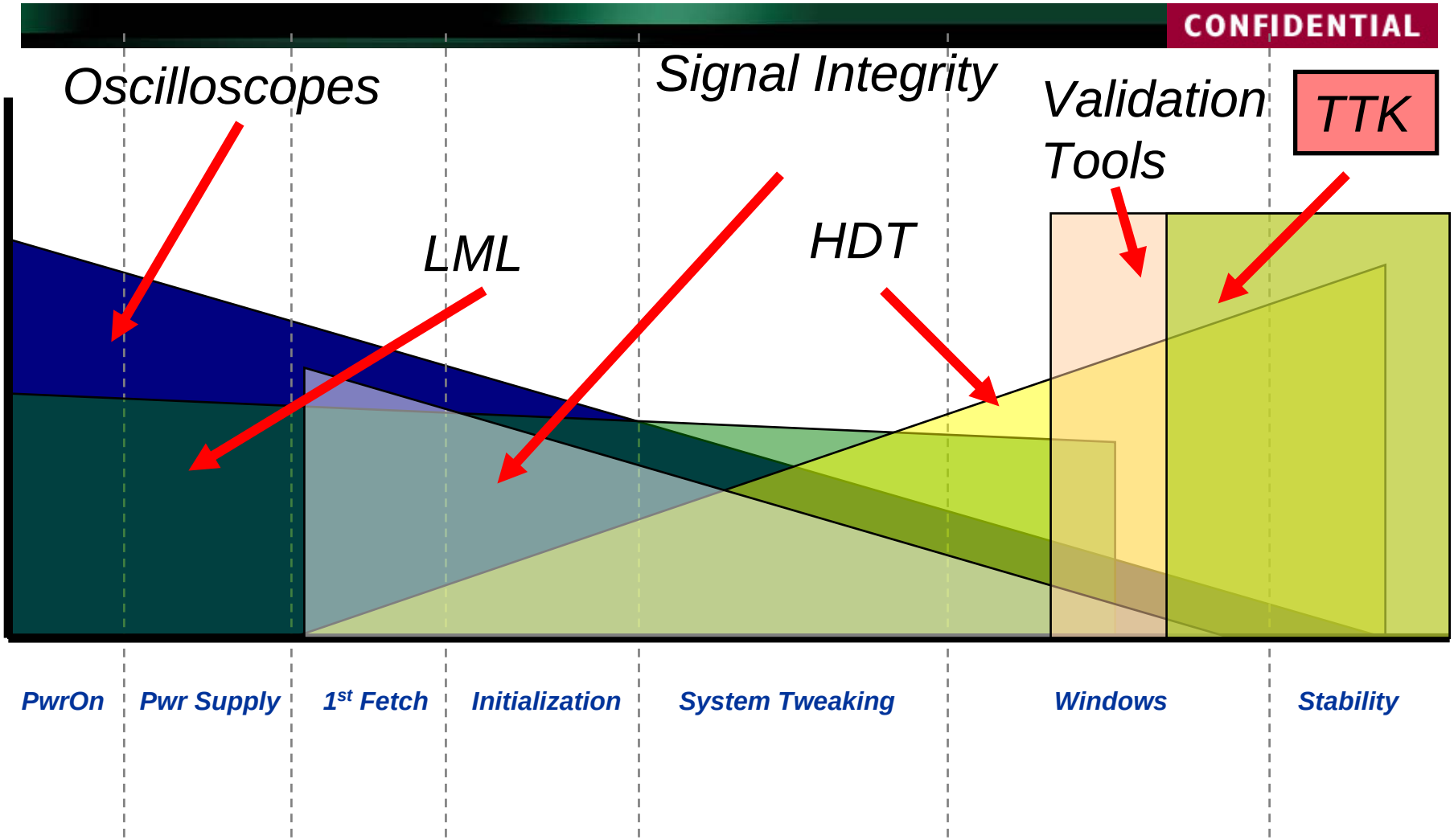
ConfigAddressPortAccess.txt - Notepad

File Edit Format View Help Send

```
General Register (Compact)
rIP              rAX              rBX              rCX              rDX              rSP              rBP
000000000000E095 00000000800000C0 0000000000000000 000000000000000D 0000000000000CF8 0000000000000000 000000000000000C
000000000000E097 00000000800000C0 0000000000000000 000000000000000D 0000000000000CF8 0000000000000000 000000000000000C
000000000000E0AB 0000000080000874 0000000000000000 000000000000000D 0000000000000CF8 0000000000000000 000000000000000C
000000000000E0BA 00000000800040C0 0000000000000000 000000000000000D 0000000000000CF8 0000000000000000 000000000000000C
000000000000E17A 000000008000C290 0000000000000824 0000000000000000 00000000078B0CF8 0000000000000000 000000000000000C
000000000000E1A2 000000008000C3D4 0000000000000824 00000000C0011022 0000000000000CF8 0000000000000000 000000000000000C
000000000000E1B8 000000008000C3D8 0000000000000824 00000000C0011022 0000000000000CF8 0000000000000000 000000000000000C
000000000000E1CE 000000008000C094 0000000000000824 00000000C0011022 0000000000000CF8 0000000000000000 000000000000000C
000000000000D973 000000008000C06C 0000000000000824 000000000000001B 0000000000000CF8 00000000E2720000 000000000000000C
000000000000D988 000000008000C06C 000000000000001C 000000000000001B 0000000000000CF8 00000000E2720000 000000000000000C
000000000000D99B 000000008000C068 000000000000001C 000000000000001B 0000000000000CF8 00000000E2720000 000000000000000C
000000000000D9B4 000000008000C068 000000000F008000 000000000000001B 0000000000000CF8 00000000E2720000 000000000000000C
```

start | AMD Hardware Debu... | D:\trash | ConfigAddressPortAc... | 2:43 PM

Board Development Timeline



AMD

CONFIDENTIAL

Development & Debug Tools Overview

Please refer all questions to:

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Q & A

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