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SFF Committee

SFF-8679

Specification for

QSFP28 4X Base Electrical Specification

Rev 1.7 August 12, 2014

Secretariat: SFF Committee

Abstract: This specification defines the contact pads, the electrical (copper), the power supply, the ESD and the thermal characteristics of the pluggable QSFP10/14/28 Module/Direct Attach cable plug and connector.

This document provides a common specification for systems manufacturers, system integrators, and suppliers. This is an internal working document of the SFF Committee, an industry ad hoc group.

This specification is intended to supersede and extend INF-8438 QSFP (Quad SFP) 4 Gb/s 4X Transceiver and SFF-8436 QSFP+ 10 Gb/s 4X Pluggable Transceiver by adding support for higher transfer rates and higher power classes.

This specification is made available for public review, and written comments are solicited from readers. Comments received by the members will be considered for inclusion in future revisions of this specification.

Support: This specification is supported by the identified member companies of the SFF Committee.

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EXPRESSION OF SUPPORT BY MANUFACTURERS

The following member companies of the SFF Committee voted in favor of this industry specification.

Avago
EMC
Finisar
Foxconn
HGST
MGE
Molex
NetApp
Oclaro
Panduit
TE Connectivity
Volex

The following member companies of the SFF Committee voted against this industry specification.

Hewlett Packard

The following member companies of the SFF Committee voted to abstain on this industry specification.

Amphenol
Dell Computer
IBM
LSI
Luxshare-ICT
Pioneer
Sandisk
Seagate
Toshiba

Change History

Rev 1.5:
- Moved referenced SFF specs to 2.1 Industry Documents and expanded the list.

Rev 1.6:
- Updated Figure 1 to show retimers.
- Removed two-wire interface timing diagram which is now in SFF-8636.
- Complete rewrite of power supply section to add support for power classes 5 to 7.
- Added section 8 "Timing Requirements".

Rev 1.7
- Editorial only, no technical changes.

Foreword

The development work on this specification was done by the SFF Committee, an industry group. The membership of the committee since its formation in August 1990 has included a mix of companies which are leaders across the industry.

When 2 1/2" diameter disk drives were introduced, there was no commonality on external dimensions e.g. physical size, mounting locations, connector type, and connector location, between vendors.

The first use of these disk drives was in specific applications such as laptop portable computers and system integrators worked individually with vendors to develop the packaging. The result was wide diversity, and incompatibility.

The problems faced by integrators, device suppliers, and component suppliers led to the formation of the SFF Committee as an industry ad hoc group to address the marketing and engineering considerations of the emerging new technology.

During the development of the form factor definitions, other activities were suggested because participants in the SFF Committee faced more problems than the physical form factors of disk drives. In November 1992, the charter was expanded to address any issues of general interest and concern to the storage industry. The SFF Committee became a forum for resolving industry issues that are either not addressed by the standards process or need an immediate solution.

> Those companies which have agreed to support a specification are identified in the first pages of each SFF Specification. Industry consensus is not an essential requirement to publish an SFF Specification because it is recognized that in an emerging product area, there is room for more than one approach. By making the documentation on competing proposals available, an integrator can examine the alternatives available and select the product that is felt to be most suitable.

SFF Committee meetings are held during T10 weeks (see www.t10.org), and Specific Subject Working Groups are held at the convenience of the participants. Material presented at SFF Committee meetings becomes public domain, and there are no restrictions on the open mailing of material presented at committee meetings.

Most of the specifications developed by the SFF Committee have either been incorporated into standards or adopted as standards by EIA (Electronic Industries Association), ANSI (American National Standards Institute) and IEC (International Electro technical Commission).

If you are interested in participating or wish to follow the activities of the SFF Committee, the signup for membership and/or documentation can be found at:

www.sffcommittee.com/ie/join.html

The complete list of SFF Specifications which have been completed or are currently being worked on by the SFF Committee can be found at:

ftp://ftp.seagate.com/sff/SFF-8000.TXT

If you wish to know more about the SFF Committee, the principles which guide the activities can be found at:

ftp://ftp.seagate.com/sff/SFF-8032.TXT

Suggestions for improvement of this specification will be welcome. They should be sent to

the SFF Committee, 14426 Black Walnut Ct, Saratoga, CA 95070.

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FIGURES

TABLES

SFF Committee --

QSFP28 4X Base Electrical Specification

1 Scope

This document specifies the electrical requirements for the QSFP10/14/28 pluggable 4-lane interfaces, hereafter referred to as QSFP28. The scope includes: electrical contacts for the host connector; fiber positions for optical interfaces; power supply requirements; ESD and thermal characteristics of pluggable QSFP28 modules and direct attach cables. The mechanical requirements are specified by reference.

This specification supersedes and extends the applications supported by INF-8438 QSFP (Quad SFP) 4 Gb/s 4X Transceiver and SFF-8436 QSFP28 10 Gb/s 4X Pluggable Transceiver by supporting higher transfer rates.

2 References

2.1 Industry Documents

The following interface standards and specifications are relevant to this Specification.

- GR-253-CORE
- ESD specifications EN61000-4-2, JEDEC JESD22-A114-B
- Optical Connectors: MPO:IEC 61754-7, Dual LC: IEC 61754-20
- Aligned key (Type B) MPO patch cords: TIA-568
- Dual LC optical patch cord: TIA/EIA-604-10A
- Thermal specifications: NEBS GR-63
- IEEE Std 802.3-2012, 802.3bj and 802.3bm
- InfiniBand Architecture Specifications FDR and EDR
- INCITS 479-2011 FC-PI-5 (Fibre Channel Physical Interface -5)
- INCITS 512-2014 FC-PI-6 (Fibre Channel Physical Interface -6)
- T10 2212-D SAS-3
- T11-533-201x FC-PI-6P (Fibre Channel Physical Interface -6 128GFC Four Lane Parallel)
- SFF-8635 QSFP+ 10 Gb/s 4X Pluggable Transceiver Solution (QSFP10)
- SFF-8665 QSFP+ 28 Gb/s 4X Pluggable Transceiver Solution (QSFP28)
- SFF-8685 QSFP+ 14 Gb/s 4X Pluggable Transceiver Solution (QSFP14)

2.2 SFF Specifications

There are several projects active within the SFF Committee. The complete list of specifications which have been completed or are still being worked on are listed in the specification at ftp://ftp.seagate.com/sff/SFF-8000.TXT. The specifications relevant to the various QSFP generations are listed below.

INF-8438	QSFP (Quad Small Formfactor Pluggable) Transceiver
SFF-8024	SFF Committee Cross Reference to Industry Products
SFF-8436	QSFP+ 10 Gbs 4X Pluggable Transceiver - Standardized as EIA-964
SFF-8635	QSFP+ 10 Gb/s 4X Pluggable Transceiver Solution (QSFP10)
SFF-8636	Common Management Interface
SFF-8661	QSFP+ 28 Gb/s 4X Pluggable Module
SFF-8662	QSFP+ 28 Gb/s 4X Connector (Style A)
SFF-8663	QSFP+ 28 Gb/s Cage (Style A)
SFF-8665	QSFP+ 28 Gb/s 4X Pluggable Transceiver Solution (QSFP28)
SFF-8672	QSFP+ 28 Gb/s 4X Connector (Style B)
SFF-8679	QSFP+ 4X Base Electrical Specification
SFF-8682	QSFP+ 14 Gb/s 4X Connector (Style B)
SFF-8683	QSFP28 14 Gb/s Cage

2.3 Sources

Those who join the SFF Committee as an Observer or Member receive electronic copies of the minutes and SFF specifications (http://www.sffcommittee.com/ie/join.html).

Copies of ANSI standards may be purchased from the InterNational Committee for Information Technology Standards (http://www.techstreet.com/incitsgate.tmpl).

2.4 Conventions

The ISO convention of numbering is used i.e., the thousands and higher multiples are separated by a space and a period is used as the decimal point. This is equivalent to the English/American convention of a comma and a period.

American	French	ISO
0.6	0,6	0.6
1,000	1 000	1 000
1,323,462.9	1 323 462,9	1 323 462.9

2.5 Acronyms

The following acronyms are used in this specification.

ANSI	American National Standards Institute
ASIC	Application Specific Integrated Circuit
ATM	Asynchronous Transfer Mode
CML	Current Mode Logic
CORE	Central Office Relay Equipment
DC	Direct Current
DDR	Double Data Rate
EDR	Enhanced Data Rate
EIA	Electronic Industries Alliance
EMI	Electro Magnetic Interference
ESD	Electro Static Discharge
FC	Fibre Channel
FDR	Fourteen Data Rate
Gb/s	Gigabits per second
GbE	Gigabit Ethernet
GFC	Gigabit Fibre Channel
HCB	Host Compliance Board
IEC	International Electrotechnical Commission
IEEE	Institute for Electrical and Electronics Engineers
ISO	Organization for International Standards
ITU	International Telecommunications Union
JEDEC	Joint Electron Device Engineering Council
kHz	kiloHertz
km	kilometer
LVCMOS	Low Voltage Complementary Metal Oxide Semiconductor
LVTTL	Low Voltage Transistor Transistor Logic
MCB	Module Compliance Board
MHz	MegaHertz
MIB	Management Information Base
MPO	Multi-fiber Push On
MSA	Multiple Source Agreement
NAS	Network-Attached Storage
NAT	Network Address Translation
NEBS	Network Equipment Building System
OC	Optical Carrier
OEM	Original Equipment Manufacturer

OMA	Open Mobile Alliance
PCB	Printed Circuit Board
PDH	Plesiochronous Digital Hierarchy
PI	Physical Interface
PON	Passive Optical Network
QDR	Quad Data Rate
QSFP	Quad SFP
Rx	Receiver
SAS	Serial Attached SCSI
SDH	Synchronous Digital Hierarchy
SDR	Software Defined Receiver
SerDes	Serializer-Deserializer
SFP	Small Formfactor Pluggable
SM	Single Mode
SNMP	Simple Network Management Protocol
SONET	Synchronous Optical NETwork
STM	Synchronous Transfer Mode
TIA	Telecommunications Industry Association
TTL	Transistor-Transistor Logic
Tx	Transmitter
XFP	10 Gigabit Small Formfactor Pluggable

3 General Description

This specification covers the following items:

a) Electrical specification. including connector contact assignments for data control, status, configuration and test signals) and the electrical connector and recommended host PCB layout requirements.
b) Mechanical and board definition.
c) Environmental and thermal. requirements (case temperatures). Electromagnetic interference (EMI) recommendations (including necessary shielding features to seal the OEM chassis front panel output with and without the module installed in the cage). Electrostatic discharge (ESD) requirements solely to the extent disclosed in the specification where the sole purpose of such disclosure is to enable products to operate, connect or communicate as defined within the specifications.
d) Timing requirements.

The overall package dimension shall conform to the required dimensions and tolerances.

- The mounting features shall be located such that the products are mechanically interchangeable with the cage and connector system.

- The overall dimensions and mounting requirements for the cage and connector system on a circuit board shall be configured such that the products are mechanically and electrically interchangeable.

- The overall dimensions and insertion requirements for the optical connector and corresponding fiber optic cable plug shall be such that the products are mechanically and optically interchangeable.

These electrical and optical specifications may be compatible with those enumerated in the following:

ITU-T Recommendation G.957	STM-1, STM-4, STM-16
Telcordia Technologies GR-253-CORE	OC-3, OC-12, OC-48, OC-192
Ethernet IEEE 802.3	10 GbE, 40 GbE, 100 GbE
Infiniband Architecture Specifications	SDR, DDR, QDR, FDR, EDR
SFF Committee	SFF-8436 QSFP+
Fibre Channel	FC-PI-3/4/5/6, 2G, 4G, 8G, 10G, 16G, 32G

The specifications will provide a common solution for combined four-channel ports that support SONET/SDH and/or Ethernet and/or Infiniband and/or Fibre Channel and/or SAS specifications. This specification encompasses design(s) capable of supporting multimode and single mode modules, passive copper, active copper and active optical cables.

An Application Reference Model, See Figure 3-1, shows the high-speed data interface between an ASIC (SerDes) and the module. Only one data channel of the interface is shown for simplicity. Either parallel MPO or duplex LC fiber connectors can be used for the optical interface.

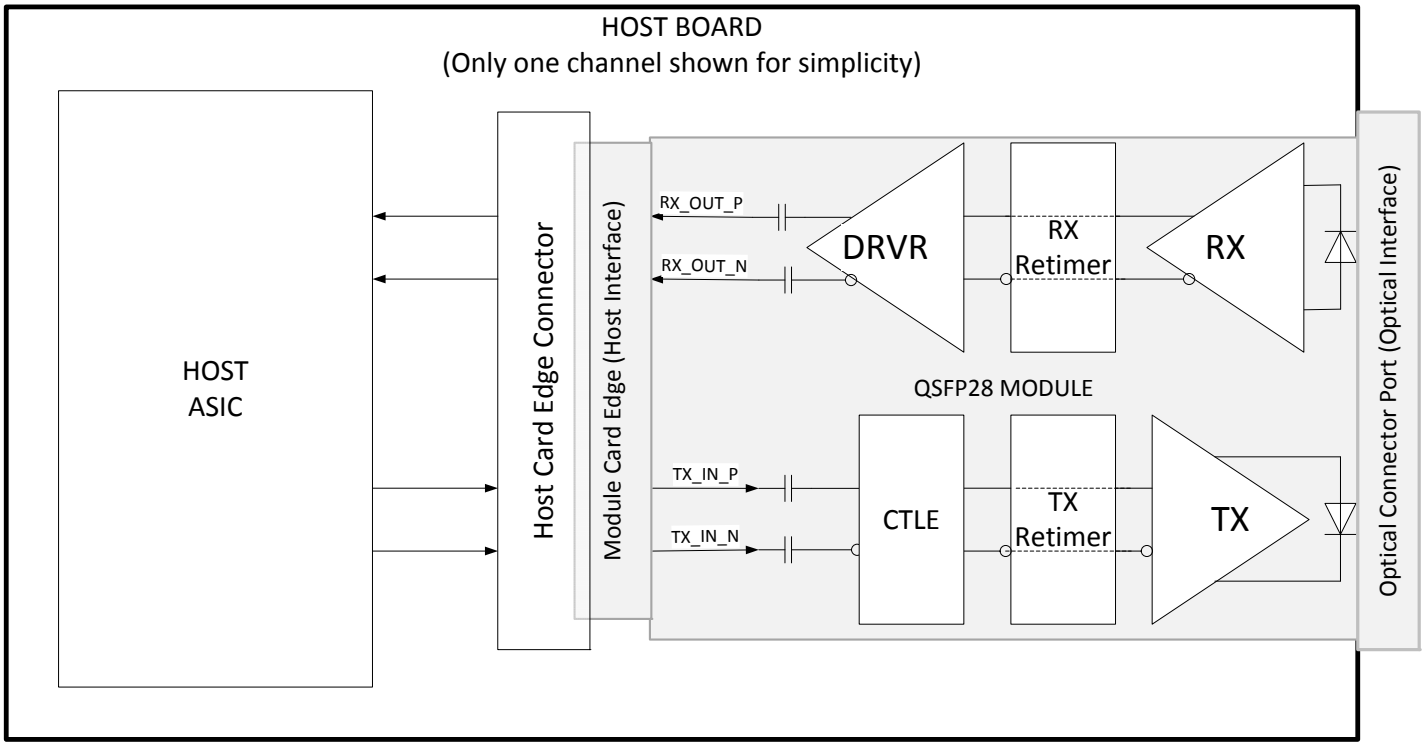


FIGURE 3-1 APPLICATION REFERENCE MODEL

4 Compliance Testing

The module electrical interface test points are intended to be measured using compliance boards as shown in Figure 4-1. These compliance boards are intended to connect the module under test to test equipment for verification of compliance to the appropriate standard. The Module Compliance Board is used to test the module. The electrical parameters of the compliance boards should be specified by the appropriate standard. The Module Compliance Board and Host Compliance Board can be plugged together for calibration of compliance signals and to check the electrical parameters of the compliance boards.

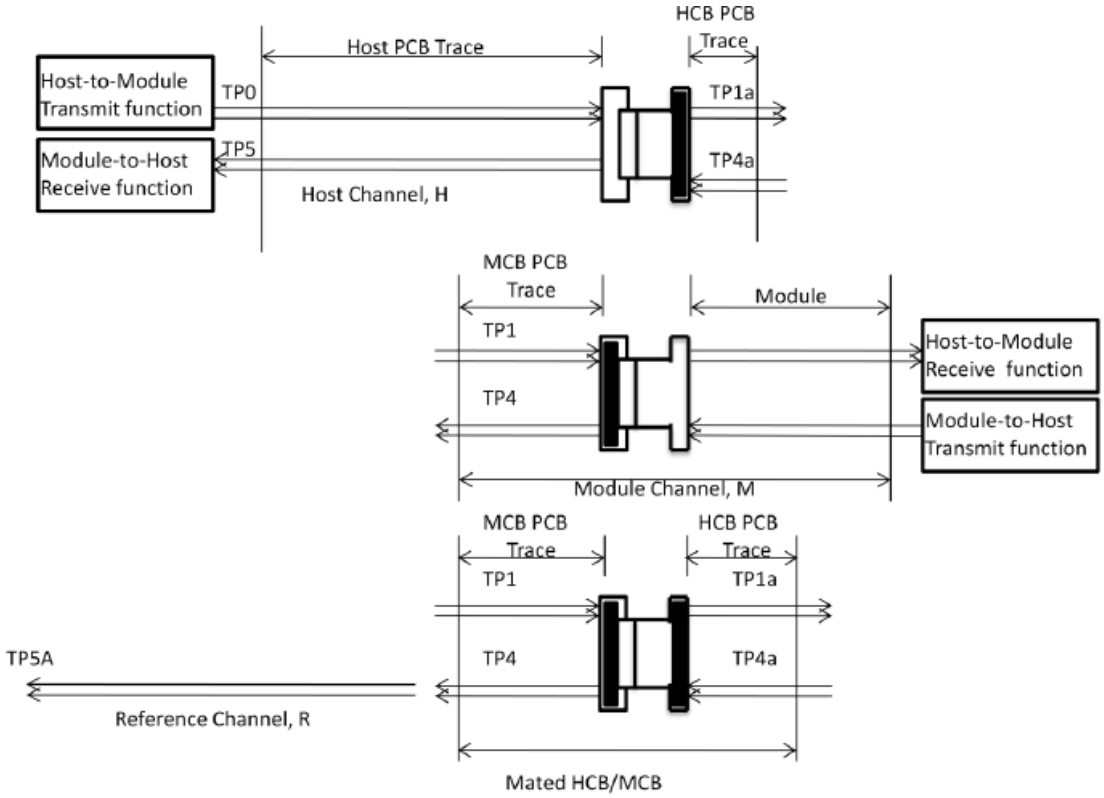


FIGURE 4-1 REFERENCE POINTS AND COMPLIANCE BOARDS

The reference points are defined in Table 4-1.

TABLE 4-1 REFERENCE POINTS

TP0	Host ASIC transmitter output at ASIC package pin on a DUT board
TP1	Input to module compliance board through mated module compliance board and module connector. Used to test module input
TP1A	Host ASIC transmitter output across the Host Board and Host Edge Card connector at the output of the host compliance board
TP4	Module output through mated module and host edge card connector through module compliance board
TP4A	Input to host compliance board through mated host compliance board and host edge card connector. Used to test host input
TP5	Input to host ASIC
Note:	Individual standards may specify unique reference points

5 Electrical Specification

This clause contains pin definition data for the module. The pin definition data is generic for gigabit-per-second datacom applications such as Fibre Channel, Ethernet and SONET/ATM applications. Compliance Points for high-speed signal electrical measurements are defined in Figure 4-1. Compliance Points for all other electrical signals are at comparable points at the host edge card connector.

5.1 Electrical Connector

Figure 5-1 shows the signal symbols and contact numbering for the module edge connector. The diagram shows the module PCB edge as a top and bottom view. There are 38 contacts intended for high speed signals, low speed signals, power and ground connections. Table 5-1 provides more information about each of the 38 contacts.

The module contains a printed circuit board that mates with the electrical connector. The pads are designed for a sequenced mating:

First mate - ground contacts
Second mate - power contacts
Third mate - signal contacts

For EMI protection the signals to the connector should be shut off when the module is removed. Standard board layout practices such as connections to Vcc and GND with Vias, use of short and equal-length differential signal lines, use of microstrip-lines and 50 Ohm terminations are recommended. The chassis ground (case common) of the module should be isolated from the module's circuit ground, GND, to provide the equipment designer flexibility regarding connections between external electromagnetic interference shields and circuit ground, GND, of the module.

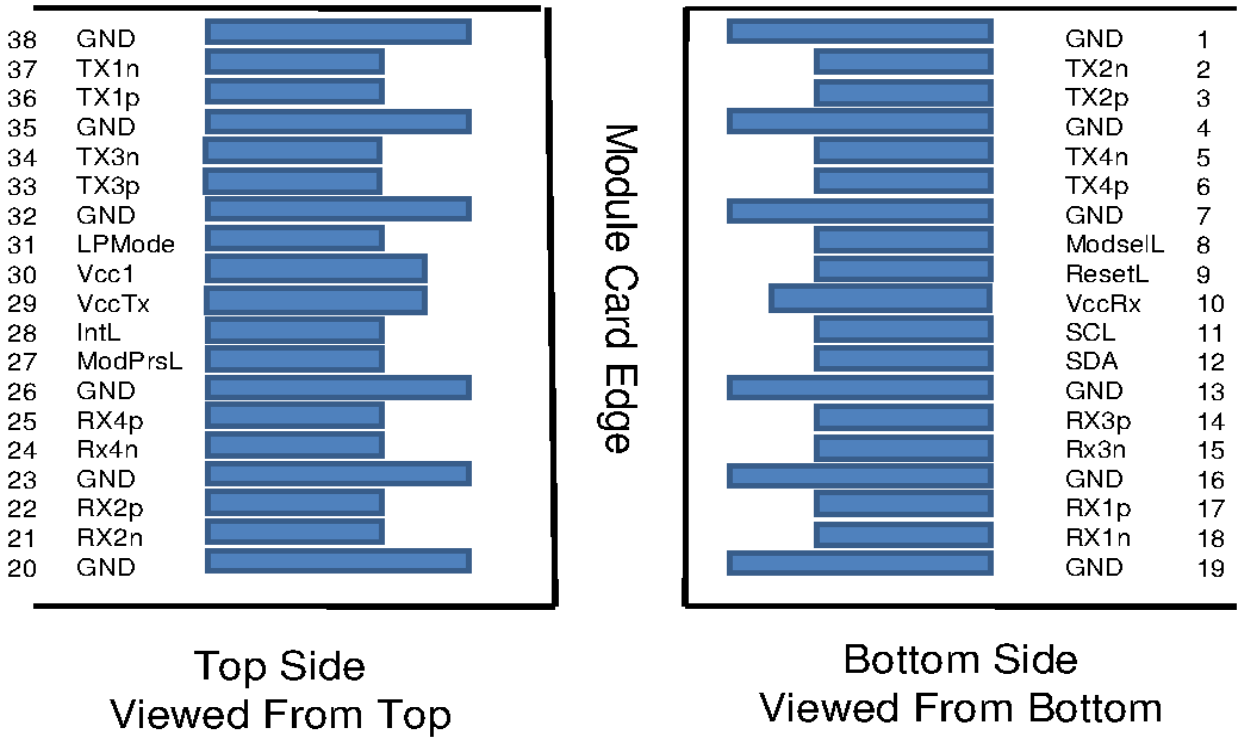


FIGURE 5-1 MODULE PAD LAYOUT

TABLE 5-1 PIN FUNCTION DEFINITION

Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	1
8	LVTTL-I	ModSelL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		Vcc Rx	+3.3V Power Supply Receiver	2	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3	
13		GND	Ground	1	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL	Interrupt	3	
29		Vcc Tx	+3.3V Power supply transmitter	2	2
30		Vcc1	+3.3V Power supply	2	2
31	LVTTL-I	LPMode	Low Power Mode	3	
32		GND	Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	1
Note 1: GND is the symbol for signal and supply (power) common for the module. All are common within the module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.					
Note 2: Vcc Rx, Vcc1 and Vcc Tx shall be applied concurrently. Requirements defined for the host side of the Host Edge Card Connector are listed in Table 5-6. Vcc Rx Vcc1 and Vcc Tx may be internally connected within the module in					

any combination. The connector pins are each rated for a maximum current of 1000 mA.

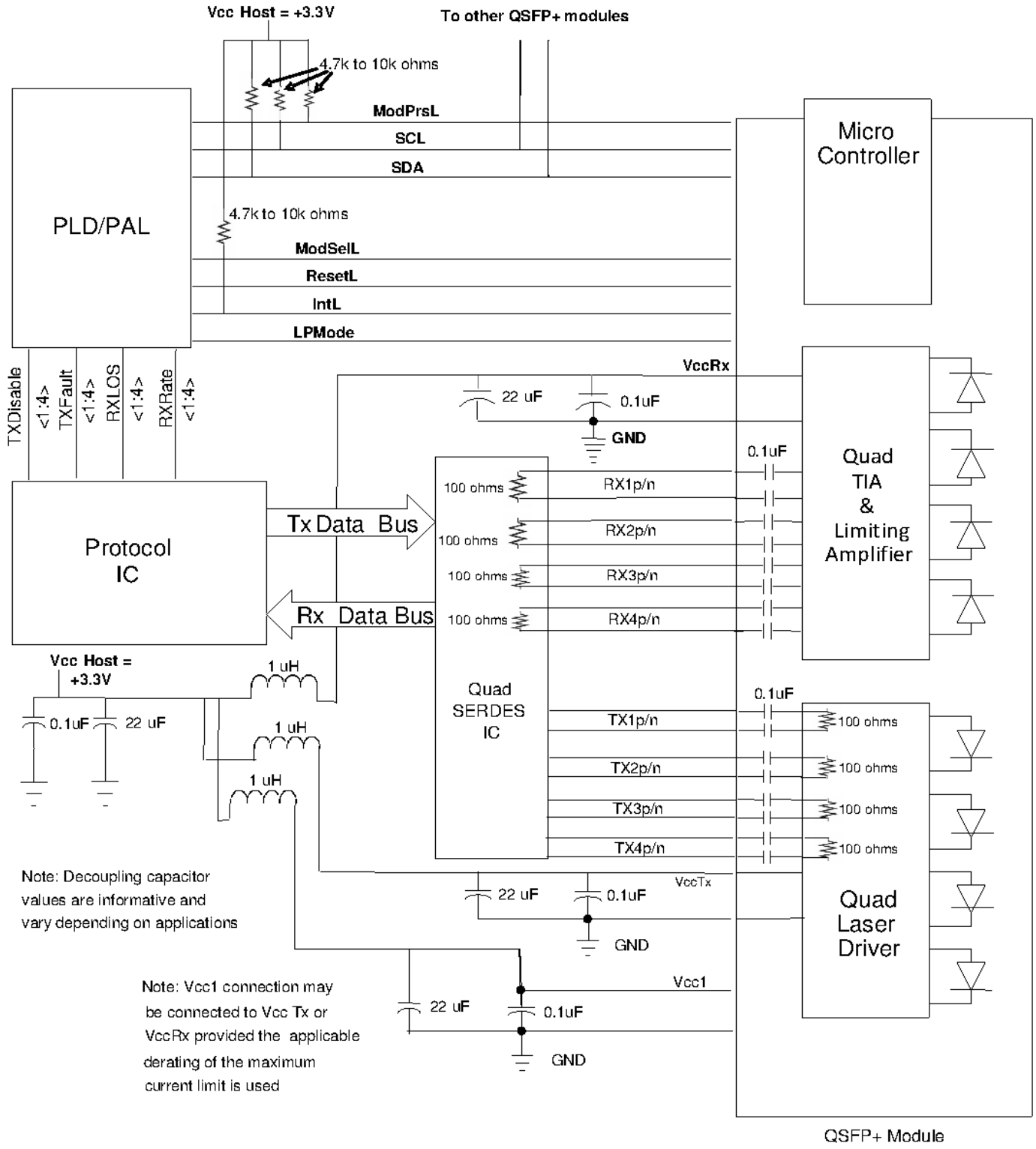


FIGURE 5-2 EXAMPLE: HOST BOARD SCHEMATIC FOR OPTICAL MODULES

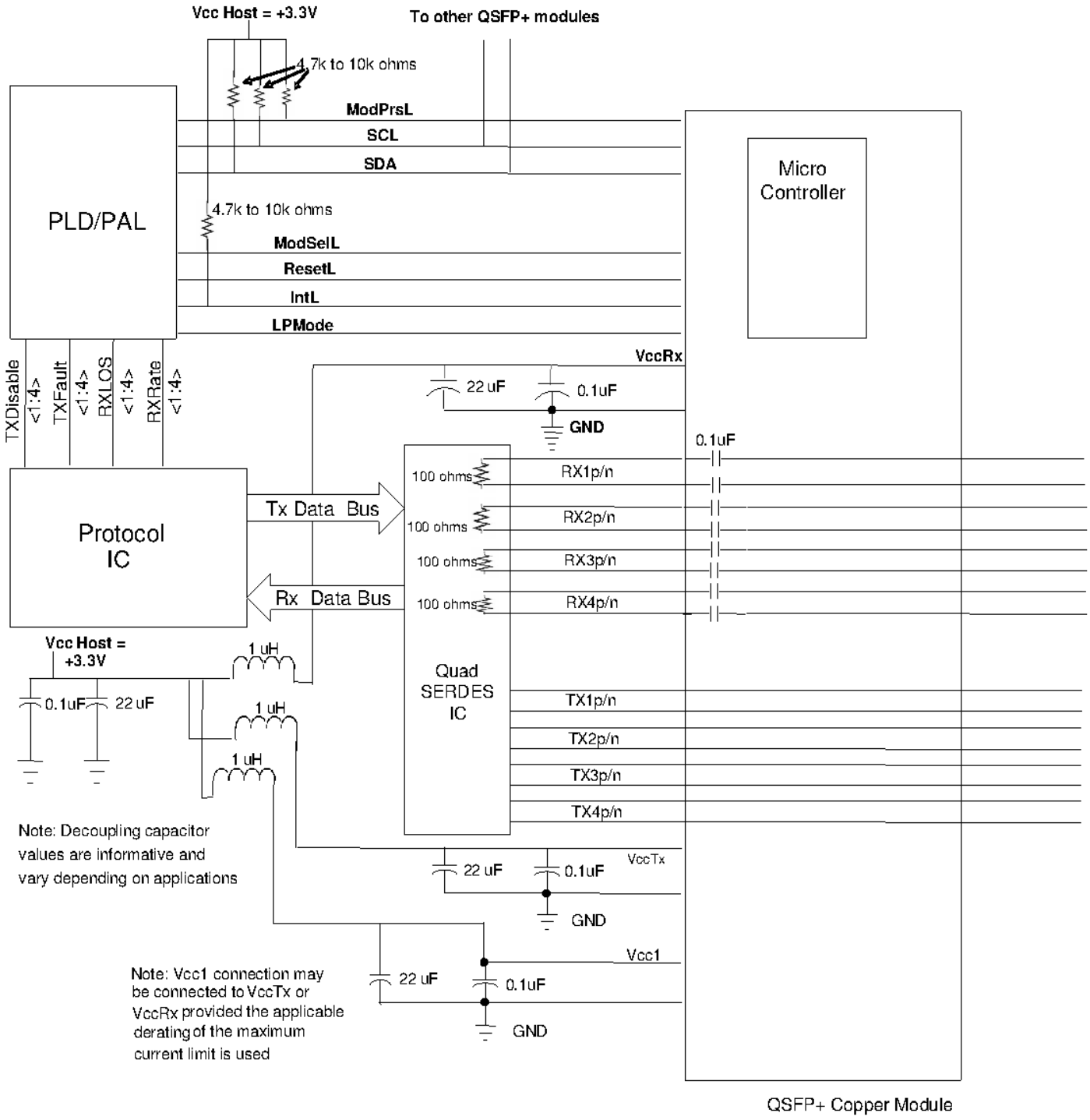


FIGURE 5-3 EXAMPLE: HOST BOARD SCHEMATIC FOR PASSIVE COPPER CABLES

5.2 Low Speed Pin Descriptions

In addition to the 2-wire serial interface the module has the following low speed pins for control and status:

ModSelL
ResetL
LPMode
ModPrsL
IntL

5.2.1 ModSelL

The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple modules on a single 2-wire interface bus. When the ModSelL is "High", the module shall not respond to or acknowledge any 2-wire interface communication from the host. ModSelL signal input node shall be biased to the "High" state in the module.

In order to avoid conflicts, the host system shall not attempt 2-wire interface communications within the ModSelL de-assert time after any modules are deselected. Similarly, the host shall wait at least for the period of the ModSelL assert time before communicating with the newly selected module. The assertion and de-asserting periods of different modules may overlap as long as the above timing requirements are met.

5.2.2 ResetL

The ResetL pin shall be pulled to Vcc in the module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_init) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by asserting "low" an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset.

5.2.3 LPMode

The LPMode pin shall be pulled up to Vcc in the module. The pin is a hardware control used to put modules into a low power mode when high. By using the LPMode pin and a combination of the Power_override, Power_set and High_Power_Class_Enable software control bits (Address A0h, byte 93 bits 0,1,2), the host controls how much power a module can dissipate.

See section 5.5 for more details on the power supply specifications.

5.2.4 ModPrsL

ModPrsL is pulled up to Vcc_Host on the host board and grounded in the module. The ModPrsL is asserted "Low" when inserted and deasserted "High" when the module is physically absent from the host connector.

5.2.5 IntL

IntL is an output pin. When IntL is "Low", it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an open collector output and shall be pulled to host supply voltage on the host board. The INTL pin is deasserted "High" after completion of reset, when byte 2 bit 0 (Data Not Ready) is read with a value of '0' and the flag field is read (see SFF-8636).

5.3 Low Speed Pin Electrical Specifications

5.3.1 Low Speed Signaling

Low speed signaling other than SCL and SDA is based on Low Voltage TTL (LVTTL) operating at Vcc. Vcc refers to the generic supply voltages of VccTx, VccRx, Vcc_host or Vcc1. Hosts shall use a pull-up resistor connected to Vcc_host on each of the 2-wire interface SCL (clock), SDA (data), and all low speed status outputs.

The SCL and SDA is a hot plug interface that may support a bus topology. During module insertion or removal, the module may implement a pre-charge circuit which prevents corrupting data transfers from other modules that are already using the bus.

Compliance with Table 5-3 provides compatibility between host bus masters and the 2-wire interface.

TABLE 5-2 LOW SPEED PIN ELECTRICAL SPECIFICATIONS

Parameter	Symbol	Min	Max	Unit	Condition
SCL and SDA	VOL	0	0.4	V	IOL(max)=3.0mA
	VOH	Vcc-0.5	Vcc+0.3	V	
SCL and SDA	VIL	-0.3	Vcc*0.3	V	
	VIH	VCC*0.7	Vcc + 0.5	V	
Capacitance for SCL and SDA I/O pin	Ci		14	pF	
Total bus capacitive load for SCL and SDA	Cb		100	pF	3.0 k Ohms pullup resistor, max
			200	pF	1.6 k Ohms pullup resistor max
LPMode, Reset and ModSelL	VIL	-0.3	0.8	V	|Iin|<=125 uA for 0V<Vin,Vcc
	VIH	2	VCC+0.3	V	
ModPrsL and IntL	VOL	0	0.4	V	IOL=2.0mA
	VOH	VCC-0.5	VCC+0.3	V	

5.3.2 Low Speed Pin Timing

Timing for SCL, SDA and ModSelL is defined in the common management interface document SFF-8636. Timing of the hardware control functions is specified in section 8.

5.4 High Speed Pin Electrical Specifications

5.4.1 Rx(n)(p/n)

Rx(n)(p/n) are module receiver data outputs. Rx(n)(p/n) are AC-coupled 100 Ohm differential lines that should be terminated with 100 Ohm differentially at the Host ASIC(SerDes). The AC coupling is inside the module and not required on the Host board. For operation at 28 Gb/s the relevant standards (e.g., OIF CEI v3.1) define the signal requirements on the high-speed differential lines. For operation at lower rates, refer to the relevant standards.

Note: Due to the possibility of insertion of legacy QSFP and QSFP+ modules into a host designed for higher speed operation, it is recommended that the damage threshold of the host input be at least 1600 mV peak to peak differential.

Output squelch for loss of optical input signal, hereafter Rx Squelch, is required and shall function as follows. In the event of the optical signal on any channel becoming equal to or less than the level required to assert LOS, then the receiver data output for that channel shall be squelched or disabled. In the squelched or disabled state output impedance levels are maintained while the differential voltage swing shall be less than

50 mVpp.

In normal operation the default case has Rx Squelch active. Rx Squelch can be deactivated using Rx Squelch Disable through the 2-wire serial interface. Rx Squelch Disable is an optional function. For specific details refer to SFF-8636.

5.4.2 Tx(n)(p/n)

Tx(n)(p/n) are module transmitter data inputs. They are AC-coupled 100 Ohm differential lines with 100 Ohm differential terminations inside the module. The AC coupling is inside the module and not required on the Host board. For operation at 28 Gb/s the relevant standards (e.g., OIF CEI v3.1) define the signal requirements on the high-speed differential lines. For operation at lower rates, refer to the relevant standards. Due to the possibility of insertion of modules into a host designed for lower speed operation, the damage threshold of the module input shall be at least 1600 mV peak to peak differential.

Output squelch, hereafter Tx Squelch, for loss of input signal, hereafter Tx LOS, is an optional function. Where implemented it shall function as follows. In the event of the differential, peak-to-peak electrical signal on any channel becomes less than 50 mVpp, then the transmitter optical output for that channel shall be squelched or disabled and the associated TxLOS flag set.

Where squelched, the transmitter OMA shall be less than or equal to -26 dBm and when disabled the transmitter power shall be less than or equal to -30 dBm. For applications, e.g. Ethernet, where the transmitter off condition is defined in terms of average power, disabling the transmitter is recommended and for applications, e.g. InfiniBand, where the transmitter off condition is defined in terms of OMA, squelching the transmitter is recommended.

In module operation, where Tx Squelch is implemented, the default case has Tx Squelch active. Tx Squelch can be deactivated using Tx Squelch Disable through the 2-wire serial interface. Tx Squelch Disable is an optional function. For specific details refer to SFF-8636.

5.5 Power Supply Pins

The circuit card in a QSFP28 module has three designated power pins, labeled VccTx, VccRx and Vcc1. When the QSFP28 module is "hot plugged" into a connector with power already present, the three pins have power applied concurrently. The module is responsible for limiting the inrush current surge during a hot plug event. The host power supply is responsible for supplying up to the maximum inrush current limits during a hot plug event without causing disturbance to other modules and components on the same power supply.

5.5.1 Power Classes and Maximum Power Consumption

QSFP28 modules are categorized into several power classes as listed in Table 5-3. Power Classes are advertised in upper page 00h of the management interface, byte 129 (81h).

TABLE 5-3 QSFP28 - MAXIMUM POWER CLASSES

Power Class	Maximum power dissipation per module (W)
1	1.5
2	2.0
3	2.5
4	3.5
5	4.0
6	4.5

7	5.0

The specification of the host power supply filtering network is beyond the scope of this specification, particularly because of the wide range of QSFP28 module power classes. An example current waveform into a host filter, labeled I1 in Figure 5-4, is plotted in Figure 5-5. Each power connection has a supply filter for the purpose of filtering out high frequency noise and ripple from host-to-module. During a hot-plug event, the filter network limits any voltage drop on the host supply so that neighboring modules sharing the same supply stay within their specified supply voltage limits.

A host board together with the QSFP28 module(s) forms an integrated power system. The host supplies stable power to the modules. Each module limits electrical noise coupled back into the host system and limits inrush charge/current during hot plug insertion. All specifications shall be met at the maximum power supply current. No power sequencing of the power supply is required of the host system since the module sequences the contacts in the order of ground, supply and signals during insertion. Any voltage drop across a filter network on the host is counted against the host DC set point accuracy specification.

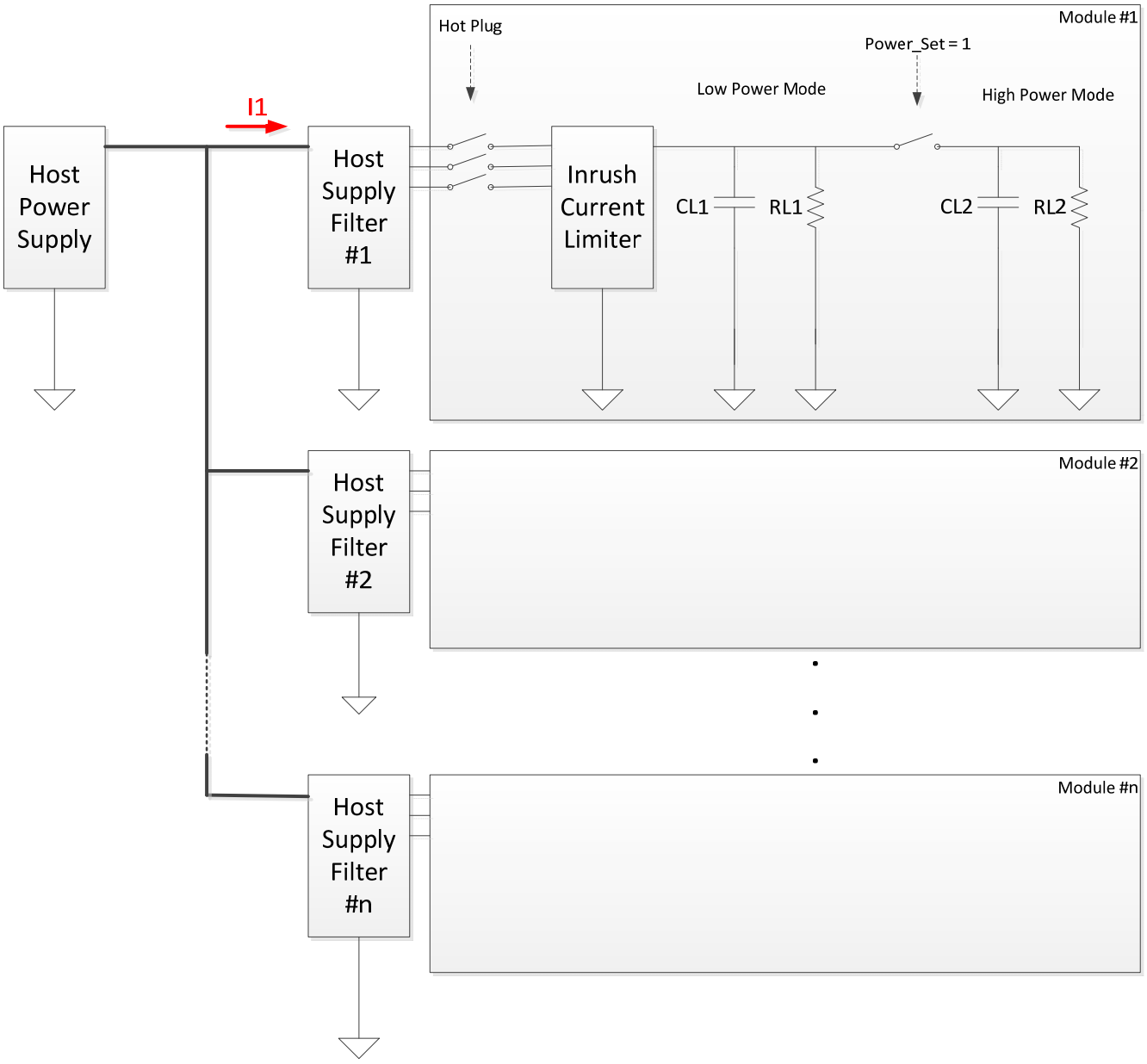


FIGURE 5-4 EXAMPLE: SCHEMATIC OF MULTIPLE QSFP28 POWER SUPPLY ARRANGEMENT

5.5.2 Module Power Supply Specification

In order to avoid exceeding the host system power capacity, upon hot-plug, power cycle or reset, all QSFP28 modules shall power up in power class 1, designated as "Low Power Mode". QSFP28 modules that are class 1 will be fully functional after initialization and remain in low power mode during system operation. All other QSFP28 modules will only reach fully functional operation after the host system enables "High Power Mode".

High power mode is defined as the maximum power class as advertised in page 00, byte 129 and will only be enabled by the host if the host can supply sufficient power to the module. The host system controls whether a particular power class is enabled using the LPMode input pin and by writing to 3 control bits in byte 93. The management interface specification, SFF-8636 provides complete details but for explanation of power supply control, the bits are listed in Table 5-4.

TABLE 5-4 POWER MODE CONTROL BITS (SEE SFF-8636)

Addrs	Bit	Name	Description
93	7-3	Reserved	
	2	High_Power_Class_Enable (Classes 5-7)	When set (=1b) enables power classes 5 to 7 if listed in address 129d. When cleared (=0b), modules with power classes 5 to 7 shall dissipate less than 3.5W, but are not required to be fully functional. Default = 0.
	1	Power_set	Power set to Low Power Mode (class 1). Default = 0.
	0	Power_override	Override of LPMode pin to allow power mode setting by software.

A truth table showing the allowed power classes is shown in Table 5-5.

TABLE 5-5 POWER MODE TRUTH TABLE

High_Power_ Class_Enable bit	LPMode pin state	Power_override bit	Power_set bit	Module Power Classes Allowed
0	1	0	X	1
0	0	0	X	2 to 4
0	X	1	1	1
0	X	1	0	2 to 4
1	1	0	X	1
1	0	0	X	2 to 7
1	X	1	1	1
1	X	1	0	2 to 7

QSFP28 modules operate from the host supplied voltage at the three power pins. To protect the host and system operation, each QSFP28 module during hot plug and normal operation shall follow the requirements listed in Table 5-5 and illustrated in Figure 5-5.

The test configuration for measuring the supply current is a module compliance board (MCB) with reference power supply filters, similar to the circuit shown in SFF-8431, Appendix D, and Figure 56. The QSFP28 MCB can have a single filter per module card or separate filters for each power pin on each module card, depending on the power class and module design. The current limits in Table 5-6 refer to the currents through each inductor.

An example current waveform into a host filter, labeled I1 in Figure 5-4, is plotted in Figure 5-5. This figure also shows the timing of the initial module turn-on in low power mode, and the later transition to full power mode after the host system has enabled it via the two-wire interface.

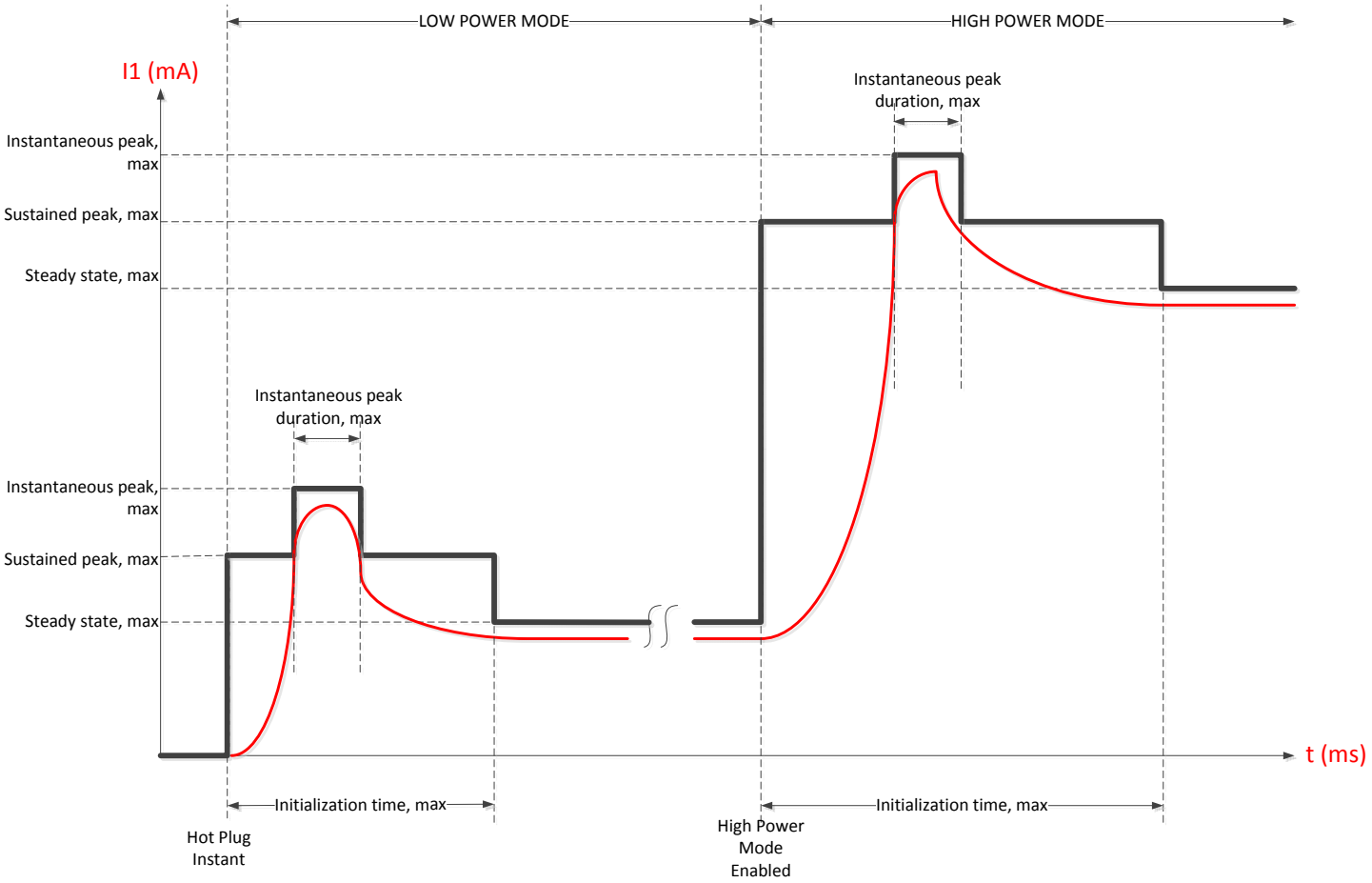


FIGURE 5-5 QSFP28 INRUSH CURRENT TIMING

TABLE 5-6 QSFP28 MODULE POWER SUPPLY SPECIFICATION

Parameter	Symbol	Min	Nom	Max	Unit
Host power supply voltages including ripple, droop and noise below 100 kHz	Vcc_Host	3.135	3.3	3.465	V
Host RMS noise output 10 Hz-10 MHz	e_{N_Host}			25	mV
Module RMS noise output 10 Hz - 10 MHz	e_{N_Mod}			15	mV
Module power supply noise tolerance 10 Hz - 10 MHz (peak-to-peak)	$PSNR_{\_Mod}$			66	mV
Module inrush - instantaneous peak duration	T_ip	-	-	50	µs
Module inrush - initialization time	T_init	-	-	500	ms
Power Class 1 module and low power mode for other modules					
Power consumption	P_1	-	-	1.5	W
Instantaneous peak current at hot plug	Icc_ip_1	-	-	600	mA
Sustained peak current at hot plug	Icc_sp_1	-	-	495	mA
Steady state current	Icc_1	-	-	432.9	mA
Power Class 2 module					
Power consumption	P_3	-	-	2.0	W
Instantaneous peak current at hot plug	Icc_ip_3	-	-	800	mA
Sustained peak current at hot plug	Icc_sp_3	-	-	660	mA
Steady state current	Icc_3	-	-	577.2	mA
Power Class 3 module					
Power consumption	P_4	-	-	2.5	W
Instantaneous peak current at hot plug	Icc_ip_4	-	-	1000	mA
Sustained peak current at hot plug	Icc_sp_4	-	-	825	mA
Steady state current	Icc_4	-	-	721.5	mA
Power Class 4 module					
Power consumption	P_5	-	-	3.5	W
Instantaneous peak current at hot plug	Icc_ip_5	-	-	1400	mA
Sustained peak current at hot plug	Icc_sp_5	-	-	1155	mA
Steady state current	Icc_5	-	-	1010.1	mA
Power Class 5 module					
Power consumption	P_6	-	-	4.0	W
Instantaneous peak current at hot plug	Icc_ip_6	-	-	1600	mA
Sustained peak current at hot plug	Icc_sp_6	-	-	1320	mA
Steady state current	Icc_6	-	-	1154.4	mA
Power Class 6 module					
Power consumption	P_7	-	-	4.5	W
Instantaneous peak current at hot plug	Icc_ip_7	-	-	1800	mA
Sustained peak current at hot plug	Icc_sp_7	-	-	1485	mA
Steady state current	Icc_7	-	-	1298.7	mA
Power Class 7 module					
Power consumption	P_8	-	-	5.0	W
Instantaneous peak current at hot plug	Icc_ip_8	-	-	2000	mA
Sustained peak current at hot plug	Icc_sp_8	-	-	1650	mA
Steady state current	Icc_8	-	-	1443.0	mA

5.5.3 Host Board Power Supply Noise Output

The host shall generate an effective weighted integrated spectrum RMS noise less than the value in Table 5-6 when tested by the methods of SFF-8431, section D.17.1.

5.5.4 Module Power Supply Noise Output

The QSFP28 module shall generate less than the value in Table 5-6 when tested by the methods of SFF-8431, section D.17.2.

5.5.5 Module Power Supply Noise Tolerance

The QSFP28 module shall meet all requirements and remain fully operational in the presence of a sinusoidal tolerance signal of amplitude given by Table 5-6, swept from 10 Hz to 10 MHz according to the methods of SFF-8431, section D.17.3. This emulates the worst case noise output of the host.

5.6 ESD

Where ESD performance is not otherwise specified, e.g. in the InfiniBand specification, the module shall meet ESD requirements given in EN61000-4-2, criterion B test specification when installed in a properly grounded cage and chassis. The units are subjected to 15kV air discharges during operation and 8kV direct contact discharges to the case.

The module and host high speed signal contacts shall withstand 1000 V electrostatic discharge based on Human Body Model per JEDEC JESD22-A114-B.

6 Mechanical and Board Definition

6.1 Introduction

The overall module defined in this clause is illustrated in Figure 6-1. All Pluggable modules and direct attach cable plugs must mate to the connector and cage design defined in this specification. The optical interface shall meet the dimensional specifications of IEC 61754-7 interface 7-3, the MPO adapter interface, and shall optically mate with the plug on the optical fiber cabling. Several cage-to-bezel options are possible. Both metal spring finger and elastomeric EMI solutions are permitted but must pass customer defined requirements. Heat sink/clip thermal designs are application specific and not defined by this specification; however a general design is given as an example.

General View: QSFP Cable Plug/Module and Receptacle/Cage (shown cage accepts heat sink)

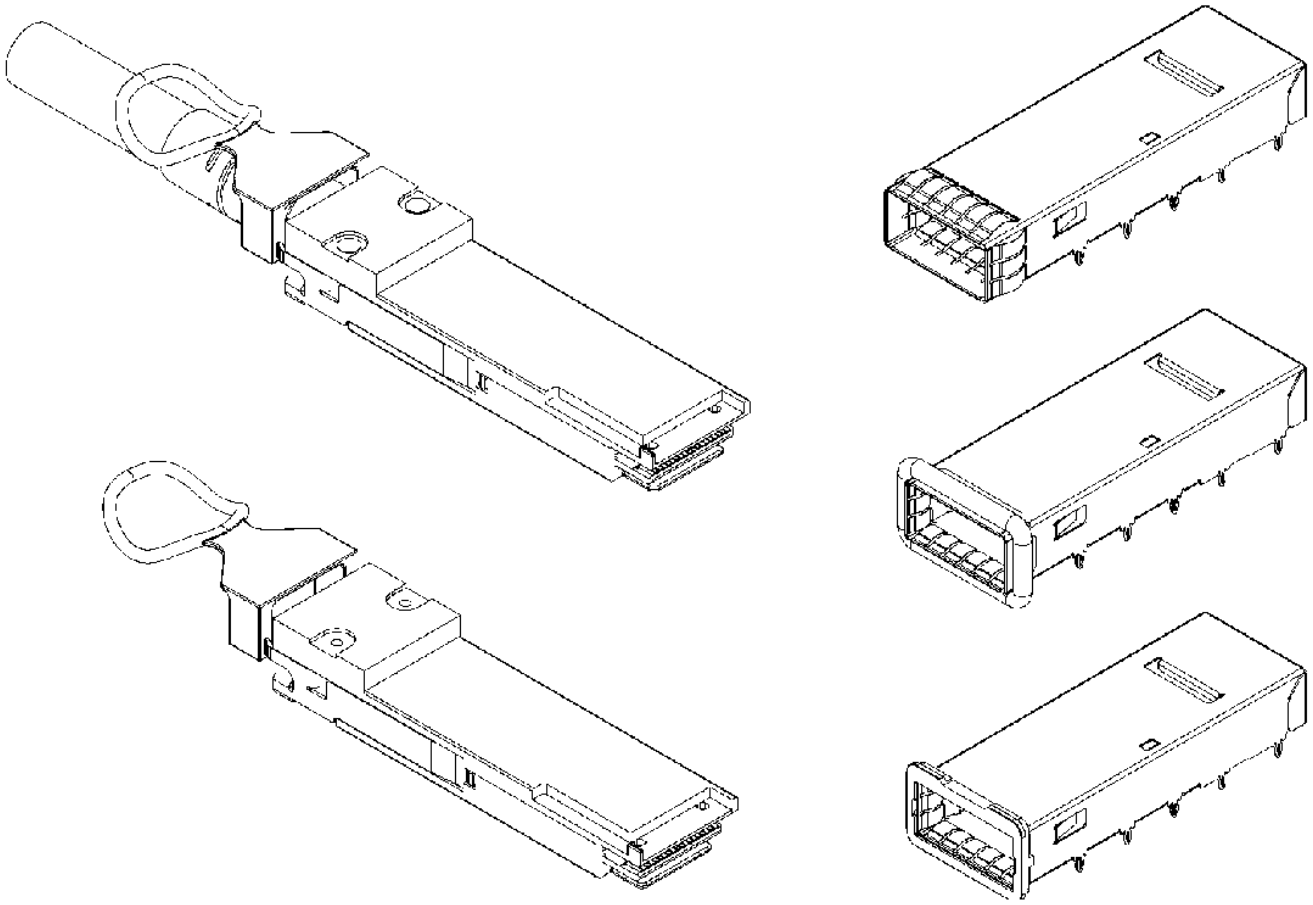


FIGURE 6-1 PLUGGABLE AND DIRECT ATTACH MODULE RENDERING

6.2 Color Coding and Labeling of Modules

An exposed feature of the module (a feature or surface extending outside of the bezel) shall be color coded as follows:

Beige for 850nm
Blue for 1310nm
White for 1550nm

Each module shall be clearly labeled. The complete labeling need not be visible when the module is installed and the bottom of the device is the recommended location for the label. Labeling shall include:

Appropriate manufacturing and part number identification
Appropriate regulatory compliance labeling
A manufacturing traceability code

The label should also include clear specification of the external port characteristics such as:

Optical wavelength
Required fiber characteristics
Operating data rate
Interface standards supported
Link length supported

The labeling shall not interfere with the mechanical, thermal or EMI features.

6.3 Optical Interface

The optical interface port shall be either a male MPO connector as specified in IEC 61754-7 (see Figure 6-4) or a dual LC as specified in IEC 61754-20 (see Figure 6-5).

The four fiber positions on the left as shown in Figure 6-2, with the key up, are used for the optical transmit signals (Channel 1 through 4). The fiber positions on the right are used for the optical receive signals (Channel 4 through 1).

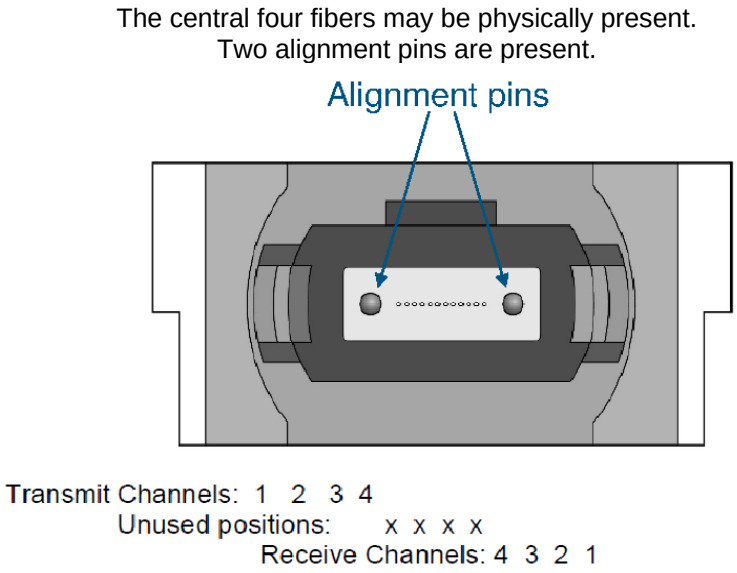


FIGURE 6-2 OPTICAL RECEPTACLE AND CHANNEL ORIENTATION FOR MPO CONNECTOR

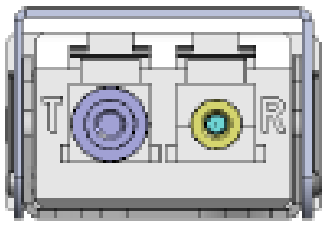


FIGURE 6-3 OPTICAL RECEPTACLE AND CHANNEL ORIENTATION FOR DUAL LC CONNECTOR

6.3.1 MPO Optical Cable Connection

Aligned key (Type B) MPO patch cords should be used to ensure alignment of the signals between the modules. The aligned key patch cord is defined in TIA-568 and shown in Figure 6-4. The optical connector is orientated such that the keying feature of the MPO

receptacle is on the top.

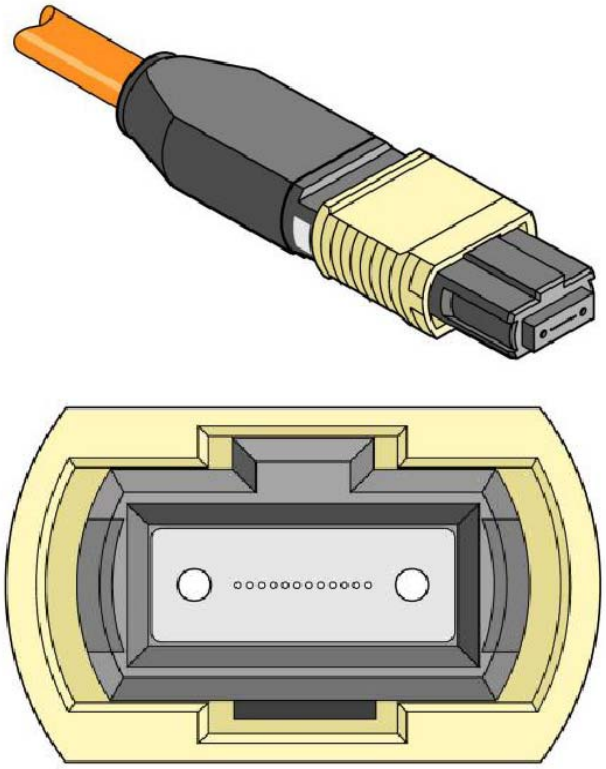


FIGURE 6-4 MPO OPTICAL PATCH CORD

6.3.2 Dual LC Optical Cable Connection

The Dual LC optical cable patch cord is defined in TIA/EIA-604-10A and shown in Figure 6-5.

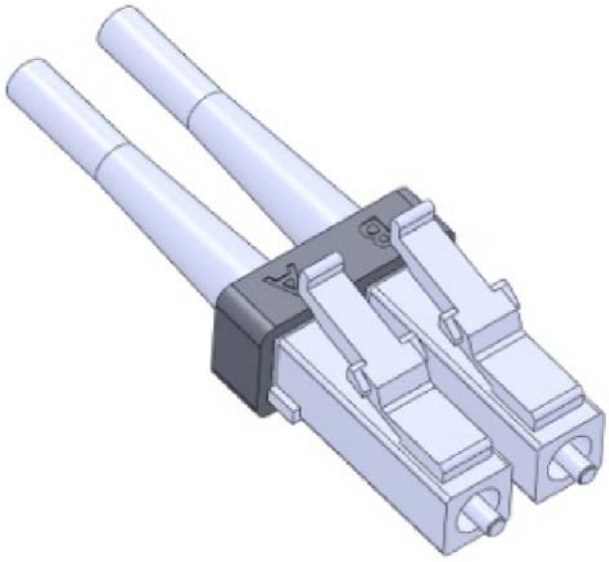


FIGURE 6-5 DUAL LC OPTICAL PATCH CORD

7 Environmental and Thermal

7.1 Thermal Requirements

The module shall operate within one or more of the case temperatures ranges defined in Table 7-1. The temperature ranges are applicable between 60m below sea level and 1800m above sea level, (Ref. NEBS GR-63) utilizing the host systems designed airflow.

TABLE 7-1 TEMPERATURE RANGE CLASS OF OPERATION

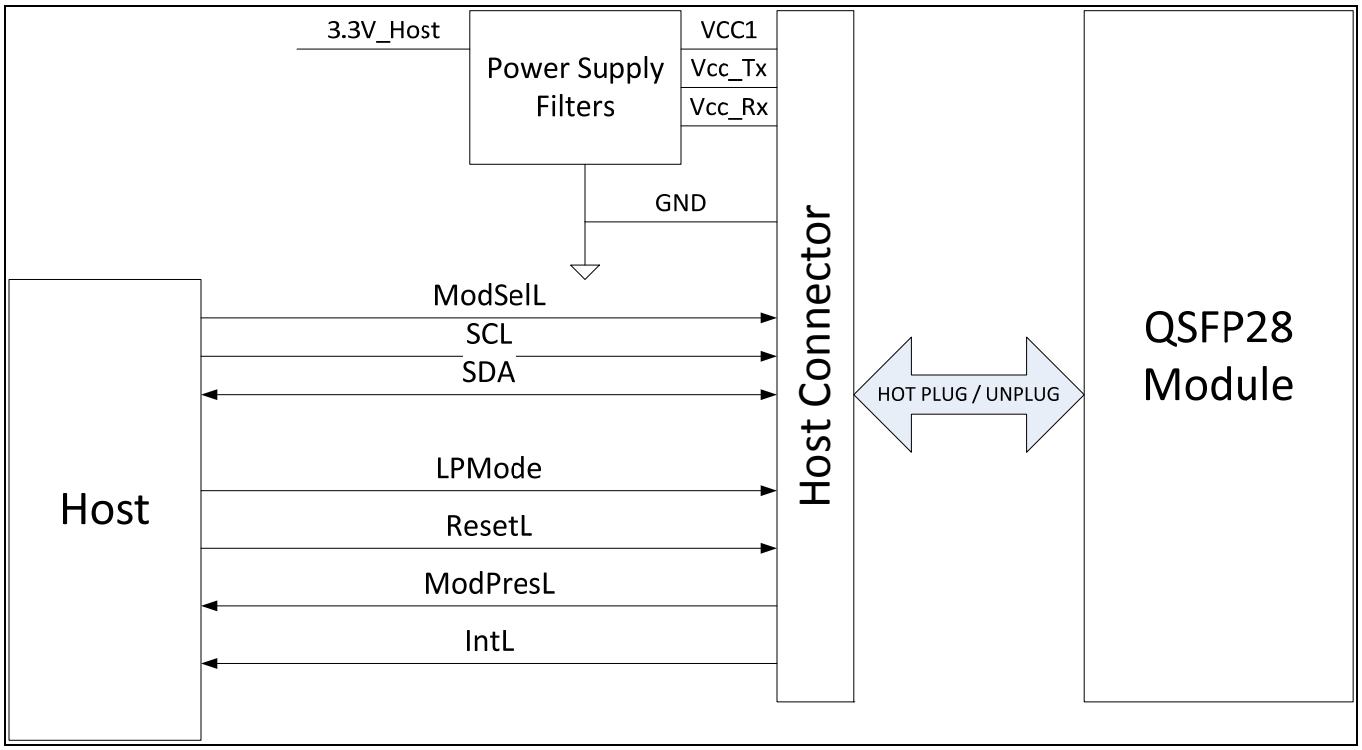
Class	Case Temperature Range
Standard	0 through 70C
Extended	-5 through 85C
Industrial	-40 through 85C

The design allows for up to 16 adjacent modules, ganged and/or belly-to-belly, with the appropriate thermal design for cooling / airflow. (Ref. NEBS GR-63)

8 Timing Requirements

A block diagram illustrating the control and status signals between a host system and a QSFP28 module is shown in Figure 8-1. Timing requirements for the signals SCL, SDA and ModSelL are provided in the SFF-8636 Common Management Interface specification. Timing requirements for the hardware signals ResetL, LPMode and IntL are provided in this section. In addition the timing of control and status functions implemented via the two-wire interface are provided.

FIGURE 8-1 BLOCK DIAGRAM OF MODULE CONTROL SIGNALS



8.1 Soft Control and Status Timing Requirements

TABLE 8-1 SOFT CONTROL AND STATUS TIMING REQUIREMENTS

Parameter	Symbol	Max	Unit	Conditions
Initialization time	t_init	2000	ms	Time from power on*2, hot plug or rising edge of reset until the module is fully functional*3. This time does not apply to non-Power level 0 modules in Low Power State.
Reset Init Assert Time	t_reset_init	2	us	A Reset is generated by a low level longer than t_reset_init present on the ResetL input.
Serial Bus Hardware Ready Time	t_serial	2000	ms	Time from power on*2 until the module responds to data transmission over the two-wire serial bus.
Monitor Data Ready Time	t_data	2000	ms	Time from power on*2 to DataNotReady, byte 2 bit 0, deasserted and IntL output asserted.
Reset Assert Time	t_reset	2000	ms	Time from a rising edge on the ResetL input until the module is fully functional*3.
LPMode Assert Time	ton_LPMode	100	us	Time from assertion of LPMode (Vin:LPMode = Vih) until module power consumption reaches Power Level 1.
LPMode Deassert Time	toff_LPMode	300	ms	Time from deassertion of LPMode (Vin:LPMode = Vil) until module is fully functional*3,*5.
IntL Assert Time	ton_IntL	200	ms	Time from occurrence of condition triggering IntL until Vout:IntL=Vol.
IntL Deassert Time	toff_IntL	500	us	Time from clear on read*4 operation of associated flag until Vout:IntL=Voh. This includes deassert times for Rx LOS, Tx Fault and other flag bits.
Rx LOS Assert Time	ton_LOS	100	ms	Time from Rx LOS state to Rx LOS bit set (value = 1b) and IntL asserted.
Tx Fault Assert Time	ton_Txfault	200	ms	Time from Tx Fault state to Tx Fault bit set (value = 1b) and IntL asserted.
Flag Assert Time	ton_flag	200	ms	Time from condition triggering flag to associated flag bit set (value = 1b) and IntL asserted.
Mask Assert Time	ton_mask	100	ms	Time from mask bit set (value = 1b)*1 until associated IntL assertion is inhibited.
Mask Deassert Time	toff_mask	100	ms	Time from mask bit cleared (value = 0b)*1 until associated IntL operation resumes.
Application or Rate Select Change Time	t_ratesel	100	ms	Time from change of state of Application or Rate Select bit*1 until transmitter or receiver bandwidth is in conformance with appropriate specification.
Power_override or Power_set Assert Time	ton_Pdown	100	ms	Time from P_Down bit set (value = 1b)*1 until module power consumption reaches Power Level 1.
Power_override or Power_set Deassert Time	toff_Pdown	300	ms	Time from P_Down bit cleared (value = 0b)*1 until module is fully functional.
*1 Measured from falling clock edge after STOP bit of write transaction.				
*2 Power on is defined as the instant when supply voltages reach and remain at or above the minimum level specified in Table 6.				
*3 Fully functional is defined as IntL asserted due to DataNotReady, bit 0 byte 2, deasserted. The module should also meet optical and electrical specifications.				
*4 Measured from falling clock edge after STOP bit of read transaction.				
*5 Does not apply to Power Level 1 modules.				

8.2 Squelch and TxRx Disable Assert, Deassert and Enable/Disable Timing

Table 8-2 lists the required timing performance for assert, deassert, enable and disable of the Tx Squelch, Rx Squelch, Tx Disable and Rx Output Disable functions.

TABLE 8-2 QSFP28 SQUELCH AND TXRX DISABLE TIMING

Parameter	Symbol	Max	Unit	Conditions
Rx Squelch Assert Time	ton_Rxsq	80	us	Time from loss of Rx input signal until the squelched output condition is reached. See Subclause 4.1.3.1.
Rx Squelch Deassert Time	toff_Rxsq	80	us	Time from resumption of Rx input signals until normal Rx output condition is reached. See Subclause 4.1.3.1.
Tx Squelch Assert Time	ton_Txsq	400	ms	Time from loss of Tx input signal until the squelched output condition is reached. See Subclause 4.1.3.2.
Tx Squelch Deassert Time	toff_Txsq	400	ms	Time from resumption of Tx input signals until normal Rx output condition is reached. See Subclause 4.1.3.2.
Tx Disable Assert Time	ton_TxDis	100	ms	Time from Tx Disable bit set (value = 1b)*1 until optical output falls below 10% of nominal.
Tx Disable Deassert Time	toff_TxDis	400	ms	Time from Tx Disable bit cleared (value = 0b)*1 until optical output rises above 90% of nominal.
Rx Output Disable Assert Time	ton_RxDis	100	ms	Time from Rx Output Disable bit set (value = 1b)*1 until Rx output falls below 10% of nominal.
Rx Output Disable Deassert Time	toff_RxDis	100	ms	Time from Rx Output Disable bit cleared (value = 0b)*1 until Rx output rises above 90% of nominal.
Squelch Disable Assert Time	ton_sqDIS	100	ms	This applies to Rx and Tx Squelch and is the time from bit cleared (value =0b)*1 until squelch functionality is enabled.
Squelch Disable Deassert Time	toff_RxDis	100	ms	This applies to Rx and Tx Squelch and is the time from bit set (value =1b)*1 until squelch functionality is disabled.
*1 Measured from falling clock edge after STOP bit of write transaction.				