SFF Committee documentation may be purchased in electronic form.
SFF specifications are available at ftp://ftp.seagate.com/sff

SFF Committee

SFF-9401

Specification for

SAS-4 Internal Cabling Pinout Recommendations

Rev 0.3 June 30, 2015

Secretariat: SFF Committee

Abstract: This specification recommends the pinouts to use when cabling SAS-4 configurations internal to the cabinet, and tabulates the relationship between PCIe Gen 3 and SAS-4 Internal Routing Connections

This specification provides a common reference for systems manufacturers, system integrators, and suppliers. This is an internal working specification of the SFF Committee, an industry ad hoc group.

This specification is made available for public review, and written comments are solicited from readers. Comments received will be considered for inclusion in future revisions of this specification.

Support: This specification is supported by the identified member companies of the SFF Committee.

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EXPRESSION OF SUPPORT BY MANUFACTURERS

The following member companies of the SFF Committee voted in favor of this industry specification:

tbd

The following member companies of the SFF Committee voted against this industry specification:

tbd

The following member companies of the SFF Committee voted to abstain on this industry specification:

tbd

Change History

Rev 0.1
- Presentation incorporated as an i-specification
Rev 0.2
- Introduced as a Development project
Rev 0.3
- Formatted to the current style

Foreword

The development work on this specification was done by the SFF Committee, an industry group. The membership of the committee since its formation in August 1990 has included a mix of companies which are leaders across the industry.

When 2 1/2" diameter disk drives were introduced, there was no commonality on external dimensions e.g. physical size, mounting locations, connector type, connector location, between vendors.

The first use of these disk drives was in specific applications such as laptop portable computers and system integrators worked individually with vendors to develop the packaging. The result was wide diversity, and incompatibility.

The problems faced by integrators, device suppliers, and component suppliers led to the formation of the SFF Committee as an industry ad hoc group to address the marketing and engineering considerations of the emerging new technology.

During the development of the form factor definitions, other activities were suggested because participants in the SFF Committee faced more problems than the physical form factors of disk drives. In November 1992, the charter was expanded to address any issues of general interest and concern to the storage industry. The SFF Committee became a forum for resolving industry issues that are either not addressed by the standards process or need an immediate solution.

Those companies which have agreed to support a specification are identified in the first pages of each SFF Specification. Industry consensus is not an essential requirement to publish an SFF Specification because it is recognized that in an emerging product area, there is room for more than one approach. By making the documentation on competing proposals available, an integrator can examine the alternatives available and select the product that is felt to be most suitable.

SFF Committee meetings are held during T10 weeks (see www.t10.org), and Specific Subject Working Groups are held at the convenience of the participants. Material presented at SFF Committee meetings becomes public domain, and there are no restrictions on the open mailing of material presented at committee meetings.

Most of the specifications developed by the SFF Committee have either been incorporated into standards or adopted as standards by EIA (Electronic Industries Association), ANSI (American National Standards Institute) and IEC (International Electrotechnical Commission).

If you are interested in participating or wish to follow the activities of the SFF Committee, the signup for membership and/or documentation can be found at:

www.sffcommittee.com/ie/join.html

The complete list of SFF Specifications which have been completed or are currently being worked on by the SFF Committee can be found at:
ftp://ftp.seagate.com/sff/SFF-8000.TXT

If you wish to know more about the SFF Committee, the principles which guide the activities can be found at:
ftp://ftp.seagate.com/sff/SFF-8032.TXT

Suggestions for improvement of this specification will be welcome. They should be sent to the SFF Committee, 14426 Black Walnut Ct, Saratoga, CA 95070.

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SFF Committee --

SAS-4 Internal Cabling Pinout Recommendations

1. Scope

Industry storage solutions are implementing both SAS and PCIe within the same or similar enclosures. This specification recommends the pinning out of standardized connectors to accommodate multiple protocols.

2. References

2.1 Industry Documents

- OCuLink Spec Rev 0.9
- SFF-8448 SAS Sideband Utilization
- SFF-8643 Mini Multilane 4/8X 12 Gb/s Unshielded Connector (HD12un)

2.2 SFF Specifications

There are several projects active within the SFF Committee. The complete list of specifications which have been completed or are still being worked on are listed in the specification at ftp://ftp.seagate.com/sff/SFF-8000.TXT

2.3 Sources

Those who join the SFF Committee as an Observer or Member receive electronic copies of the minutes and SFF specifications (http://www.sffcommittee.com/ie/join.html).

Copies of ANSI standards may be purchased from the InterNational Committee for Information Technology Standards (http://www.techstreet.com/incitsgate.tmpl).

3. General Description

The connector figures below are shown for reference only to show how the pinouts shown in the tables relate to the physical locations of the pins for each of the connector styles. These pinouts comply with the SAS pinouts defined in SFF-8448 and in the PCIe pinouts defined by OCuLink. All are based on the fixed end definitions of the pin assignments.

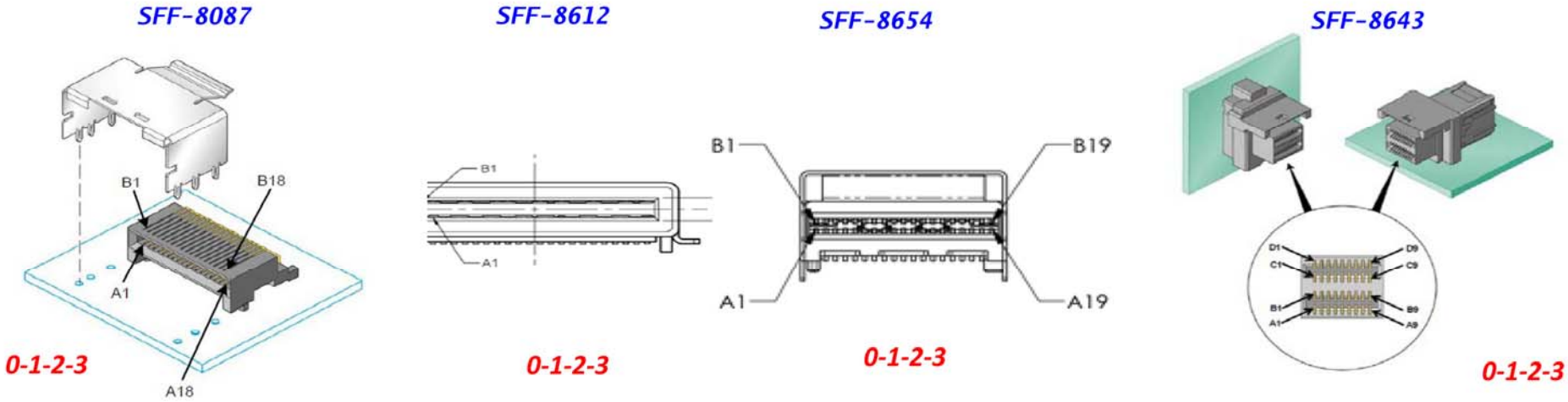

FIGURE 3-1 CONNECTOR VIEWS

The tables define the lane and polarity of the high speed pairs through all the standardized connectors.

The sideband pin assignments for the SFF-8643 connector have been optimized to support PCIe sideband (REFCLK) signals and would revert back to the SAS-3 definitions for SAS applications.

TABLE 3-1 PINOUT FOR A 4 LANE STORAGE INTERFACE WITH SIDEBANDS

Controller / Root (Downstream)								Backplane/ Endpoint (Upstream)							DEVICE	DEVICE
8087	8643	8643	8654	8612	OCuLink(R9_v3)	9400	CABLE	9400	OCuLink(R9_v3)	8612	8654	8643	8643	8087	8639	MultiLink
SAS-2.1	SAS-3	PCIE	SAS-4	SAS-4	PCIE	UNIVERSIAL		UNIVERSAL	PCIE	SAS-4	SAS-4	PCIE	SAS-3	SAS-2.1	PCIE	SAS
PIN	PIN	PIN	PIN	PIN	PIN	ROOT	DIR	END Point	PIN	PIN	PIN	PIN	PIN	PIN	PIN	PIN
				A1	A1	RESERVED	NC	RESERVED	B1	B1						
A1	***B3***	***B3***	***A1***	***A2***	***A2***	***GROUND***	⍰	***GROUND***	***B2***	***B2***	***B1***	***D3***	***D3***	***B1***		
A2	B4	B4	A2	A3	A3	PER(RX)p0	←	PET(TX)p0	B3	B3	B2	D4	D4	B2	E14 (PERp0)	S6 (TX0+)
A3	B5	B5	A3	A4	A4	PER(RX)n0	←	PET(TX)n0	B4	B4	B3	D5	D5	B3	E13 (PERn0)	S5 (TX0-)
A4	***A3***	***A3***	***A4***	***A5***	***A5***	***GROUND***	⍰	***GROUND***	***B5***	***B5***	***B4***	***C3***	***C3***	***B4***		
A5	A4	A4	A5	A6	A6	PER(RX)p1	←	PET(TX)p1	B6	B6	B5	C4	C4	B5	S21 (PERp1)	S13 (TX1+)
A6	A5	A5	A6	A7	A7	PER(RX)n1	←	PET(TX)n1	B7	B7	B6	C5	C5	B6	S20 (PERn1)	S12 (TX1-)
A7	***A6***	***A6***	***A7***	***A8***	***A8***	***GROUND***	⍰	***GROUND***	***B8***	***B8***	***B7***	***C6***	***C6***	***B7***		
A8(SB7)	A1(SB7)	A1	A8	A9 (BP_TYPE)	A9(BP_TYPE)	*VSP7/SB7*	←	*VSP7/SB7*	B9(BP_TYPE)	B9(BP_TYPE)	B8	A2	A2(SB7)	B8(SB7)		
A9(SB3)	B1(SB3)	B1	A9	A10(GND)	A10(CWAKE#)	*VSP3/SB3*	←	*VSP3/SB3*	B10(CWAKE#)	B10(GND)	B9	B2	B2(SB3)	B9(SB3)	P1 (WAKE#)	
			A10	A11 (VSP9/SB9)	A11(GND)	*VSP9/SB9*	⍰	*VSP9/SB9*	B11(GND)	B11(VSP9/SB9))	B10					
A10(SB4)	C1(SB4)	C1	A11	A12(RESET#)	A12(VSP)	*VSP4/SB4*	→	*VSP4/SB4*	B12(VSP)	B12(RESET#)	B11	C2	C2(SB4)	B10(SB4)	E7 (REFCLK+)	
A11(SB5)	D1(SB5)	D1	A12	A13(ADD)	A13(VSP)	*VSP5/SB5*	→	*VSP5/SB5*	B13(VSP)	B13(ADD)	B12	D2	D2(SB5)	B11(SB5)	E8 (REFCLK-)	
A12	***B6***	***B6***	***A13***	***A14***	***A14***	***GROUND***	⍰	***GROUND***	***B14***	***B14***	***B13***	***D6***	***D6***	***B12***		
A13	B7	B7	A14	A15	A15	PER(RX)p2	←	PETp2	B15	B15	B14	D7	D7	B13	S27 (PERp2)	S21 (TX2+)
A14	B8	B8	A15	A16	A16	PER(RX)n2	←	PETn2	B16	B16	B15	D8	D8	B14	S26 (PERn2)	S20 (TX2-)
A15	***B9***	***B9***	***A16***	***A17***	***A17***	***GROUND***	⍰	***GROUND***	***B17***	***B17***	***B16***	***D9***	***D9***	***B15***		
A16	A7	A7	A17	A18	A18	PER(RX)p3	←	PET(TX)p3	B18	B18	B17	C7	C7	B16	E21 (PERp3)	S27 (TX3+)
A17	A8	A8	A18	A19	A19	PER(RX)n3	←	PET(TX)n3	B19	B19	B18	C8	C8	B17	E20 (PERn3)	S26 (TX3-)
A18	***A9***	***A9***	***A19***	***A20***	***A20***	***GROUND***		***GROUND***	***B20***	***B20***	***B19***	***C9***	***C9***	***B18***		
				A21	A21	RESERVED	NC	RESERVED	B21	B21						
				B1	B1	RESERVED	NC	RESERVED	B1	B1						
B1	***D3***	***D3***	***B1***	***B2***	***B2***	***GROUND***	⍰	***GROUND***	***A2***	***A2***	***A1***	***B3***	***B3***	***A1***		
B2	D4	D4	B2	B3	B3	PET(TX)p0	→	PER(RX)p0	A3	A3	A2	B4	B4	A2	E10 (PETp0)	S2 (RX0+)
B3	D5	D5	B3	B4	B4	PET(TX)n0	→	PER(RX)n0	A4	A4	A3	B5	B5	A3	E11 (PETn0)	S3 (RX0-)
B4	***C3***	***C3***	***B4***	***B5***	***B5***	***GROUND***	⍰	***GROUND***	***A5***	***A5***	***A4***	***A3***	***A3***	***A4***		
B5	C4	C4	B5	B6	B6	PET(TX)p1	→	PER(*RX*) p1	A6	A6	A5	A4	A4	A5	S17 (PETp1)	S9 (RX1+)
B6	C5	C5	B6	B7	B7	PET(TX)n1	→	PER(RX)n1	A7	A7	A6	A5	A5	A6	S18 (PETn1)	S10 (RX1-)
B7	***C6***	***C6***	***B7***	***B8***	***B8***	***GROUND***	⍰	***GROUND***	***A8***	***A8***	***A7***	***A6***	***A6***	***A7***		
B8(SB0)	A2(SB0)	A2	B8	B9(2W-CLK)	B9(2W-CLK)	*VSP0/SB0*	↔	*VSP0/SB0*	A9(2W-CLK)	A9(2W-CLK)	A8	A1	A1(SB0)	A8(SB0)		
B9(SB1)	B2(SB1)	B2	B9	B10(2W-DATA)	B10(2W-DATA)	*VSP1/SB1*	↔	*VSP1/SB1*	A10(2W-DATA)	A10(2W-DATA)	A9	B1	B1(SB1)	A9(SB1)		
			B10	B11(VSP8/SB8)	B11(GROUND)	*VSP8/SB8*	⍰	*VSP8/SB8*	A11(GROUND)	A11(VSP8/SB8)	A10					
B10(SB2)	C2(SB2)	C2	B11	B12(GND)	B12(PERST#)	*VSP2/SB2*	→	*VSP2/SB2*	A12(PERST#)	A12(GND)	A11	C1	C1(SB2)	A10(SB2)	E5 (PERST#)	
B11(SB6)	D2(SB6)	D2	B12	B13(CNTR_TYPE)	B13(CPRSNT#)	*VSP6/SB6*	←	*VSP6/SB6*	A13(CPRSNT#)	A13 (CNTR_TYPE)	A12	D1	D1(SB6)	A11(SB6)		
B12	***D6***	***D6***	***B13***	***B14***	***B14***	***GROUND***	⍰	***GROUND***	***A14***	***A14***	***A13***	***B6***	***B6***	***A12***		
B13	D7	D7	B14	B15	B15	PET(TX)p2	→	PER(RX)p2	A15	A15	A14	B7	B7	A13	S23 (PETp2)	S17 (RX2+)
B14	D8	D8	B15	B16	B16	PET(TX)n2	→	PER(RX)n2	A16	A16	A15	B8	B8	A14	S24 (PETn2)	S18 (RX2-)
B15	***D9***	***D9***	***B16***	***B17***	***B17***	***GROUND***	⍰	***GROUND***	***A17***	***A17***	***A16***	***B9***	***B9***	***A15***		
B16	C7	C7	B17	B18	B18	PET(TX)p3	→	PER(RX)p3	A18	A18	A17	A7	A7	A16	E17 (PETp3)	S23 (RX3+)
B17	C8	C8	B18	B19	B19	PET(TX)n3	→	PER(RX)n3	A19	A19	A18	A8	A8	A17	E18 (PETn3)	S24 (RX3-)
B18	***C9***	***C9***	***B19***	***B20***	***B20***	***GROUND***	⍰	***GROUND***	***A20***	***A20***	***A19***	***A9***	***A9***	***A18***		
				B21	B21	RESERVED	NC	RESERVED	A21	A21						
														T10 15-118r3 4x Molex		
														SHEET 1 OF 1		

TABLE 3-2 PINOUT FOR AN 8 LANE STORAGE INTERFACE WITH SIDEBANDS (1 OF 2)

Controller / Root (Downstream)								Backplane/ Endpoint (Upstream)							DEVICE	DEVICE
8087	8643	8643	8654	8612	OCuLink(R9-v3)	9400	CABLE	9400	OCuLink(R9_v3)	8612	8654	8643	8643	8087	8639	MultiLink
SAS-2.1	SAS-3	PCIE?	SAS-4	SAS-4	PCIE	UNIVERSAL		UNIVERSAL	PCIE	SAS-4	SAS-4	PCIE?	SAS-3	SAS-2.1	PCIE	SAS
PIN	PIN	PIN	PIN	PIN	PIN	ROOT	DIR	END Point	PIN	PIN	PIN	PIN	PIN	PIN	PIN	PIN
A1	B3	B3	A1	A1	A1	GROUND	–	GROUND	B1	B1	B1	D3	D3	B1		
A2	B4	B4	A2	A2	A2	PER(RX)p0	←	PET(TX)p0	B2	B2	B2	D4	D4	B2	E14 (PERp0)	S6 (TX0+)
A3	B5	B5	A3	A3	A3	PER(RX)n0	←	PET(TX)n0	B3	B3	B3	D5	D5	B3	E13 (PERn0)	S5 (TX0-)
A4	A3	A3	A4	A4	A4	GROUND	–	GROUND	B4	B4	B4	C3	C3	B4		
A5	A4	A4	A5	A5	A5	PER(RX)p1	←	PET(TX)p1	B5	B5	B5	C4	C4	B5	S21 (PERp1)	S13 (TX1+)
A6	A5	A5	A6	A6	A6	PER(RX)n1	←	PET(TX)n1	B6	B6	B6	C5	C5	B6	S20 (PERn1)	S12 (TX1-)
A7	A6	A6	A7	A7	A7	GROUND	–	GROUND	B7	B7	B7	C6	C6	B7		
A8(SB7)	A1(SB7)	A1	A8	A8(BP_TYPE)	A8(BP_TYPE)	VSP7/SB7	←	VSP7/SB7	B8(BP_TYPE)	B8(BP_TYPE)	B8	A2	A2(SB7)	B8(SB7)		
A9(SB3)	B1(SB3)	B1	A9	A9(GND)	A9(CWAKE#)	VSP3/SB3	←	VSP3/SB3	B9(CWAKE#)	B8(GND)	B9	B2	B2(SB3)	B9(SB3)	P1 (WAKE#)	
			A10	A10(VSP9/SB9)	A10(GND)	VSP9/SB9	–	VSP9/SB9	B10(GND)	B10(VSP9/SB9))	B10					
A10(SB4)	C1(SB4)	C1	A11	A11(RESET#)	A11(VSP)	VSP4/SB4	→	VSP4/SB4	B11(VSP)	B11(RESET#)	B11	C2	C2(SB4)	B10(SB4)	E7 (REFCLK+)	
A11(SB5)	D1(SB5)	D1	A12	A12(ADD)	A12(VSP)	VSP5/SB5	→	VSP5/SB5	B12(VSP)	B12(ADD)	B12	D2	D2(SB5)	B11(SB5)	E8 (REFCLK-)	
A12	B6	B6	A13	A13	A13	GROUND	–	GROUND	B13	B13	B13	D6	D6	B12		
A13	B7	B7	A14	A14	A14	PER(RX)p2	←	PETp2	B14	B14	B14	D7	D7	B13	S27 (PERp2)	S21 (TX2+)
A14	B8	B8	A15	A15	A15	PER(RX)n2	←	PETn2	B15	B15	B15	D8	D8	B14	S26 (PERn2)	S20 (TX2-)
A15	B9	B9	A16	A16	A16	GROUND	–	GROUND	B16	B16	B16	D9	D9	B15		
A16	A7	A7	A17	A17	A17	PER(RX)p3	←	PET(TX)p3	B17	B17	B17	C7	C7	B16	E21 (PERp3)	S27 (TX3+)
A17	A8	A8	A18	A18	A18	PER(RX)n3	←	PET(TX)n3	B18	B18	B18	C8	C8	B17	E20 (PERn3)	S26 (TX3-)
A18	A9	A9	A19	A19	A19	GROUND	–	GROUND	B19	B19	B19	C9	C9	B18		
				A20	A20	RESERVED	NC	RESERVED	B20	B20						
				A21	A21	RESERVED	NC	RESERVED	B21	B21						
A1	B3	B3		A22	A22	GROUND	–	GROUND	B22	B22		D3	D3	B1		
A2	B4	B4	A20	A23	A23	PER(RX)p4	←	PET(TX)p4	B23	B23	B20	D4	D4	B2	E14 (PERp0)	S6 (TX0+)
A3	B5	B5	A21	A24	A24	PER(RX)n4	←	PET(TX)n4	B24	B24	B21	D5	D5	B3	E13 (PERn0)	S5 (TX0-)
A4	A3	A3	A22	A25	A25	GROUND	–	GROUND	B25	B25	B22	C3	C3	B4		
A5	A4	A4	A23	A26	A26	PER(RX)p5	←	PET(TX)p5	B26	B26	B23	C4	C4	B5	S21 (PERp1)	S13 (TX1+)
A6	A5	A5	A24	A27	A27	PER(RX)n5	←	PET(TX)n5	B27	B27	B24	C5	C5	B6	S20 (PERn1)	S12 (TX1-)
A7	A6	A6	A25	A28	A28	GROUND	–	GROUND	B28	B28	B25	C6	C6	B7		
A8(SB7)	A1(SB7)	A1	A26	A29 (BP_TYPE)	A29(BP_TYPE)	VSP7/SB7	←	VSP7/SB7	B29(BP_TYPE)	B29(BP_TYPE)	B26	A2	A2(SB7)	B8(SB7)		
A9(SB3)	B1(SB3)	B1	A27	A30(GND)	A30(CWAKE#)	VSP3/SB3	←	VSP3/SB3	B30(CWAKE#)	B30(GND)	B27	B2	B2(SB3)	B9(SB3)	P1 (WAKE#)	
			A28	A31 (VSP9/SB9)	A31(GND)	VSP9/SB9	–	VSP9/SB9	B31(GND)	B31(VSP9/SB9))	B28					
A10(SB4)	C1(SB4)	C1	A29	A32(RESET#)	A32(VSP)	VSP4/SB4	→	VSP4/SB4	B32(VSP)	B32(RESET#)	B29	C2	C2(SB4)	B10(SB4)	E7 (REFCLK+)	
A11(SB5)	D1(SB5)	D1	A30	A33(ADD)	A33(VSP)	VSP5/SB5	→	VSP5/SB5	B33(VSP)	B33(ADD)	B30	D2	D2(SB5)	B11(SB5)	E8 (REFCLK-)	
A12	B6	B6	A31	A34	A34	GROUND	–	GROUND	B34	B34	B31	D6	D6	B12		
A13	B7	B7	A32	A35	A35	PER(RX)p6	←	PETp6	B35	B35	B32	D7	D7	B13	S27 (PERp2)	S21 (TX2+)
A14	B8	B8	A33	A36	A36	PER(RX)n6	←	PETn6	B36	B36	B33	D8	D8	B14	S26 (PERn2)	S20 (TX2-)
A15	B9	B9	A34	A37	A37	GROUND	–	GROUND	B37	B37	B34	D9	D9	B15		
A16	A7	A7	A35	A38	A38	PER(RX)p7	←	PET(TX)p7	B38	B38	B35	C7	C7	B16	E21 (PERp3)	S27 (TX3+)
A17	A8	A8	A36	A39	A39	PER(RX)n7	←	PET(TX)n7	B39	B39	B36	C8	C8	B17	E20 (PERn3)	S26 (TX3-)
A18	A9	A9	A37	A40	A40	GROUND	–	GROUND	B40	B40	B37	C9	C9	B18		
														T10 15-118r3 8x Molex		
														SHEET 1 OF 2		

TABLE 3-3 PINOUT FOR AN 8 LANE STORAGE INTERFACE WITH SIDEBANDS (2 OF 2)

Controller / Root (Downstream)								Backplane/ Endpoint (Upstream)							DEVICE	DEVICE
8087	8643	8643	8654	8612	OCuLink(R9_v2)	9400	CABLE	9400	OCuLink(R9_v2)	8612	8654	8643	8643	8087	8639	MultiLink
SAS-2.1	SAS-3	PCIE?	SAS-4	SAS-4	PCIE	UNIVERSAL		UNIVERSAL	PCIE	SAS-4	SAS-4	PCIE?	SAS-3	SAS-2.1	PCIE	SAS
B1	D3	D3	B1	B1	B1	GROUND	–	GROUND	A1	A1	A1	B3	B3	A1		
B2	D4	D4	B2	B2	B2	PET(TX)p0	→	PER(RX)p0	A2	A2	A2	B4	B4	A2	E10 (PETp0)	S2 (RX0+)
B3	D5	D5	B3	B3	B3	PET(TX)n0	→	PER(RX)n0	A3	A3	A3	B5	B5	A3	E11 (PETn0)	S3 (RX0)
B4	C3	C3	B4	B4	B4	GROUND	–	GROUND	A4	A4	A4	A3	A3	A4		
B5	C4	C4	B5	B5	B5	PET(TX)p1	→	PER(RX) p1	A5	A5	A5	A4	A4	A5	S17 (PETp1)	S9 (RX1+)
B6	C5	C5	B6	B6	B6	PET(TX)n1	→	PER(RX)n1	A6	A6	A6	A5	A5	A6	S18 (PETn1)	S10 (RX1)
B7	C6	C6	B7	B7	B7	GROUND	–	GROUND	A7	A7	A7	A6	A6	A7		
B8(SB0)	A2(SB0)	A2	B8	B8(2W-CLK)	B8(2W-CLK)	VSP0/SB0	↔	VSP0/SB0	A8(2W-CLK)	A8(2W-CLK)	A8	A1	A1(SB0)	A8(SB0)		
B9(SB1)	B2(SB1)	B2	B9	B9(2W-DATA)	B9(2W-DATA)	VSP1/SB1	↔	VSP1/SB1	A9(2W-DATA)	A9(2W-DATA)	A9	B1	B1(SB1)	A9(SB1)		
			B10	B10(VSP8/SB8)	B10(GROUND)	VSP8/SB8	–	VSP8/SB8	A10(GROUND)	A10(VSP8/SB8)	A10					
B10(SB2)	C2(SB2)	C2	B11	B11(GND)	B11(PERST#)	VSP2/SB2	→	VSP2/SB2	A11(PERST#)	A11(GND)	A11	C1	C1(SB2)	A10(SB2)	E5 (PERST#)	
B11(SB6)	D2(SB6)	D2	B12	B12(CNTR_TYPE)	B12(CPRSNT#)	VSP6/SB6	←	VSP6/SB6	A12(CPRSNT#)	A12(CNTR_TYPE)	A12	D1	D1(SB6)	A11(SB6)		
B12	D6	D6	B13	B13	B13	GROUND	–	GROUND	A13	A13	A13	B6	B6	A12		
B13	D7	D7	B14	B14	B14	PET(TX)p2	→	PER(RX)p2	A14	A14	A14	B7	B7	A13	S23 (PETp2)	S17 (RX2+)
B14	D8	D8	B15	B15	B15	PET(TX)n2	→	PER(RX)n2	A15	A15	A15	B8	B8	A14	S24 (PETn2)	S18 (RX2)
B15	D9	D9	B16	B16	B16	GROUND	–	GROUND	A16	A16	A16	B9	B9	A15		
B16	C7	C7	B17	B17	B17	PET(TX)p3	→	PER(RX)p3	A17	A17	A17	A7	A7	A16	E17 (PETp3)	S23 (RX3+)
B17	C8	C8	B18	B18	B18	PET(TX)n3	→	PER(RX)n3	A18	A18	A18	A8	A8	A17	E18 (PETn3)	S24 (RX3)
B18	C9	C9	B19	B19	B19	GROUND	–	GROUND	A19	A19	A19	A9	A9	A18		
				B20	B20	RESERVED	NC	RESERVED	A20	A20						
				B21	B21	RESERVED	NC	RESERVED	A21	A21						
B1	D3	D3		B22	B22	GROUND	–	GROUND	A22	A22		B3	B3	A1		
B2	D4	D4	B20	B23	B23	PET(TX)p4	→	PER(RX)p4	A23	A23	A20	B4	B4	A2	E10 (PETp0)	S2 (RX0+)
B3	D5	D5	B21	B24	B24	PET(TX)n4	→	PER(RX)n4	A24	A24	A21	B5	B5	A3	E11 (PETn0)	S3 (RX0-)
B4	C3	C3	B22	B25	B25	GROUND	–	GROUND	A25	A25	A22	A3	A3	A4		
B5	C4	C4	B23	B26	B26	PET(TX)p5	→	PER(RX) p5	A26	A26	A23	A4	A4	A5	S17 (PETp1)	S9 (RX1+)
B6	C5	C5	B24	B27	B27	PET(TX)n5	→	PER(RX)n5	A27	A27	A24	A5	A5	A6	S18 (PETn1)	S10 (RX1-)
B7	C6	C6	B25	B28	B28	GROUND	–	GROUND	A28	A28	A25	A6	A6	A7		
B8(SB0)	A2(SB0)	A2	B26	B29(2W-CLK)	B29(2W-CLK)	VSP0/SB0	↔	VSP0/SB0	A29(2W-CLK)	A29(2W-CLK)	A26	A1	A1(SB0)	A8(SB0)		
B9(SB1)	B2(SB1)	B2	B27	B30(2W-DATA)	B30(2W-DATA)	VSP1/SB1	↔	VSP1/SB1	A30(2W-DATA)	A30(2W-DATA)	A27	B1	B1(SB1)	A9(SB1)		
			B28	B31(VSP8/SB8)	B31(GROUND)	VSP8/SB8	–	VSP8/SB8	A31(GROUND)	A31(VSP8/SB8)	A28					
B10(SB2)	C2(SB2)	C2	B29	B32(GND)	B32(PERST#)	VSP2/SB2	→	VSP2/SB2	A32(PERST#)	A32(GND)	A29	C1	C1(SB2)	A10(SB2)	E5 (PERST#)	
B11(SB6)	D2(SB6)	D2	B30	B33(CNTR_TYPE)	B33(CPRSNT#)	VSP6/SB6	←	VSP6/SB6	A33(CPRSNT#)	A33 (CNTR_TYPE)	A30	D1	D1(SB6)	A11(SB6)		
B12	D6	D6	B31	B34	B34	GROUND	–	GROUND	A34	A34	A31	B6	B6	A12		
B13	D7	D7	B32	B35	B35	PET(TX)p6	→	PER(RX)p6	A35	A35	A32	B7	B7	A13	S23 (PETp2)	S17 (RX2+)
B14	D8	D8	B33	B36	B36	PET(TX)n6	→	PER(RX)n6	A36	A36	A33	B8	B8	A14	S24 (PETn2)	S18 (RX2)
B15	D9	D9	B34	B37	B37	GROUND	–	GROUND	A37	A37	A34	B9	B9	A15		
B16	C7	C7	B35	B38	B38	PET(TX)p7	→	PER(RX)p7	A38	A38	A35	A7	A7	A16	E17 (PETp3)	S23 (RX3+)
B17	C8	C8	B36	B39	B39	PET(TX)n7	→	PER(RX)n7	A39	A39	A36	A8	A8	A17	E18 (PETn3)	S24 (RX3-)
B18	C9	C9	B37	B40	B40	GROUND	–	GROUND	A40	A40	A37	A9	A9	A18		
														T10 15-118r3 8x Molex		
														SHEET 2 OF 2		