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SFF specifications are available at ftp://ftp.seagate.com/sff

SFF Committee

SFF-8418

Specification for

SFP+ 10 Gb/s Electrical Interface

Rev 1.4 July 30, 2015

Secretariat: SFF Committee

Abstract: This specification defines the high speed electrical interface specifications for 10 Gb/s SFP+ modules and hosts. The 8.5 Gb/s high speed electrical interface specifications are defined in FC-PI-4. The modules may optionally support lower signaling rates as well. The modules may be used to implement single-mode or multimode serial optical interfaces at 850 nm, 1310 nm, or 1550 nm. The SFP+ module design may use one of several different optical connectors.

This specification provides a common reference for systems manufacturers, system integrators, and suppliers. This is an internal working specification of the SFF Committee, an industry ad hoc group.

This specification is made available for public review, and written comments are solicited from readers. Comments received by the members will be considered for inclusion in future revisions of this specification.

Support: This specification is supported by the identified member companies of the SFF Committee.

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EXPRESSION OF SUPPORT BY MANUFACTURERS

The following member companies of the SFF Committee voted in favor of this industry specification:

Amphenol	JDS Uniphase
Arista	QLogic
Broadcom	Shinning Electronics
Finisar	Sichuan
GLGnet Electronics	Sumitomo
Hewlett Packard	TE Connectivity
HGST	

The following member companies of the SFF Committee voted against this industry specification.

Foxconn	Mellanox

The following member companies of the SFF Committee voted to abstain on this industry specification.

EMC	Seagate
FCI	

The user's attention is called to the possibility that implementation to this Specification may require use of an invention covered by patent rights. By distribution of this specification, no position is taken with respect to the validity of a claim or claims or of any patent rights in connection therewith. Members of the SFF Committee which advise that a patent exists are required to provide a statement of willingness to grant a license under these rights on reasonable and non-discriminatory terms and conditions to applicants desiring to obtain such a license.

Change History:

Rev 1.0 March 31, 2015
- Content derived from SFF-8431 Rev 4.2 excepting Sections 2.1-2.7 and 4
- Updated with current template, with exception that Table and Figure numbering is sequential and not within Section.
- Converted symbols to text and editorial corrections made to case, consistency of expression, etc.
- Adopted 10^ for consistent expression of powers (BER et al)
- Corrected references to SFF-8083 to be SFF-8071

Rev 1.1 May 8, 2015
- Added cross-references to SFF-8431 sections/tables/figures

Rev 1.2 June 2, 2015
- Corrected reference to SFF-8071 in C.1.2 to be SFF-8084
- Minor editorial changes as requested

Rev 1.3 June 11, 2015
- Transferred power supply Section 2 and Appendix D.17 to SFF-8419

Rev 1.4 July 30, 2015
- Updated 1.1.1 Industry Documents
- Corrected Table 1 reference to low speed test method to SFF-8419
- Corrected invalid symbol conversions on p36 and p56

Foreword

The development work on this specification was done by the SFF Committee, an industry group. The membership of the committee since its formation in August 1990 has included a mix of companies which are leaders across the industry.

When 2 1/2" diameter disk drives were introduced, there was no commonality on external dimensions e.g. physical size, mounting locations, connector type, connector location, between vendors.

The first use of these disk drives was in specific applications such as laptop portable computers and system integrators worked individually with vendors to develop the packaging. The result was wide diversity, and incompatibility.

The problems faced by integrators, device suppliers, and component suppliers led to the formation of the SFF Committee as an industry ad hoc group to address the marketing and engineering considerations of the emerging new technology.

During the development of the form factor definitions, other activities were suggested because participants in the SFF Committee faced more problems than the physical form factors of disk drives. In November 1992, the charter was expanded to address any issues of general interest and concern to the storage industry. The SFF Committee became a forum for resolving industry issues that are either not addressed by the standards process or need an immediate solution.

Those companies which have agreed to support a specification are identified in the first pages of each SFF Specification. Industry consensus is not an essential requirement to publish an SFF Specification because it is recognized that in an emerging product area, there is room for more than one approach. By making the documentation on competing proposals available, an integrator can examine the alternatives available and select the product that is felt to be most suitable.

SFF Committee meetings are held during T10 weeks (see www.t10.org), and Specific Subject Working Groups are held at the convenience of the participants. Material presented at SFF Committee meetings becomes public domain, and there are no restrictions on the open mailing of material presented at committee meetings.

Most of the specifications developed by the SFF Committee have either been incorporated into standards or adopted as standards by EIA (Electronic Industries Association), ANSI (American National Standards Institute) and IEC (International Electrotechnical Commission).

If you are interested in participating or wish to follow the activities of the SFF Committee, the signup for membership and/or documentation can be found at:
www.sffcommittee.com/ie/join.html

The complete list of SFF Specifications which have been completed or are currently being worked on by the SFF Committee can be found at:
ftp://ftp.seagate.com/sff/SFF-8000.TXT

If you wish to know more about the SFF Committee, the principles which guide the activities can be found at:
ftp://ftp.seagate.com/sff/SFF-8032.TXT

Suggestions for improvement of this specification will be welcome. They should be sent to the SFF Committee, 14426 Black Walnut Ct, Saratoga, CA 95070.

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FIGURES

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SFF Committee --

SFP+ 10 Gb/s Electrical Interface

1. Scope

This specification defines the electrical interfaces and their test methods between the SFP+ module and host board for operation up to 11.1 GBd. The high speed electrical interface between the host and SFP+ module is called SFI. SFI simplifies the module and leverages host based transmit pre-emphasis and host based receive equalization to overcome PCB and external media impairments.

SFI typically operates with one connector at the module interface and up to about 200 mm of improved FR4 material or 150 mm of standard FR4. The electrical interface is based on high speed, low voltage AC coupled logic with a nominal differential impedance of 100 Ohms.

The SFP+ specifications includes management, connector (SFF-8071), mechanical (SFF-8432), power supply and low speed signalling (SFF-8419), high speed signalling, and appendices providing parameter and test board definitions, and implementation and measurement descriptions

SFP+ modules are hot pluggable and active connections are powered by individual power connections for the transmitter (VccT) and the receiver (VccR). Multiple modules can share a single 3.3 V power supply with individual filtering for each VccT and VccR. Detailed power supply specifications are found in SFF-8419.

All SFP+ module compliance points are defined and measured through the mated reference test card as defined by C.3 . All SFP+ host compliance points are defined and measured through the mated reference test card as defined by C.2 .

The SFP+ module could be an electrical-to-optical or an electrical-to-electrical device intended to support one or more of the applications listed in Table 1.

It is expected that a range of SFP+ modules will operate on single-mode fiber, multimode fiber, and SFP+ electrical cable assemblies.

SFP+ compliant hosts are permitted to support just linear modules, just limiting modules, or both linear and limiting modules. Linear modules are modules which contain a linear receiver. Limiting modules are modules which contain a limiting receiver. Although not required, host supporting linear specifications are encouraged to support 10GSFP+Cu direct attach cables (Appendix E). For other copper variants see SFF-8461.

1.1 References

1.1.1 Industry Documents

IEEE 802.3	IEEE Standard for Ethernet *
INCITS 450	FC-PI-4 (Fibre Channel Physical Interface - 4 (T11/1647D)
INCITS 364	FC-10GFC (10 Gb/s)
INCITS TR-46	FC-MJSQ - Methodologies for Jitter and Signal Quality
OIF-CEI	Optical Internetworking Forum - Common Electrical I/O
INF-8074i	SFP (Small Formfactor Pluggable) 1 Gb/s Transceiver
INF-8077i	XFP 10 Gb/s 1X Pluggable Module
SFF-8071	SFP+ 1X 0.8mm Card Edge Connector
SFF-8083	SFP+ 1X 10 Gb/s Pluggable Transceiver Solution (SFP10)
SFF-8079	SFP Rate and Application Selection
SFF-8089	SFP Rate and Application Codes
SFF-8419	SFP+ Power and Low Speed Interface plus Matlab Code

SFF-8431	SFP+ 10 Gb/s and Low Speed Electrical Interface
SFF-8432	SFP+ 10 Gb/s Module and Cage
SFF-8472	Management Interface for SFP+

* Relevant clauses are 49, 10GBASE-R LAN PHY; 50, 10GBASE-W WAN PHY; 52, 10 Gigabit Ethernet serial PMDs; and 68, 10GBASE-LRM)

1.1.2 SFF Specifications

There are several projects active within the SFF Committee. The complete list of specifications which have been completed or are still being worked on are listed in the specification at ftp://ftp.seagate.com/sff/SFF-8000.TXT

1.1.3 Sources

Those who join the SFF Committee as an Observer or Member receive electronic copies of the minutes and SFF specifications (http://www.sffcommittee.com/ie/join.html).

Copies of ANSI standards may be purchased from the InterNational Committee for Information Technology Standards (http://www.techstreet.com/incitsgate.tmpl).

1.1.4 Conventions

The dimensioning conventions are described in ANSI-Y14.5M, Geometric Dimensioning and Tolerancing. All dimensions are in millimeters, which are the controlling dimensional units (if inches are supplied, they are for guidance only).

The ISO convention of numbering is used i.e., the thousands and higher multiples are separated by a space and a period is used as the decimal point. This is equivalent to the English/American convention of a comma and a period.

American	French	ISO
0.6	0,6	0.6
1,000	1 000	1 000
1,323,462.9	1 323 462,9	1 323 462.9

1.1.5 Abbreviations

64B/66B	Data encoded with 64B/66B encoder as defined by the IEEE Std. 802.3 CL 49.
BER	bit error ratio
CDR	clock and data recovery
CRU	clock recovery unit
dB	decibel. 10*log10(ratio of power quantities). Powers can be electrical or optical. Conventional usage. See also dBe and dBo.
dBe	Specific case of dB where signals are electrical. 10*log10(ratio of electrical power quantities). 20*log10(ratio of voltage quantities) can be used if reference impedances are equal.
dBm	decibel (relative to 1 mW)
dBo	Specific case of dB where the signals are in optical power. 10*log10(ratio of optical power quantities). Also, in certain cases with electrical signals relating to linear optical modules, where it is expected that electrical voltage is in proportion to optical power, 10*log10(ratio of voltage quantities).
DCD	Duty cycle distortion
DDPWS	Data Dependent Pulse Width Shrinkage
DDJ	Data Dependent Jitter
dRN	Difference of Relative noise see Appendix D
DUT	device under test
dWDP	Difference of the waveform distortion penalty of an optical receiver
dWDPc	Difference of the waveform distortion penalty of an electrical cable assembly
EMC	electromagnetic compatibility
EMI	electromagnetic Interference
FC	Fibre Channel
h	hexadecimal notation
HCB	Host Compliance Board
IEEE	Institute of Electrical and Electronics Engineers
ITU-T	ITU Telecommunication Standardization Sector
Gbit	gigabit = 10^(9) bits
GBd	Gigabaud
J2	99% Jitter
LRM	IEEE 802.3 CL68 Physical Layer Specifications for 10 Gb/s using 10GBASE-R encoding and long wavelength optics for multimode fiber
MCB	Module Compliance Board
OMA	optical modulation amplitude
PCB	printed circuit board
PRBS9	Pseudo-Random Bit Sequence 2e9-1, see D.1.1
PRBS31	Pseudo-Random Bit Sequence 2e31-1, see D.1.1
Qsq	a measure of SNR, see D.8 and IEEE 802.3.68.6.7
RI	random interference
RMS	root mean square
RN	relative noise
Rx	receiver
Rx_LOS	Loss of signal same as defined in FC PI-4 and the inverse of signal detect (SD) in 802.3
RSS	Root Sum of Squares

SD	Signal Detect
SerDes	Serializer/Deserializer
SFI	SFP+ high speed serial electrical interface
SNR	signal-to-noise ratio
VccT	Module positive power supply rail for the transmitter
VccR	Module positive power supply rail for the receiver
VMA	voltage modulation amplitude
Tx	transmitter
TWDP	Transmitter Waveform Distortion Penalty for an optical transmitter
TWDPc	Transmitter Waveform Distortion Penalty of a host transmitter supporting an electrical cable assembly
UI	unit interval = 1 symbol period
UJ	Uncorrelated Jitter
WDP	Waveform distortion penalty
WDPc	Waveform distortion penalty for an electrical cable assembly

1.2 The SFP+ Supported Standards

An SFP+ module may comply with any combination of the standards shown in Table 1, and may be suitable for other or future standards. This specification does not preclude operation at other signalling rates not listed in this table, such as 2.125 GBd for 2GFC, or 4.25 GBd for 4GFC.

Due to the possibility of insertion of classic SFP modules into a host designed for SFP+ the damage threshold of the host for the input signal at C (see Figure 2) shall be at least 2000 mV peak to peak differential.

TABLE 1 SFP+ STANDARD COMPLIANCE

Standard	Signaling Rate (GBd)	High Speed Serial Interface	High Speed Serial Test Method	Low Speed Electrical Definitions	Low Speed Test Methods	Management	Mechanical/ Connector
IEEE 802.3 Clause 38 or Clause 59 (1 Gb/s Ethernet)	1.25	802.3 Clause 38 or 59 Appendix F		SFF-8419	SFF-8419	SFF-8419 SFF-8472 SFF-8079 SFF-8089	SFF-8432 SFF-8071
1 GFC	1.0625	FC-PH	FC-PH				
2 GFC	2.125	FC-PI	FC-PI				
4 GFC	4.25	FC-PI-2	FC-PI-2				
8 GFC *	8.5	FC-PI-5	FC-PI-5				
16 GFC	14.025	FC-PI-5	FC-PI-5				
32 GFC	28.05	FC-PI-6	FC-PI-6				
10GSFP+Cu	10.3125	Section 3 Appendix E	Appendix D Appendix E				
IEEE 802.3 Clause 52 (10 Gb/s Ethernet LAN PHY)	10.3125	Section 3	Appendix D				
IEEE 802.3 Clause 52 (10 Gb/s Ethernet WAN PHY)	9.95328						
IEEE 802.3 Clause 68 (LRM)	10.3125						
10 GFC	10.51875						
10GBASE-R (IEEE 802.3 Clause 49) Encapsulated in G.709 ODU-2 Frame (FEC)	11.10						
* 8GFC specifications revised in FC-PI-5 and override FC-PI-4 requirements							

1.3 SFI Typical PCB Reach (Informative)

The SFI channel may be implemented with either microstrip or stripline structures. Example host board designs with typical PCB trace reaches are shown in Table 2. Detailed channel properties and recommendations are documented in Appendix A

TABLE 2 HOST BOARD ACHIEVABLE TRACE LENGTH

Type	Material	Trace Width (mm)	Loss Tangent	Copper Thickness (oz) *	Copper Thickness (um)	Trace Length (mm)
Microstrip	FR4-6/8	0.3	0.022	1.0	35.0	200
	Nelco 4000-13	0.3	0.016	1.0	35.0	300
Stripline	FR4-6/8	0.125	0.022	0.5	17.5	150
	Nelco 4000-13	0.125	0.016	0.5	17.5	200
* Copper (oz) is an ounce of copper over one square foot of laminate.						

2. Power and Low Speed Electrical Specifications

Section 2, Section 4, Appendix D.17 and Appendix G of SFF-8431 SFP+ 10 Gb/s and Low Speed Electrical Interface were removed to create the SFF-8419 specification. This was done to separate module management's low speed interface from 10 Gb/s operation, so SFF-8419 could be referenced by later generations of a higher speed.

3. High Speed Electrical Specification SFI

3.1 Introduction

SFI signalling is based on differential high speed low voltage logic with AC-coupling in the module. SFI was developed with the primary goal of low power and low electromagnetic interference (EMI). To satisfy this requirement the nominal differential signal levels are ~500 mV p-p with edge speed control to reduce EMI. SFP+ compliant hosts are allowed to support just linear modules, just limiting modules, or both linear and limiting modules.

3.2 SFI Applications Definition

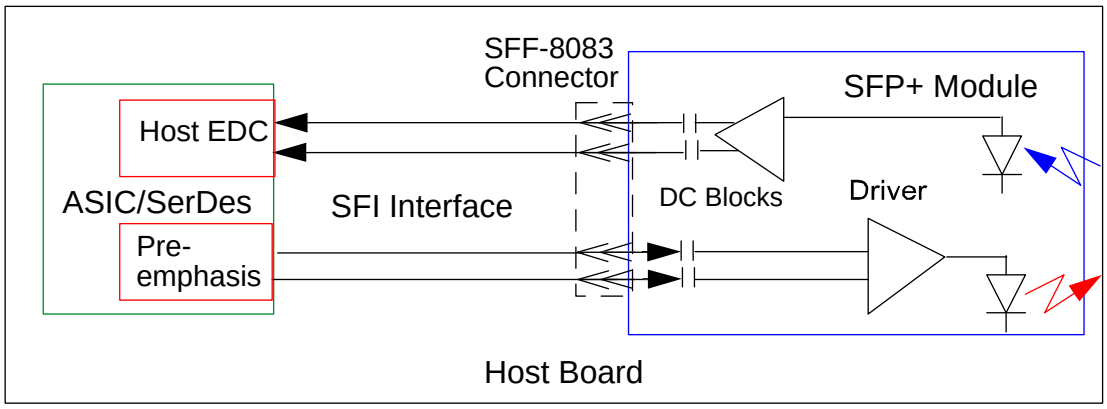
The application reference model for SFI connects a high speed ASIC/SERDES to the SFP+ module as shown in Figure 1.

The SFI interface is designed to support IEEE 802.3 10Gig standards Clauses 49, 50, and 51, and 10GFC. For all other FC signalling rates see FC-PI-4. SFI supported signalling rates are listed in Table 3. SFP+ compliant modules and hosts may support one or more of the signalling rates listed in Table 3. For 10GSFP+Cu (direct attach copper) specifications and applications reference model, see Appendix E.

TABLE 3 SFI SUPPORTED SIGNALLING RATES

Standard	Description	Signaling Rate	Unit
IEEE std-802.3 Clause 50	10GBASE-W WAN PHY	9.95328	GBd
IEEE std-802.3 Clause 49	10GBASE-R LAN PHY	10.3125	GBd
Fibre Channel - 10 Gigabit	10GFC	10.51875	GBd
10Gig Ethernet with FEC	10GBASE-R over G.709	11.10	GBd

The SFI interface operates from 9.95 to 11.1 GBd.



Note: SFF-8083 contents transferred to SFF-8071

FIGURE 1 SFI APPLICATION REFERENCE MODEL

3.3 SFI Test Points Definition and Measurements

SFI reference compliance test points are defined with the Host Compliance Board and the Module Compliance Board for measurement consistency, see Appendix C. The reference test boards provide a set of overlapping measurements for ASIC/SerDes,

module, and host validation to ensure interoperability. For improved measurement accuracy the actual reference test card responses may be calibrated out of the measurements and replaced with functions that represent the ideal responses defined in Appendix C for the reference test cards.

Points A, B, C, and D require AC coupled test equipment. All SFI test equipment must have 50 Ohms single ended impedance on all test ports.

The reference impedance for differential measurements and S-parameters is 100 Ohms, and the reference impedance for common mode measurements and S-parameters is 25 Ohms.

The bandwidth of measurement instrument shall be 12 GHz unless specified otherwise. SFI reference points are listed in Table 4.

TABLE 4 SFI REFERENCE POINTS

Compliance point	Designation
ASIC/SerDes output	A
Host output	B
Host input	C
ASIC/SerDes input	D
Module input	B'
Module output	C'
Module input calibration	B'' (double quotation)
Host input calibration	C'' (double quotation)

3.3.1 Host Compliance Points

Host system transmitter and receiver compliance are defined by tests in which a Host Compliance Board is inserted as shown in place of the SFP+ module. The Host Compliance Board meets the specifications of Appendix C. The compliance points are B and C.

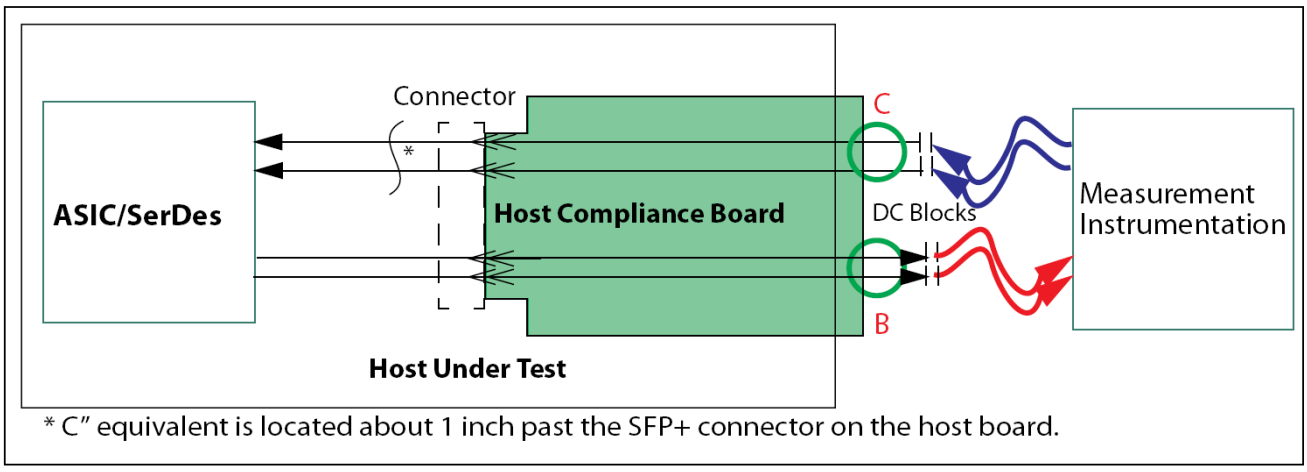


FIGURE 2 HOST COMPLIANCE BOARD

SFP+ host compliance points are defined as the following:

B Host transmitter output at the output of the Host Compliance Board. Specifications for B are given in Section 3.5.1.
C Host receiver input at the input of the Host Compliance Board. Specifications for C are given in Section 3.5.2.

3.3.2 Module Compliance Points

Module transmitter and receiver compliance are defined by tests in which the module is inserted into the Module Compliance Board. The Module Compliance Board meets the specifications of Appendix C. The compliance points for the module are B' and C'.

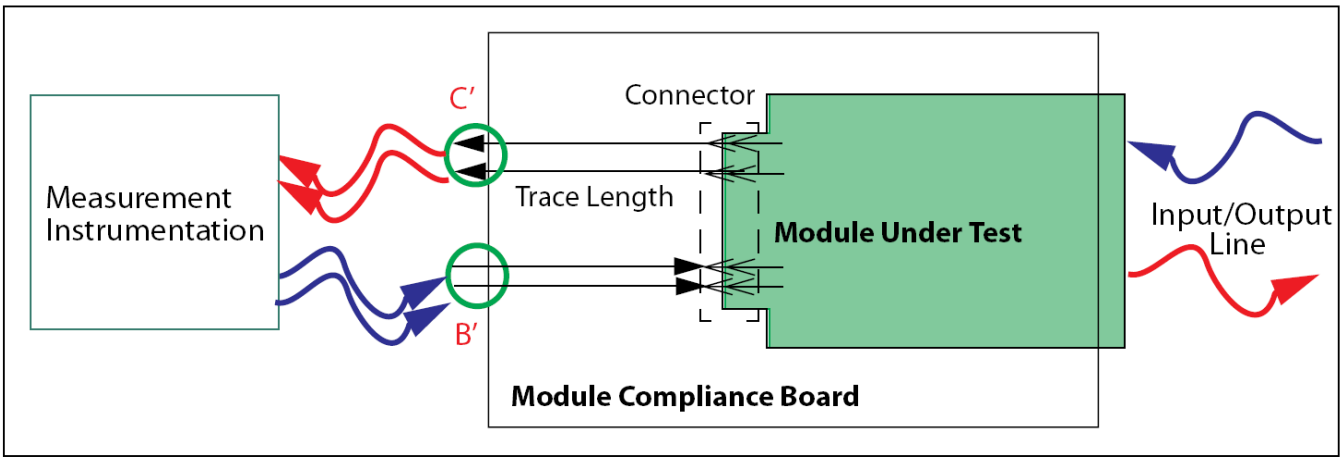


FIGURE 3 MODULE COMPLIANCE BOARD

SFP+ module compliance points are defined as the following:

B' SFP+ module transmitter input at the input of the Module Compliance Board. Specifications for B' are given in Section 3.6.1.
C' SFP+ module receiver output at the output of the Module Compliance Board. Specifications for C' are given in Section 3.6.2.

3.3.3 ASIC/SerDes Test Points (Informative)

ASIC/SerDes transmitter and receiver may be tested on a test board as shown in Figure 4 with nominal trace response as specified by C.1.3 to avoid degradation due to excessive trace loss and to ensure consistent measurements.

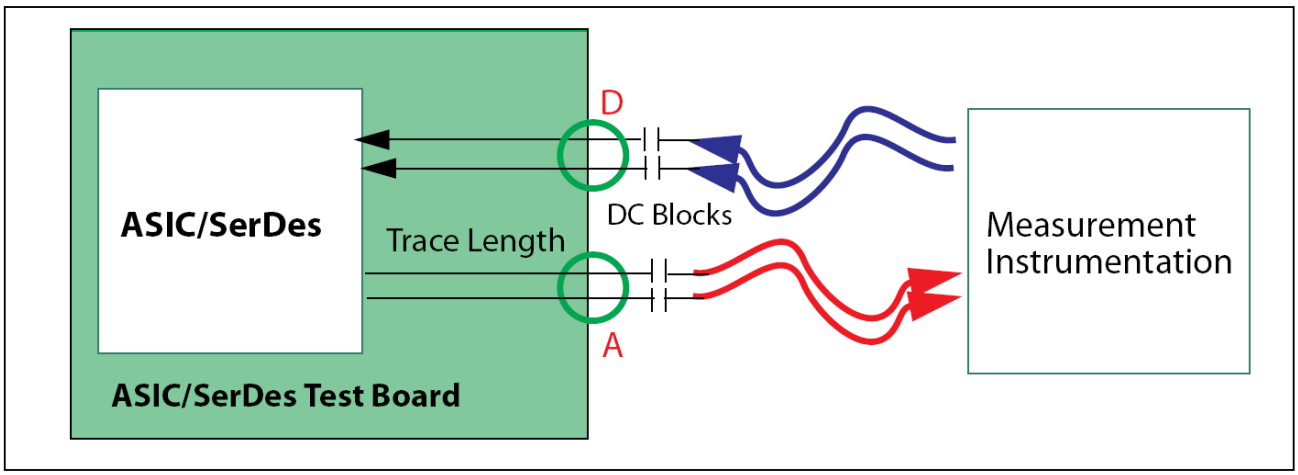


FIGURE 4 ASIC/SERDES TEST BOARD

SFI ASIC/SerDes test points are defined as the following:

A SerDes transmitter output at the output of the ASIC/SerDes Test Board. Recommendations for A are given in B.2.

D ASIC/SerDes receiver input at the input of the ASIC/SerDes Test Board. Recommendations for D are given in B.3.

3.3.4 Host Input Calibration Point

Host receiver input tolerance signals are calibrated through the Host Compliance Board at the output of the Module Compliance Board as shown in Figure 5. The host input calibration point is at C'' with specifications for C'' given in 3.5.2. The response between the connector and C'' is specified by C.1.2.

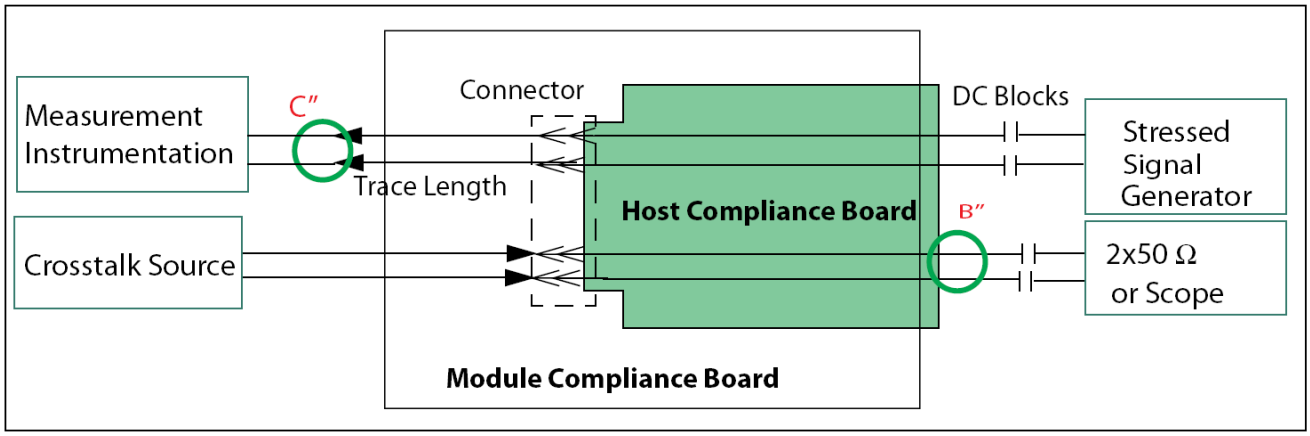


FIGURE 5 HOST INPUT CALIBRATION POINT C'' AND CROSSTALK SOURCE CALIBRATION POINT B''

3.3.5 Module Input Calibration Point

Module transmitter input tolerance signals are calibrated through the Module Compliance Board at the output of the Host Compliance Board as shown in Figure 6. The module input calibration point is at B'' with specifications for B'' given in Section 3.6.1. The response between the connector and B'' is specified by C.1.1.

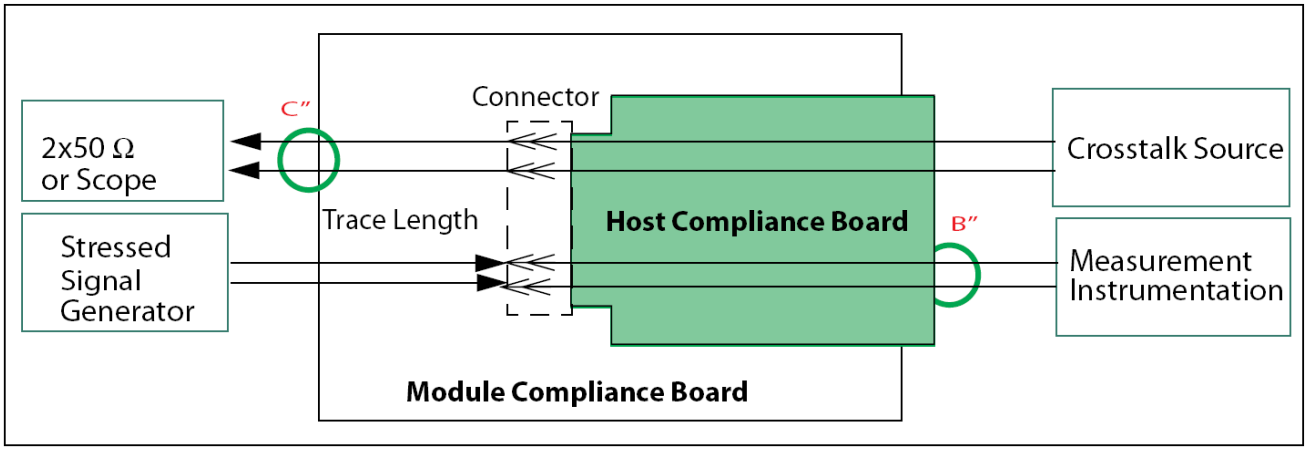


FIGURE 6 MODULE INPUT CALIBRATION POINT B'' AND CROSSTALK SOURCE CALIBRATION POINT C''

3.4 SFI Termination and DC Blocking

The SFI link uses nominal 100 Ohms differential source and load terminations on both the host board and the module. The SFI transmitter provides both differential and common mode termination. The SFI transmitter and receiver termination specifications for each of the compliance points are given by:

- Host: 3.5 SFP+ Host System Specifications
- Module: 3.6 SFP+ Module Specifications

Host SerDes termination recommendations are given by:

- ASIC/SerDes (Appendix B)

SFP+ modules shall incorporate blocking capacitors or equivalent on all SFI inputs and outputs as shown in Figure 7. The SFI transmitter is represented by terminations Zp and Zn which form a 100 Ohms differential source. Each termination has a nominal value of 50 Ohms, and therefore the common mode impedance is 25 Ohms. The SFI receiver is represented with termination Zdiff with nominal 100 Ohms value. This representation is not intended to preclude the use of other implementations which may provide common mode termination, however the SFI specification does not require any common mode termination at the receiver. If common mode terminations are provided, it may reduce common mode voltage and EMI.

It is recommended that both the module and the host use transmission lines targeted to have 100 Ohms differential impedance with about 7% coupling. SFP+ percent differential coupling is defined by the following equation:

$$Coupling = \frac{Zcm \times 4 - Zdiff}{Zcm \times 4 + Zdiff} \times 100$$

Where Zcm is the common mode impedance and Zdiff is the differential impedance.

Differential traces with nominal 7% coupling offer a good compromise between reasonable common mode match and practical transmission line geometries. These are the targets for the module and host Compliance Boards described in Appendix C.

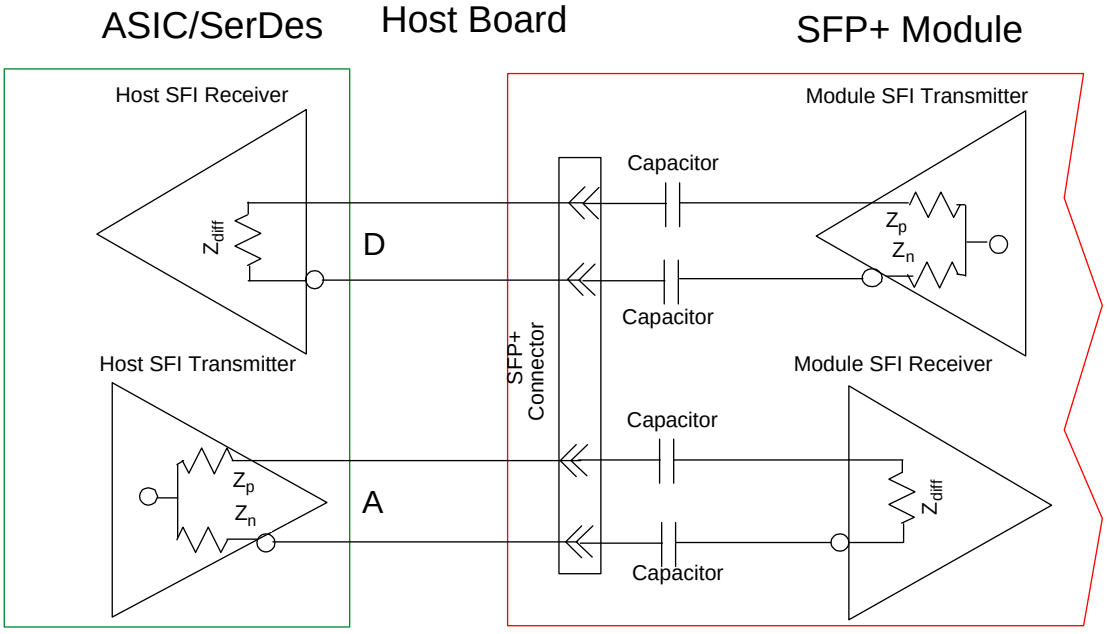


FIGURE 7 SFI TERMINATION AND AC COUPLING

3.5 SFP+ Host System Specifications

SFP+ host system transmitter specifications at compliance point B are given in Section 3.5.1. SFP+ Host system receiver specifications at compliance point C are

given in Section 3.5.2.

All specifications are to be met at the host compliance test points defined in Section 3.3.1.

The solder pads for the high speed traces in the SFF-8431 Module Compliance Board are 1.1x0.4 mm to improve high frequency performance instead of 2.0x0.5 mm as defined in the SFF-8071 for improved manufacturability. Trade-off between host performance and manufacturability are left to the host designer. For detailed geometry of the Module Compliance Board, see the Gerber files in Section C.3.4.

Warning: The host expects DC blocking in the module, and for improved performance the Host Compliance Board is not required to incorporate DC blocks. DC blocking within the test equipment or between the host and the equipment is necessary for all host SFI signals.

3.5.1 Host Transmitter Output Specifications at B

SFP+ host transmitter electrical specifications defined at compliance point B are given in Table 5 and Table 6. These specifications are defined at the output of the Host Compliance Board specified in C.2 . Host transmitters must provide adequate low frequency signal response for the applications supported.

TABLE 5 HOST TRANSMITTER OUTPUT ELECTRICAL SPECIFICATIONS AT B

Parameter - B	Symbol	Conditions	Min	Max	Unit
Termination Mismatch at 1 MHz	DeltaZm	See D.16 , Figure 36		5	%
Single Ended Output Voltage Range			-0.3	4.0	V
Output AC Common Mode Voltage		See 3.6.2D.15		15	mV (RMS)
Differential Output S-parameter	SDD22	0.01 to 2 GHz		-12	dB
		2 to 11.1 GHz		*1	dB
Common Mode Output S-parameter	SCC22	0.01 to 2.5 GHz		*2	dB
		2.5 to 11.1 GHz		-3	dB
*1 Reflection coefficient given by equation SDD22(dB) < -6.68 + 12.1 x log10(f/5.5), with f in GHz *2 Reflection coefficient given by equation SCC22(dB) < -7 + 1.6 x f, with f in GHz					

The specification of common mode output return loss reduces EMI and noise by absorbing common mode reflections and noise.

The SFI jitter specifications at reference point B are listed in Table 6 and the compliance mask is shown in Figure 8. As baseline wander can create low probability eye closure which is not detected by the 5x10-5 mask hit ratio, baseline wander must be controlled so as not to significantly degrade the signal at B.

TABLE 6 HOST TRANSMITTER OUTPUT JITTER AND EYE MASK SPECIFICATIONS AT B

Parameters- B	Symbol	Conditions	Min	Target Value	Max	Unit
Crosstalk Source Rise/Fall time (20% to 80%)	Tr, Tf	*1 *2 D.6		34		ps
Crosstalk Source Amplitude (p-p differential)		*1 *2 D.7		1000		mV
Signal Rise/Fall time (20% to 80%)	Tr, Tf	See D.6	34			ps
Total Jitter	TJ	See D.5			0.28	UI(p-p)
Data Dependent Jitter	DDJ	See D.3			0.1	UI(p-p)
Data Dependent Pulse Width Shrinkage	DDPWS				0.055	UI(p-p)
Uncorrelated Jitter	UJ	*3 and D.4			0.023	UI (RMS)
Transmitter Qsq	Qsq	*4	50			

Parameters- B	Symbol	Conditions	Value	Unit
Eye Mask	X1	Mask hit ratio of 5 x 10^(-5) See D.2 and Figure 8	0.12	UI
Eye Mask	X2		0.33	UI
Eye Mask	Y1		95	mV
Eye Mask	Y2		350	mV

*1 Measured at C'' with Host Compliance Board and Module Compliance Board pair, see Figure 6
*2 Since the minimum module output transition time is faster than the crosstalk transition time the amplitude of crosstalk source is increased to achieve the same slew rate.
*3 It is not possible to have the maximum UJ and meet the TJ specifications if the UJ is all Gaussian.
*4 Qsq=1/RN if the one level and zero level noises are identical and see D.8 .

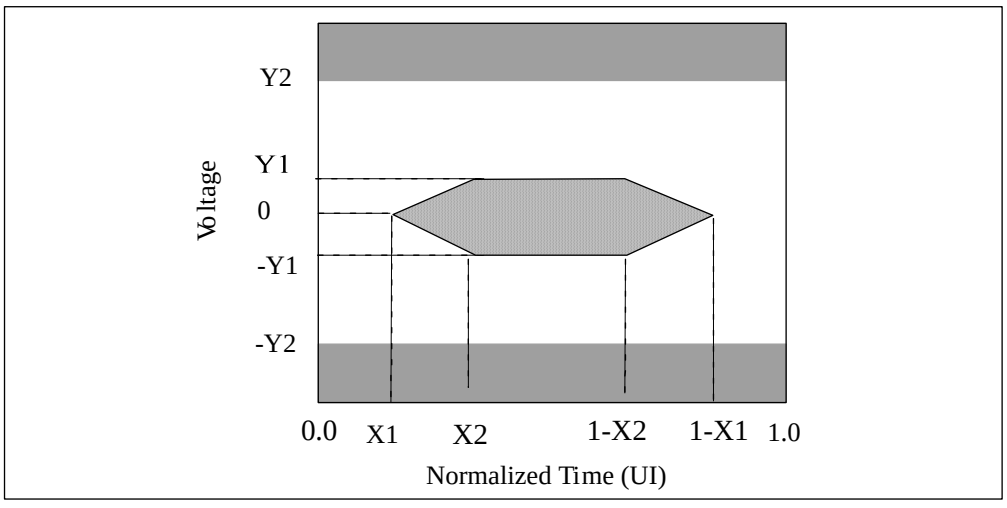


FIGURE 8 TRANSMITTER DIFFERENTIAL OUTPUT COMPLIANCE MASK AT B AND B''

3.5.2 Host Receiver Input Specifications at C and C''

The SFP+ Host receiver electrical specifications at compliance point C and C'' for both linear and limiting modules are given in Table 7. The host shall provide differential termination and must constrain differential to common mode conversion for quality signal termination and low EMI, as given in Table 7. Common mode

termination on the receiver is not required see Figure 7.

Signals used as input tolerance test conditions are calibrated at C'' with the Host Compliance Board connected through a Module Compliance Board to measurement instrumentation. Specifications at C'' supporting limiting modules are given in Table 8. Specifications at C'' supporting linear module are given in Table 9.

SFP+ compliant hosts are allowed to support just linear modules, just limiting modules, or both linear and limiting modules.

TABLE 7 HOST RECEIVER INPUT ELECTRICAL SPECIFICATIONS AT C AND C''

Parameters- C and C''	Symbol	Conditions	Min	Target Value	Max	Unit
Single Ended Input Voltage Range		Referenced to VeeR	-0.3		4.0	V
Input AC Common Mode Voltage Tolerance		*1 and D.15.3	7.5			mV (RMS)
Damage Threshold (p-p differential)		*1	2000			mV
Differential Input S-parameter	SDD11	0.01 to 2 GHz			-12	dB
		2 to 11.1 GHz			*2	dB
Reflected Differential to Common Mode Conversion	SCD11	0.1 to 11.1 GHz			-10	dB
*1 Measured at C'' with the Module Compliance Board *2 Reflection Coefficient given by equation SDD11(dB) < -6.68 + 12.1 x log10(f/5.5), with f in GHz						

Jitter specifications to support the limiting module are listed in Table 8. Figure 9 gives the host compliance eye mask requirements to support the limiting module. The host shall operate at and between the sensitivity and overload limits. The SFP+ limiting host shall tolerate sinusoidal jitter given by Figure 10. Test procedures for the host for limiting module are given in D.11 .

TABLE 8 HOST RECEIVER SUPPORTING LIMITING MODULE INPUT COMPLIANCE TEST SIGNAL CALIBRATED AT C''

Parameters- C''	Symbol	Conditions	Target Value	Max	Unit
Crosstalk Source Rise/Fall time (20% to 80%)	Tr, Tf	See D.6	34		ps
Crosstalk Source Amplitude (p-p differential)		*1	700		mV
AC Common Mode Voltage		*2 and D.15		7.5	mV (RMS)
99% Jitter	J2	*3, D.5 , D.11	0.42		UI(p-p)
Pulse Width Shrinkage Jitter	DDPWS	*4, D.3	0.3		UI(p-p)
Total Jitter	TJ	BER 1 x 10^(-12) see D.5 , D.11	0.70		UI(p-p)
Eye Mask	X1	Mask hit ratio of 1 x 10^(-12) See D.2 , D.11	0.35		UI
Eye Mask Amplitude Sensitivity 5,8	Y1		150		mV
Eye Mask Amplitude Overload 6,7,8	Y2		425		mV

*1 Measured at B'' with Host Compliance Board and Module Compliance Board pair, see Figure 5
*2 The tester is not expected to generate this common mode voltage however its output must not exceed this value.
*3 Includes sinusoidal jitter, per Figure 10, when measured with the reference PLL specified by the given standard.
*4 In practice the test implementer may trade DDPWS with other pulse width shrinkage from the sinusoidal interferer.
*5 Eye mask amplitude sensitivity tests the host receiver with the minimum eye opening expected from a module within the constraint set by Y2.
*6 Eye mask amplitude overload tests the host receiver tolerance to the largest peak signal levels expected from the module within the constraint set by Y1.
*7 It is not expected that module Rx output will exhibit both maximum peak level and minimum eye opening.
*8 Sensitivity and overload are tested separately, see D.11

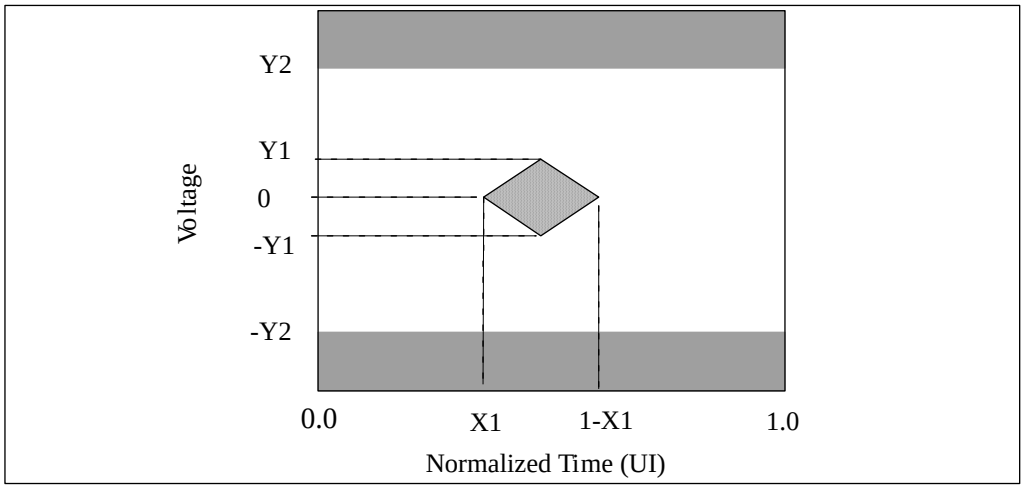


FIGURE 9 HOST RECEIVER INPUT COMPLIANCE MASK AT C'' SUPPORTING LIMITING MODULE

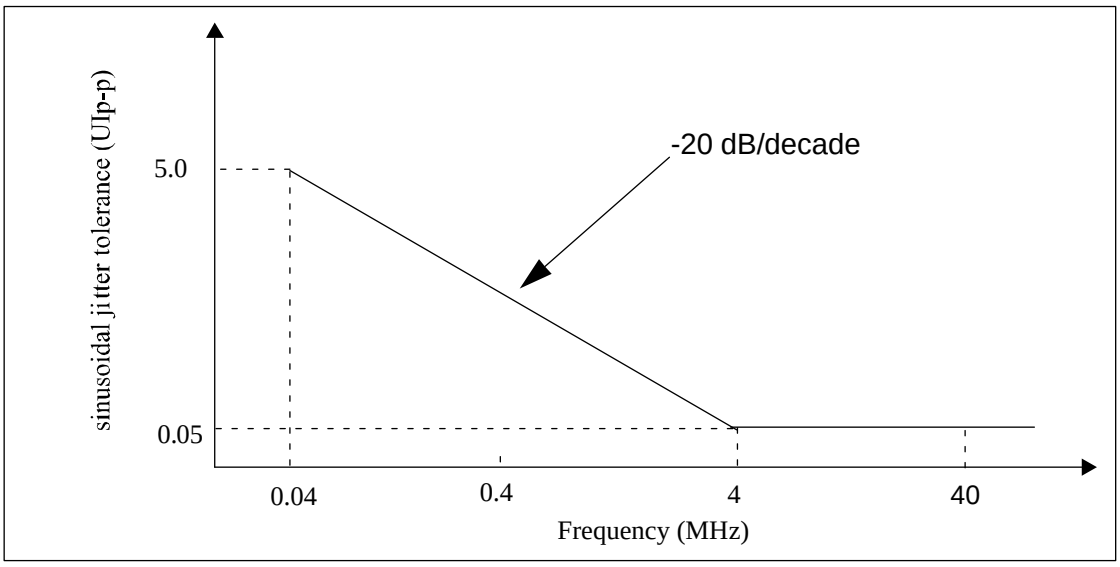


FIGURE 10 SR AND LR HOST SINUSOIDAL JITTER TOLERANCE MASK

Table 9 defines the input compliance test signal as calibrated at C'' for a host that supports linear modules. The parameters in Table 9 include the effects of a worst case module that operates in conjunction with optical TP3 tester(s) defined for the LRM and LR standards. SR specifications are covered by the fact that LR links have high noise, and on the other extreme, LRM links have high distortion. Test procedures for the linear host are given in D.13 . For illustrative purpose, Figure 13 shows the host test calibration line along which specific host test points for LRM are defined.

For LR test conditions, the SFP+ linear host shall operate with sinusoidal jitter given by Figure 10 while the stress conditions given in Table 9 are applied. For LRM test conditions, the host shall operate with sinusoidal jitter as defined in IEEE802.3, clause 68, with the stressors and noises in Figure 33 including those in the TP3 tester turned off.

Only two specific test conditions for each LRM stressor are defined in Table 9. In general, however, a host must meet operational requirements with any compliant module. It is expected that lower dWDP modules will exist. However, this specification has not defined host test conditions below dWDP of 0.6 to 0.8 dB. At low dWDP values, guard bands between module specifications and host requirements are left to the host implementation.

TABLE 9 HOST RECEIVER SUPPORTING LINEAR MODULE INPUT COMPLIANCE TEST SIGNAL CALIBRATED AT C''

Parameters- C''	Symbol	Conditions	Min	Target	Max	Unit
Crosstalk Source Rise/Fall time (20% to 80%)	Tr/Tf	*1 D.6		34		ps
Crosstalk Source Amplitude (p-p differential)		*1		700		mV
AC Common Mode Voltage		*2 and D.15			7.5	mV (RMS)
Differential Voltage Modulation Amplitude	VMA	for LRM, *3	180		600	mV
Differential Voltage Modulation Amplitude	VMA	for SR and LR, *3	150		600	mV

Applications	Symbol	Compliance stress test conditions *4 *7 and D.13	Target WDP (dBo)	Target RN, (RMS)		WDPi (dBo)
				mu	beta	
LRM	WDP	High WDP & pre-cursor stressor	Approximately 5.1, *5	-0.0148	0.0477	4.1
	WDP	High WDP & split-symmetric stressor	5.4			3.9
	WDP	High WDP & post-cursor stressor	Approximately 5.2, *5			4.2
	WDP	Low WDP & pre-cursor stressor	Approximately 4.7, *6			4.1
	WDP	Low WDP & split-symmetric stressor	Approximately 4.7, *6			3.9
	WDP	Low WDP & post-cursor stressor	Approximately 4.8, *6			4.2
LR	WDP	Low WDP	Approximately 2.6, *6	-0.02	0.096	1.9

*1 Measured at B'' with Host Compliance Board and Module Compliance Board pair, see Figure 5
*2 The tester is not expected to generate this common mode voltage, however its output must not exceed this value.
*3 Peak levels of received signals in service may exceed their VMA due to overshoot of the far end transmitter and/or the module receiver.
*4 Target WDP is calibrated with a reference receiver with 14 T/2 spaced FFE taps and 5 T spaced DFE taps.
*5 The filter bandwidth in the TP3 to electrical adapter in Figure 33 is set to produce 5.4 dBo for WDP for the split-symmetrical TP3 stressor. The same filter is to be used for high WDP pre-cursor and post-cursor LRM stressors - their approximate target WDP values are given only for guidance. WDP is to be measured for each stressor, and target RN is determined by the relevant equation in *7.
*6 The filter bandwidth in the TP3 to electrical adapter in Figure 33 is set to 7.5 GHz for all three LRM low WDP conditions and for the LR condition. The approximate target WDP values are given for guidance. WDP is to be measured for each stressor, and target RN is determined by the relevant equation in *7.
*7 Target RN rms values are given by the following equation:
RN = m x (WDP - WDPi), where WDP is the actual value of the tester, and WDPi values are based on waveshapes expected at TP3.

3.6 SFP+ Module Specifications

SFP+ module transmitter specifications at compliance point B' are given in Section 3.6.1. SFP+ module receiver specifications at compliance point C' are given in Section 3.6.2.

3.6.1 Module Transmitter Input Specifications at B' and B''

The SFP+ module transmitter electrical specifications, given in Table 10, at compliance point B' are measured with the Module Compliance Board as shown in Section 3.3.2. The transmitter input impedance is 100 Ohms differential. The module must provide differential termination and limit differential to common mode conversion for quality signal termination and low EMI.

Signals used as input conditions for testing the transmitter input tolerance are calibrated at B'' with the Module Compliance Board connected through a Host Compliance Board to appropriate instrumentation. This is further described in D.10 . The specifications used for this calibration are listed in Table 11. The test signal at B'' as illustrated by Figure 6 shall comply with the mask defined in Table 11 and illustrated in Figure 8.

TABLE 10 MODULE TRANSMITTER INPUT ELECTRICAL SPECIFICATIONS AT B'

Parameters- B'	Symbol	Conditions	Min	Target	Max	Unit
Single Ended Input Voltage Tolerance		Referenced to VeeT	-0.3		4.0	V
AC common mode voltage tolerance		*1, D.15.3	15			mV
Differential Input S-parameter	SDD11	0.01 to 4.1 GHz			*2	dB
		4.1 to 11.1 GHz			*3	dB
Reflected Differential to Common Mode Conversion	SCD11	0.01 to 11.1 GHz			-10	dB

*1 Measured at B'' with Host Compliance Board and Module Compliance Board pair, see Figure 6
*2 Reflection Coefficient given by equation SDD11(dB)< -12 + 2 x SQRT(f), with f in GHz.
*3 Reflection Coefficient given by equation SDD11(dB)< -6.3 + 13 x log10(f/5.5), with f in GHz

TABLE 11 MODULE TRANSMITTER INPUT TOLERANCE SIGNAL CALIBRATED AT B''

Parameters- B''	Symbol	Conditions	Target Value	Max	Unit
Crosstalk Source Rise/Fall time (20% to 80%)	Tr, Tf	*1 *2 and D.6	34		ps
Crosstalk Source Amplitude (p-p differential)		*1 *2	1000		mV
AC Common Mode Voltage		*3 and D.15.2		15	mV (RMS)
Total Jitter	TJ	*D.5		0.28	UI(p-p)
Data Dependent Jitter	DDJ	*D.3	0.10		UI(p-p)
Pulse Width Shrinkage Jitter	DDPWS		0.055		UI(p-p)
Uncorrelated Jitter	UJ	*4 and D.4	0.023		UI(RMS)

Parameters- B''	Symbol	Conditions	Value	Unit
Eye Mask	X1	Mask hit ratio of 5 x 10^(-5), See D.2	0.12	UI
Eye Mask	X2		0.33	UI
Eye Mask	Y1		95	mV
Eye Mask	Y2		350	mV

*1 Measured at C'' with Host Compliance Board and Module Compliance Board pair, see Figure 6
*2 Since the minimum module output transition time is faster than the crosstalk transition time the amplitude of crosstalk source is increased to achieve the same slew rate.
*3 The tester is not expected to generate this common mode voltage however its output must not exceed this value
*4 It is not possible to have the maximum UJ and meet the TJ specifications if the UJ is all Gaussian.

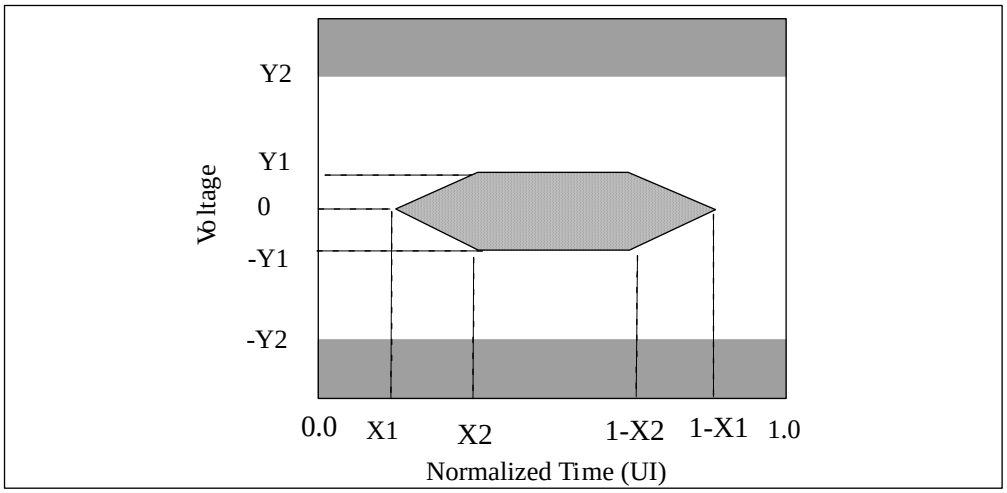


FIGURE 11 MODULE TRANSMITTER DIFFERENTIAL INPUT COMPLIANCE MASK AT B''

3.6.2 Module Receiver Output Specifications at C'

The SFP+ receiver electrical output specifications at compliance point C' are given in Table 12. The module must provide differential termination and common mode termination for quality signal termination and low EMI, as given in Table 12.

TABLE 12 MODULE RECEIVER OUTPUT ELECTRICAL SPECIFICATIONS AT C'

Parameters- C'	Symbol	Conditions	Min	Target	Max	Unit
Crosstalk source rise/fall time (20% to 80%)	Tr, Tf	*1, D.6		34		ps
Crosstalk Source Amplitude (p-p differential)		*1		700		mV
Termination Mismatch at 1 MHz	DeltaZm	See D.16 , Figure 36			5	%
Single Ended Output Voltage Tolerance			-0.3		4.0	V
Output AC Common Mode Voltage		See D.15			7.5	mV (RMS)
Differential Output S-parameter	SDD22	0.01 to 4.1 GHz			*2	dB
		4.1 to 11.1 GHz			*3	dB
Common Mode Output Reflection Coefficient	SCC22	0.01 to 2.5 GHz			*4	dB
		2.5 to 11.1 GHz			-3	dB

*1	Measured at B'' with the Host Compliance Board and Module Compliance Board pair, see Figure 5
*2	Reflection Coefficient given by equation SDD22(dB)< -12 + 2 x SQRT(f), with f in GHz.
*3	Reflection Coefficient given by equation SDD22(dB)< -6.3 + 13 x log10(f/5.5), with f in GHz
*4	Reflection coefficient given by equation SCC22(dB) < -7 + 1.6 x f, with f in GHz.

Common Mode Output Reflection Coefficient helps absorb reflection and noise improving EMI.

Jitter specifications for limiting modules are listed in Table 13. Figure 12 gives the compliance eye mask for limiting modules output. Requirements for linear modules are given in Table 14.

Both limiting and linear modules must provide adequate low frequency signal response for the applications supported, to control the effects of baseline wander.

TABLE 13 LIMITING MODULE RECEIVER OUTPUT JITTER AND EYE MASK SPECIFICATIONS AT C'

Parameters- C'	Symbol	Conditions	Min	Target	Max	Unit
Output Rise and Fall time (20% to 80%)	Tr, Tf	See D.6	28			ps
Total Jitter	TJ	See D.5 , D.12			0.70	UI(p-p)
99% Jitter	J2	See D.5 , D.12			0.42	UI(p-p)

Parameters- C'	Symbol	Conditions	Value	Unit
Eye Mask	X1	Mask hit ratio of 1 x 10^(-12) See D.2 , D.12	0.35	UI
Eye Mask	Y1		150	mV
Eye Mask	Y2		425	mV

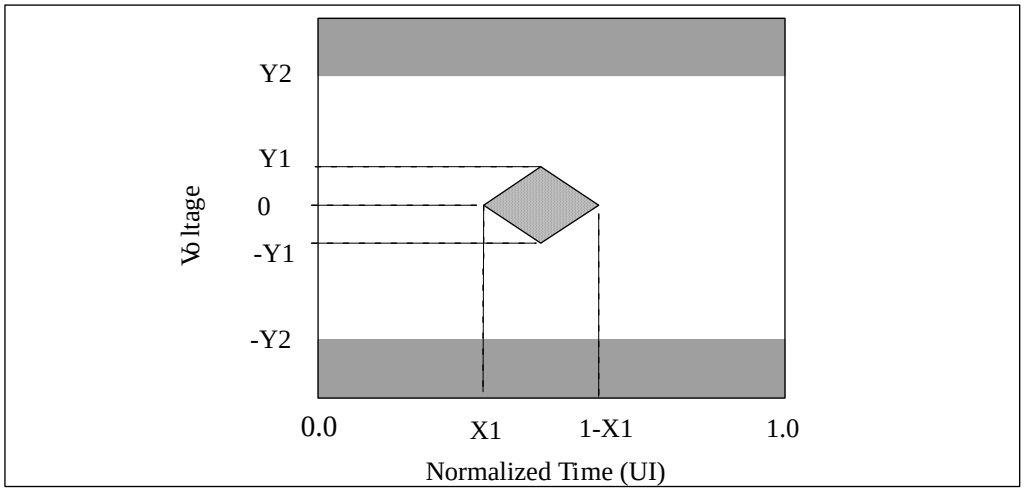


FIGURE 12 LIMITING MODULE RECEIVER DIFFERENTIAL OUTPUT COMPLIANCE MASK AT C'

Linear module test parameters are given by Table 14. Compliance methods for a linear module are given in Appendix D.14 .

TABLE 14 LINEAR MODULE RECEIVER SPECIFICATIONS AT C'

Parameters- C'	**Symbol**	**Conditions**	**RN**				
			m1	**b1**	**m2**	**b2**	**RNmax**
Relative Noise SR	RN	See D.14.1	-0.02	0.078	-0.02	0.078	0.078
Relative Noise LR			-0.02	0.083	-0.02	0.083	0.083
Relative Noise LRM with pre-cursor stressor			-0.0153	0.0475	-0.0092	0.0457	0.0475
Relative Noise LRM with split-symmetrical stressor			-0.017	0.0475	-0.01	0.0455	0.0475
Relative Noise LRM with post-cursor stressor			-0.0153	0.0475	-0.0092	0.0457	0.0475
Parameters- C'	**Symbol**	**Conditions**		**Min**		**Max**	**Unit**
Difference Waveform Distortion Penalty for SR and LR	dWDP	*1 and D.14.2				2.7	dBo
Difference Waveform Distortion Penalty for LRM	dWDP					1.5	dBo
Differential Voltage Modulation Amplitude For SR and LR	VMA	See D.7		150		600	mV
Differential Voltage Modulation Amplitude For LRM	VMA			180		600	mV
Differential peak to peak voltage	Vpk-pk	See D.14.3				600	mV
*1 Defined with reference receiver with 14 T/2 spaced FFE taps and 5 T spaced DFE taps.							

Appendix D.14.2 defines RN for a linear module receiver. The limits for RN are functions of measured dWDP for the module, expressed in optical decibels. As an example, the trade-off between the parameters for LRM are shown in Figure 13. To pass, RN must be below the respective limit line.

dWDP and RN shall meet the specifications in Table 14 and can be calculated by

$$RN \leq min[(m1 \times dWDP + b1), (m2 \times dWDP + b2), RNmax]$$

for each TP3 test condition for which compliance is required. For example, if compliance is required for LRM, the module must meet specifications with all three stressors and under the sensitivity and overload test conditions specified in IEEE Std 802.3 68.6.9.

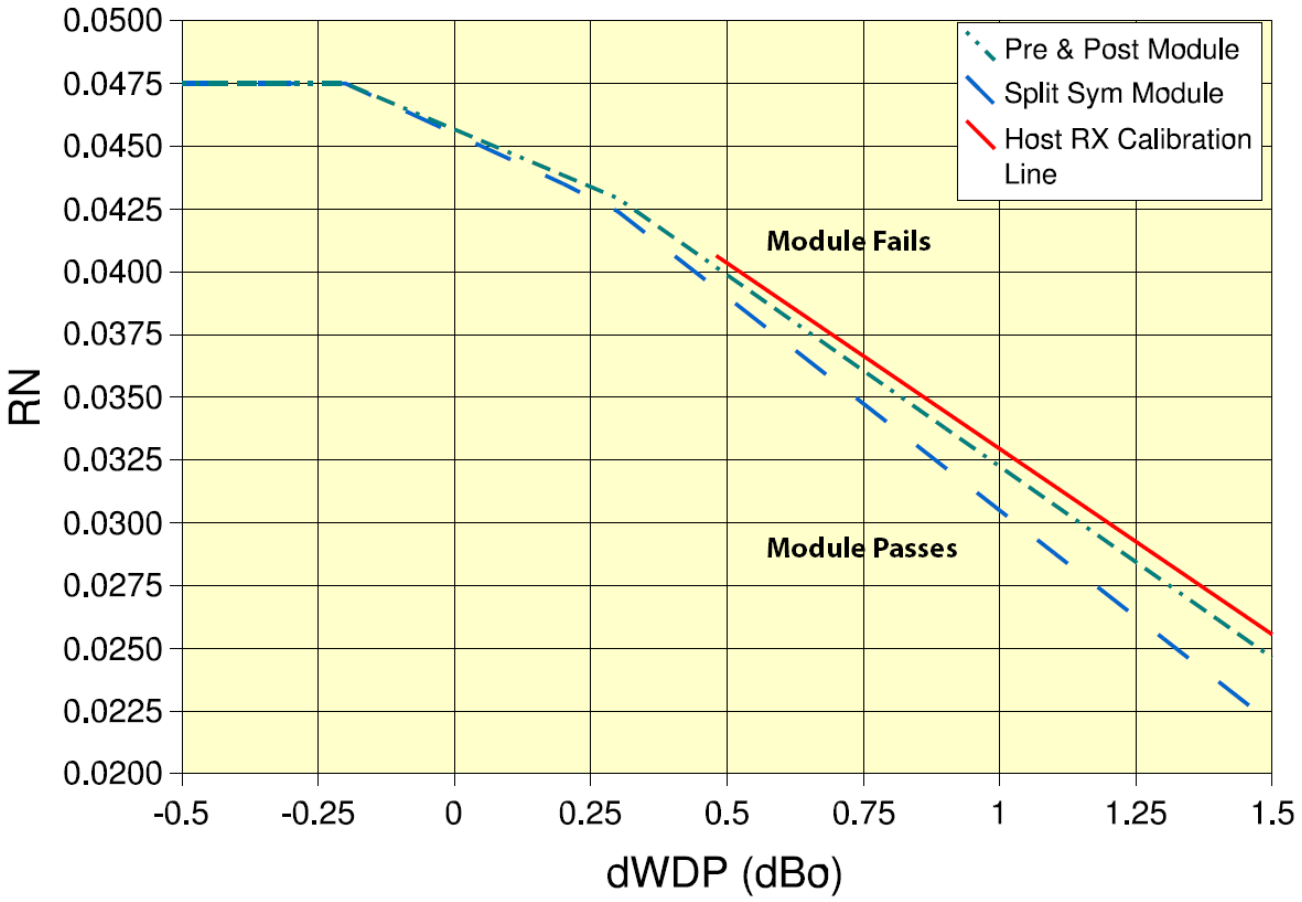


FIGURE 13 LRM MODULE RECEIVER RN AND DWDP COMPLIANCE AND HOST RECEIVER TEST CALIBRATION

For illustrative purposes, Figure 13 shows the host test calibration line along which specific host test points for LRM are defined. The gap between the host and module lines is because the host is tested with linear impairments, which given the same dWDP, are more benign to a host than non-linear impairments which are possible from a module.

A. SFI Channel Recommendation (Informative)

A.1 SFI Host Channel General Recommendations

The purpose of the recommended SFI channel is to provide guidelines for host designers. The recommended SFI host channel consists of PCB traces, vias, and the 20-position enhanced connector defined by SFF-8071. The PCB traces are recommended to meet 100 +/- 10 Ohms differential impedance with nominal 7% differential coupling.

SFI channel S-parameters are defined from ASIC transmitter pads to Host Compliance Board output at B and from Host Compliance Board input at C to ASIC input pads.

See SFF INF-8077i for differential S-parameters measurements and conversions.

A.2 SFI Channel Transfer Recommendations

The SFI maximum channel transfer budget is 9.0 dB allocated as shown in Table 15.

TABLE 15 SFI HOST INTERCONNECT BUDGET

Parameter	Symbol	Conditions	Min	Max	Units
Channel Transfer Including Connector measured with Host Compliance Board (see Appendix C)	SDD21	at 5.5 GHz *1	-6.5	-2.25	dB
Penalty for reflections and other impairments			-2.5		dB
Total Channel Link Budget When Measured with HCB			-9.0	-2.25	dB
*1 SFI channel response (SDD21) is defined from chip pads to compliance point B or C.					

To mitigate multiple reflections, SFI also recommends a minimum channel attenuation. This requirement for both a minimum and maximum channel attenuation results in a mask that is shown approximately by Figure 14. The response including ripple should be within the channel response mask.

The SFI recommended channel is measured with the ASIC removed and measured with the Host Compliance Board of section C.2 . The S-parameters are measured by connecting a 4-port network analyzer to the ASIC pads and the SMA connectors on the Host Compliance Board.

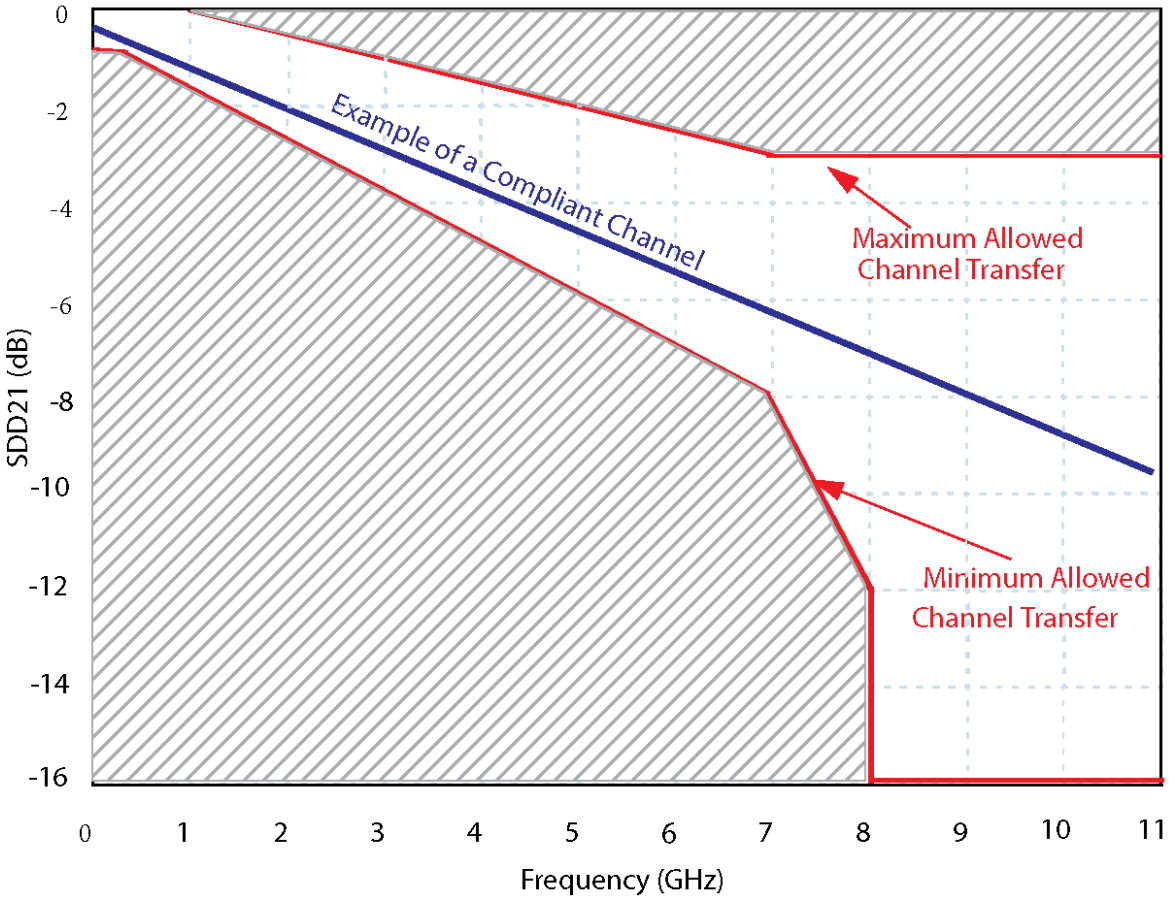


FIGURE 14 EXAMPLE OF SFI HOST RECOMMENDED CHANNEL

The minimum channel transfer SDD21 (maximum loss) mask contour is given by:

$$SDD21(dB) = -0.73$$ f from 0.01 GHz to 0.25 GHz

$$SDD21(dB) = (-0.108 - 0.845 \times \sqrt{f} - 0.802 \times f)$$ f from 0.25 GHz to 7 GHz

$$SDD21(dB) = 20 - 4 \times f$$ f from 7 GHz to 8 GHz

$$SDD21(dB) \geq -16$$ f from 8 GHz to 11.1 GHz

The SFI channel maximum transfer is given by:

$$SDD21(dB) = 0$$ f from 0.25 GHz to 1.0 GHz

$$SDD21(dB) = 0.5 \times (1 - f)$$ f from 1 GHz to 7 GHz

$$SDD21(dB) = -3$$ f from 7 GHz to 11.1 GHz

where f is the frequency in GHz.

A.3 SFI Channel Return Loss Recommendations

The reflection coefficients, SDD11 and SDD22, of the SFI channel are recommended to meet the following equations:

$$SDDxx(dB) \le -14.5 \qquad \text{f from 0.01 to 5 GHz}$$

$$SDDxx(dB) \le -23.25 + 8.75 \times \left(\frac{f}{5}\right) \qquad \text{f from 5 to 11.1 GHz}$$

where f is the frequency in GHz and SDDxx is either SDD11 or SDD22.

A.4 SFI Channel Ripple Recommendations

SFI channel ripple is defined as the difference between the measured insertion response (SDD21m) and the fitted transfer response (SDD21f), all in dB magnitude:

$$Ripple(dB) = SDD21_m - SDD21_f$$

The channel ripple magnitude should conform to the equation:

$$|Ripple(dB)| \le 0.15 + 0.1 \times f$$

where the variable f (frequency) is in GHz. The above equation must be satisfied over the frequency range of 0.25 GHz to 5.5 GHz.

SDD21m is the measured channel differential transfer response. SDD21f is the fitted channel differential transfer response and is given by

$$SDD21_f = [-a - b \times \sqrt{f} - c \times f]$$

Where a, b, and c are determined by the least squares fit over the frequency range of 250 MHz to 5.5 GHz as defined below. Frequency steps should be of equal size and not greater than 50 MHz.

Measured data will provide a frequency vector, f, and gain vector, G defined by

$$G = 20 \times log_{10}[|SDD21|]$$

Create an input vector array called X from frequency variable f

$$X = \begin{bmatrix} 1 & \sqrt{f0} & f0 \\ 1 & \sqrt{f1} & f1 \\ . & . & . \\ 1 & \sqrt{fn} & fn \end{bmatrix}$$

Next calculate the coefficient vector using matrix math

$$C = [X^T \times X]^{-1} X^T \times G$$

Where the calculated coefficient values are given by

a = -C(1)
b = -C(2)
c = -C(3)

B. SFI ASIC/SerDes Specification (Informative)

B.1 Introduction

SFI ASIC/SerDes specifications are informative.

- SFI ASIC/SerDes Transmitter specifications at reference point A are given in B.2
- SFI ASIC/SerDes Receiver specifications at reference point D are given in B.3

ASIC/SerDes meeting the specifications in this appendix when used with the recommended channel of Appendix A are expected to meet the host specifications at B 3.5.1 and C 3.5.2, however any implementation that meets those host specifications is a compliant SFP+ implementation, independent of whether the ASIC/SerDes and/or channel meet the specifications in Appendix A and this appendix. This allows flexibility between channel and SerDes performances and costs.

B.2 SFI ASIC/SerDes Transmitter Output Specifications At A (Informative)

The driver is based on low voltage high speed driver logic with a nominal differential impedance of 100 Ohms. The SFI transmitter electrical specifications at reference point A are given in Table 16 . The source must provide both differential and common mode termination for quality signal termination and low EMI.

Pre-compensation such as de-emphasis may be required to mitigate data dependent jitter at compliance point B.

All parameters at A are measured with the ASIC/SerDes Test Board as shown in C.1.3.

Jitter specifications at A are not provided, the host transmitter in conjunction with the host SFP+ channel must deliver jitter specifications as given by reference point B, Table 6.

B.3 SFI ASIC/SerDes Receiver Input Specifications At D (Informative)

SFI ASIC/SerDes receiver electrical specifications are given in Table 17 and measured at reference point D. All specifications at D are measured with the SerDes on a ASIC/SerDes Test Board C.1.3. The nominal receiver input impedance is 100 Ohms differential. The load must provide differential termination and avoid significant differential to common mode conversion for high quality signal termination and low EMI.

The necessary jitter performance at D is to be determined by the implementer based on the specifications at C.

TABLE 16 ASIC/SERDES TRANSMITTER OUTPUT ELECTRICAL SPECIFICATIONS AT A

Parameter - A	Symbol	Conditions	Min	Typ	Max	Units
Differential Output Voltage	Vdiff				*1	mV (p-p)
Termination Mismatch at 1 MHz	ZM	See D.16			5	%
Single Ended Output Voltage Range			-0.3		4.0	V
Output Rise and Fall time (20-80%)	Tr Tf	See D.6	24			ps
Output AC Common Mode Voltage		See D.15			12	mV (RMS)
Differential Output S-parameter *2	SDD22	0.01-2.8 GHz			-12	dB
		2.8-11.1 GHz			*3	dB
Common Mode Output S-parameter *4	SCC22	0.01-4.74 GHz			-9	dB
		4.74-11.1 GHz			*5	dB

*1 Host ASIC output must be set in combination of host channel to meet Y1 and Y2 levels of Table 6.
*2 Reference differential impedance is 100 Ohms
*3 Differential Output S-parameter is given by equation SDD22(dB)= -8.15 + 13.33 log10(f/5.5), with f in GHz.
*4 Reference common mode impedance is 25 Ohms
*5 Common mode output S-parameter is given by equation SCC22(dB)= -8.15 + 13.33 log10(f/5.5), with f in GHz.

TABLE 17 ASIC/SERDES RECEIVER ELECTRICAL INPUT SPECIFICATIONS AT D

Parameter - D	Symbol	Conditions	Min	Typ	Max	Units
Differential Input Voltage Swing Supporting Limiting Module	Vdiff	*1			850	mV (p-p)
Differential Input Voltage Modulation Amplitude Supporting Linear Module	VMA	*1 *5 see D.7			600	mV
AC Common Mode Voltage Tolerance		see D.15.3	15			mV (RMS)
Differential Input S-parameter *2	SDD11	0.01-2.8 GHz			-12	dB
		2.8-11.1 GHz			*3	dB
Differential to Common Mode Input Conversion S-parameter *4	SCD11	0.01-11.1 GHz			-15	dB

*1 Maximum value represents maximum input level to be tolerated by receiver.
*2 Reference differential impedance is 100 Ohms.
*3 Response is given by equation SDD11(dB)= -8.15 + 13.33 log10(f/5.5), with f in GHz.
*4 The test set common mode reference impedance is 25 Ohms.
*5 Peak levels may exceed VMA due to overshoot of the far end transmitter.

C. Application Reference Boards (Normative)

In order to provide test results that are reproducible and easily measured, this document defines 3 test boards that have SMA interfaces for easy connection to test equipment. One reference board is designed for testing the ASIC/SerDes, one reference board (HCB) for testing the host, and another ref-erence board (MCB) for testing the module. All host, module and ASIC/SerDes specifications and recommendations in this document, and the specifications for the mated pair of compliance boards, are defined at the SMA interfaces. This appendix describes these test cards in detail. The reference test boards' objectives are:

- Satisfy the need for interoperability at the electrical level.
- Allow for independent validation of ASIC/SerDes, host, and module.
- The PCB traces are targeted at 100 Ohms differential impedance with nominal 7% differential coupling.

Testing compliance to specifications in a high-speed system is delicate and requires thorough consideration. Using common test boards that allow predictable, repeatable and consistent results among vendors will help to ensure consistency and true compliance in the testing.

C.1 Compliance Boards

The Host Compliance Board, the Module Compliance Board, and the ASIC test board are made with defined losses of PCB trace with specific high performance properties. Compliance boards are intended to ease building practical test boards with non-zero loss. SFI specifications incorporate the effect of non-zero loss reference test boards which improve the return loss and slightly slows down edges.

Measurements made using non-compliant test boards are invalid and no valid conclusions can be drawn from the results.

C.1.1 Host Compliance Board Transfer Characteristics

SDD21 is defined from the SFF-8071 mating pads, excluding these mating pads, to the mating interface of the SMA connector. The Host Compliance Board is a passive test board and SDD21 and SDD12 should be identical. The recommended response of the Host Compliance Board PCB excluding the SFF-8071 connector is given by.

$$SDD21(dB) = (-0.01 - 0.25 \times \sqrt{f} - 0.0916 \times f) \quad \text{from 0.01 to 15 GHz}$$

where f is the frequency in GHz. From 10 MHz to 11.1 GHz the discrepancy between the measured transfer response and the specified SDD21(dB) shall be <+/-15% of the transfer response in dB or +/-0.1 dB, whichever is larger. For frequencies >11.1 GHz and up to 15 GHz the discrepancy between measured transfer response and the specified SDD21(dB) shall be less than +/-25% transfer response in dB.

The channel transfer characteristic is shown approximately in Figure 15.

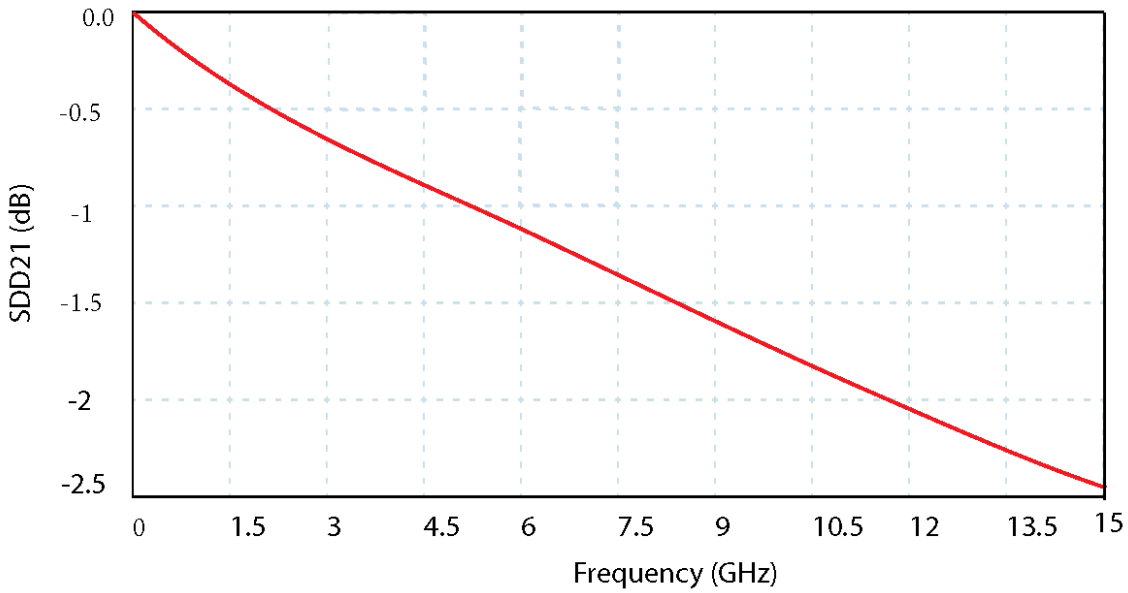


FIGURE 15 APPROXIMATE RESPONSE OF HOST COMPLIANCE BOARD

SFF-8071 connector response is defined by SFF-8071.

C.1.2 Module Compliance Board Transfer Characteristics

SDD21 is defined from the SFF-8071 connector, excluding its solder pads, to the mating interface of the SMA connector. The Host Compliance Board is a passive test board and SDD21 and SDD12 should be identical. The recommended response of the Module Compliance Board PCB excluding the SFF-8071 connector is given by:

$$SDD21(dB) = (-0.00045 - 0.1135 \times \sqrt{f} - 0.04161 \times f) \quad \text{from 0.01 to 15 GHz}$$

where f is the frequency in GHz. Over the range of frequencies specified (10 MHz to 11.1 GHz) any discrepancy between measured transfer response and the specified SDD21(dB) shall be <+/- 15% of the transfer response in dB or +/-0.1 dB, whichever is larger. For frequencies >11.1 GHz and up to 15 GHz the discrepancy between measured transfer response and the specified SDD21(dB) shall be <+/-25% of the transfer response in dB.

The channel transfer response is shown approximately in Figure 16.

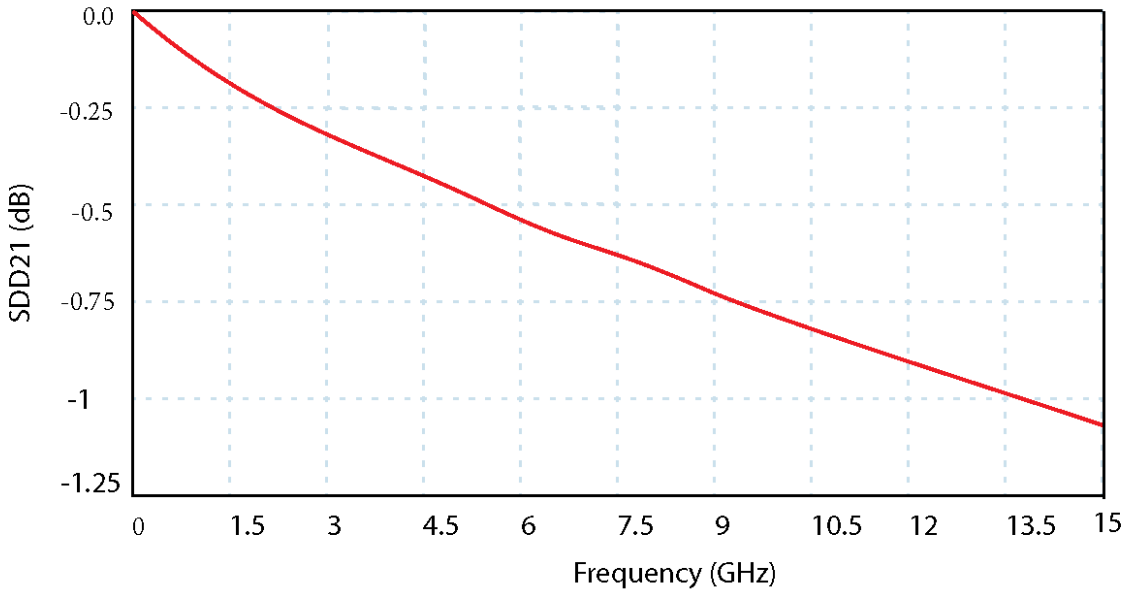


FIGURE 16 APPROXIMATE TRANSFER RESPONSE OF MODULE COMPLIANCE BOARD

SFP+ connector response is defined by SFF-8083.

C.1.3 ASIC/SerDes Test Board Transfer Characteristics

The recommended response of the ASIC/SerDes test board PCB is the same as for the Module Compliance Board (see C.1.2).

C.2 Host Compliance Board

The Host Compliance Board allows predictable, repeatable and consistent results among Host vendors and will help to ensure consistency and true compliance in the testing of Hosts. Host Compliance Boards are provided by Spirent Communication.

C.2.1 Host Compliance Board Material And Layer Stack-Up

Host Compliance Board stack-up shown in Figure 17 is on six metal layers Rogers RO4350B/FR4-6 material. The board is compliant with requirements of SFF-8432 and SFF-8071. SFI signals are routed on signal layer 1, low speed signals and controls are routed on signal layer 6.

1. Top Layer	Signal	17 µ m/0.5 oz Copper plated to 1 oz min+ 1.25 µ m Nickel + 2.5 µ m Gold
0.168 mm / 6.6 mils Rogers RO4350B		
2. Layer	Vee	34 µ m/1 oz Copper
0.14 mm / 5.5 mils FR4-6		
3. Layer	Signal 1	17 µ m/0.5 oz Copper
0.178 mm / 7 mils FR4-6		
4. Layer	Signal 2	17 µ m /0.5 oz Copper
0.14 mm / 5.5 mils FR4-6		
5. Layer	Power	34 µ m/1 oz Copper
0.168 mm / 6.6 mils Rogers RO4350B		
6. Bottom Layer	Signal	17 µ m/0.5 oz Copper plated to 1 oz min + 1.25 µ m Nickel + 0.25 µ m Gold

FIGURE 17 HOST COMPLIANCE BOARD STACK-UP

C.2.2 Host Compliance Board Partlist

The Host Compliance Board part list is given below.

TABLE 18 HOST COMPLIANCE BOARD PART LIST

Qty	RefDes	Value	Description	Example Part Number
2	C5, C6	0.1 uF	Ceramic Capacitor	10% X7R 10V 0402 SMT LFR
3	D1, D2, D3	GREEN	LED Single Green	120 DEG 0603 SMT LFR
2	D4, D5	BLUE	LED Single Blue	120 DEG 0603 SMT LFR
1	J1	Conn3	Connector Header 3 Pins Straight	Tyco PN#3-644695-3
4	J2, J3, J4, J5	EDGE SMA	SMA Connector Jack R/A	Rosenberger PN# 32K243-40ME3
1	J6	CONN1X3P	Connector Header 3 Pins 100 mil Pitch	Molex PN# 22-23-203
5	R1, R2, R3, R4, R5	1.0 kOhms	Resistor	RES 1.00K 1% 1/10W 0603 SMT LFR
1	SW1	SPST	SW 4 Position Dip Switch SMT	ITT Cannon PN# TDA04H0SB1

Note: Table 18 does not use all in-sequence part numbers.

C.2.3 HCB Gerber Files

The Gerber file for the Host Compliance Board is available in SFF-8434.

C.2.4 Schematic of Host Compliance Board

The schematic of Host Compliance Board is shown in Figure 18.

Mod-DEF0 in the schematic is Mod_ABS as defined by SFF-8419 SFP+ Module and Host Electrical Contact Definition and AS0/AS1 in the schematic are RS0/RS1 as defined by SFF-8419 SFP+ Module and Host Electrical Contact Definition.

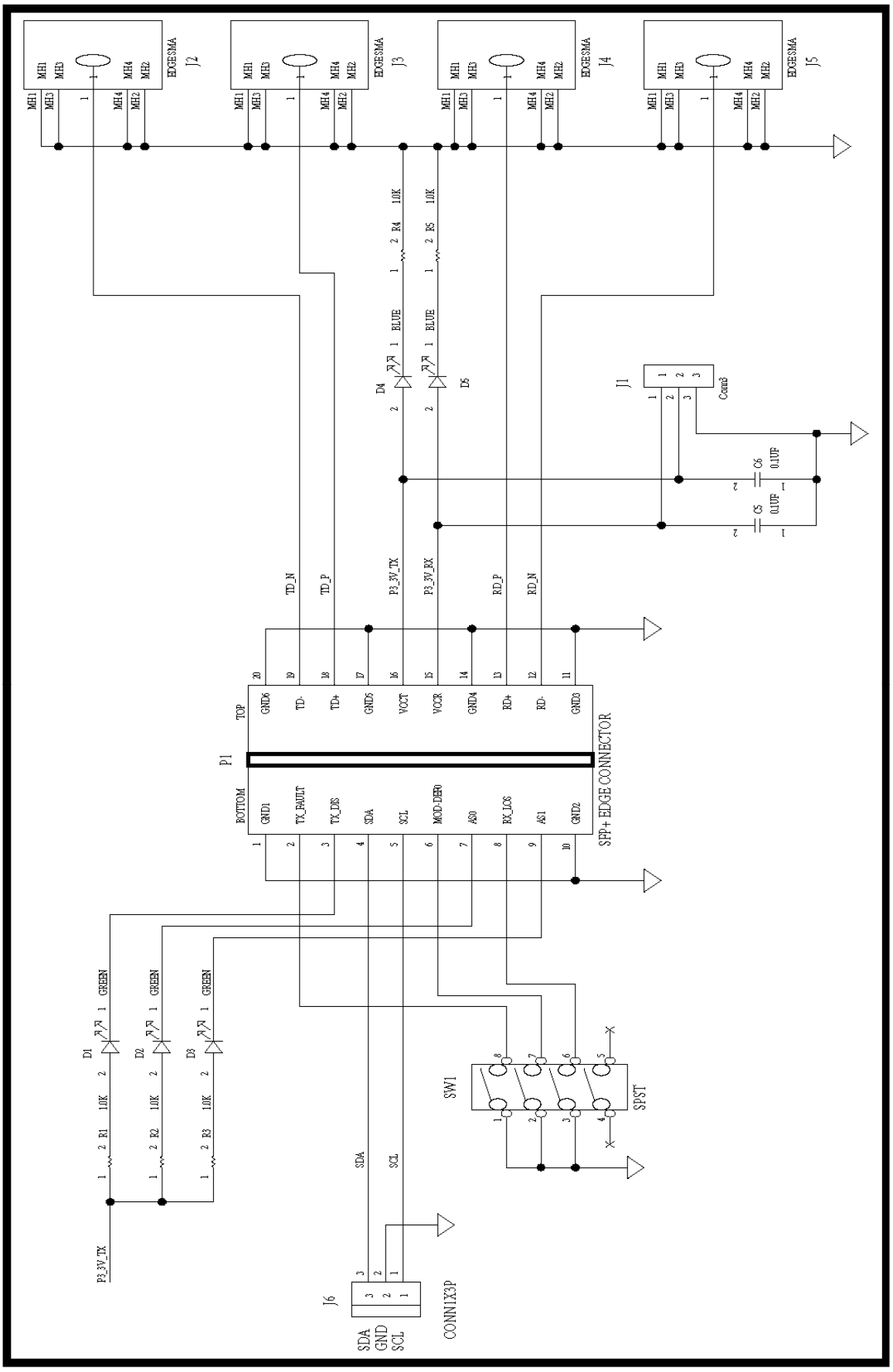


FIGURE 18 SCHEMATIC OF THE HOST COMPLIANCE BOARD

C.3 Module Compliance Board

The Module Compliance Board allows predictable, repeatable and consistent results among module vendors and will help to ensure consistency and true compliance in the testing of modules. Module Compliance Boards are provided by Broadcom Corporation.

The solder pads for the high speed traces in the Module Compliance Board are 1.1x0.4 mm to improve high frequency performance instead of 2.0x0.5 mm as defined in the SFF-8071 for improved manufacturability. For detailed geometry, see the Gerber files in C.3.4.

C.3.1 Module Compliance Board Material And Layer Stack-Up

Module Compliance Board stack-up shown in Figure 19 is based on a laminate of Rogers RO4350B/FR4-6 with ten metal layers. SFI signals are routed on signal layer 1, low speed signals and controls are routed on signal layers 8 and 10.

1. Top Layer	Signal	17 µm/0.5 oz Copper + 1.25 µm Nickel + 2.5 µm Gold
0.168 mm / 6.6 mils Rogers RO4350B		
2. Layer	Vee	17 µm /0.5 oz Copper
0.382 mm / 15 mils FR4-6		
3. Layer	Vee	34 µm/1 oz Copper
0.076 mm / 3 mils FR4-6		
4. Layer	VccR	34 µm/1 oz Copper
0.076 mm / 3 mils FR4-6		
5. Layer	Vee	34 µm /1 oz Copper
0.076 mm / 3 mils FR4-6		
6. Layer	VccT	34 µm /1 oz Copper
0.076 mm / 3 mils FR4-6		
7. Layer	Vee	34 µm/1 oz Copper
0.076 mm / 3 mils FR4-6		
8. Layer	Signal	34 µm/1 oz Copper
0.382 mm / 15 mils FR4-6		
9. Layer	Vee	17 µm /0.5 oz Copper
0.168 mm / 6.6 mils Rogers RO4350B		
10. Bottom Layer	Signal	17 µm/0.5 oz Copper + 1.25 µm Nickel + 2.5 µm Gold

FIGURE 19 MODULE COMPLIANCE BOARD STACK UP

C.3.2 Schematic of Module Compliance Board

Schematic of Module Compliance Board is shown in Figure 20.

Mod-DEF0 in the schematic is Mod_ABS as defined by SFF-8419 SFP+ Module and Host Electrical Contact Definition and AS0/AS1 in the schematic are RS0/RS1 as defined by SFF-8419 SFP+ Module and Host Electrical Contact Definition.

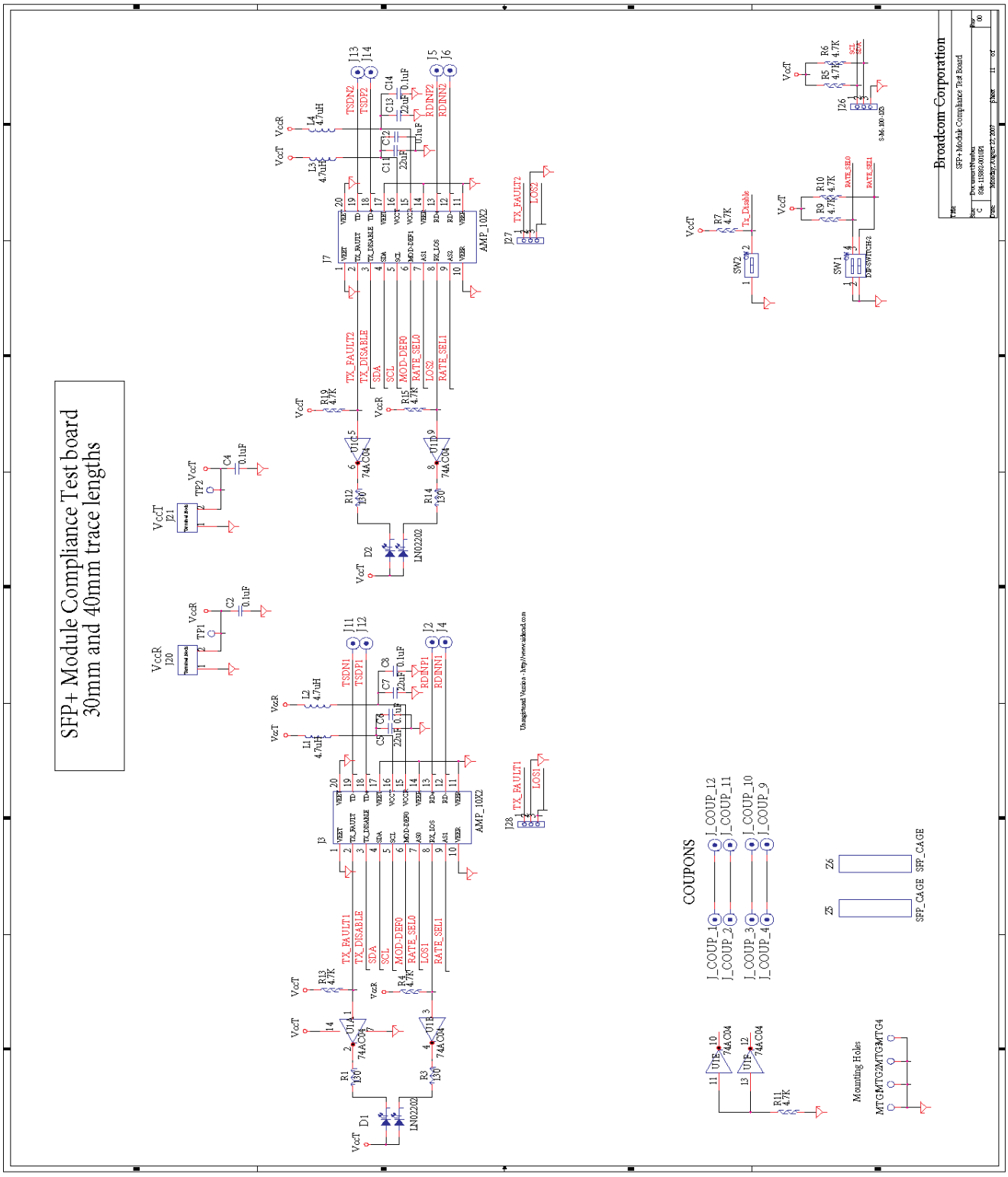


FIGURE 20 SCHEMATIC OF THE MODULE COMPLIANCE BOARD

C.3.3 Module Compliance Board Partlist

Component part list for the Module Compliance Board is given below.

TABLE 19 MODULE COMPLIANCE BOARD PART LIST

Qty	RefDes	Value	Description	Example Part Number
6	C2, C4, C6, C8, C12, C14	0.1uF	Ceramic Capacitors	Murata/GRM188R71C104MA01D
4	C5, C7, C11, C13	22 uF	Ceramic Capacitors	Murata/GRM21BR60J226ME39K
	D1, D2, D4, D5	RED	LED	Panasonic/LNJ208R8ARA
12	J_COUP_2, J2, J_COUP_4, J4, J5,J6, J_COUP_9, J_COUP_11, J12, J14J_COUP_1, J_COUP_3, J_COUP_10, J11, J_COUP_12, J13	SMA	SMA Connector R/A	Huber&Suhner/92_SK-U50-0-3/199_NE
2	J3, J7	Con_10x2	SFF-8071 Connector	Tyco 1888247 or Molex 74441
2	J20, J21	Terminal Block	Terminal Block	On-Shore-Tech/EDZ5002DS
3	J26, J27, J28	S-M-.100-1X3	PCB Header	Molex/22-10-2031
4	L1, L2, L3, L4	4.7 uH	Inductor	Toko/A914BYW-4R7M
4	R1, R3, R12, R14	130 Ohms	Resistors	Walsin/WR06X131JTL
10	R4, R5, R6, R7, R9, R10, R11, R13, R15, R19	4.7 kOhms	Resistors	Walsin/WR06X472JTL
1	SW1	DIP-SWITCH-2	DipSwitch	CT2062-ND
1	SW2	sw_pb_ck-k	Toggle Switch	C&K/ET01MD1AVBE
1	U1	74AC04	Inverter	Fairchild/530438-00
2	Z5, Z6	SFP_CAGE	SFP Cage	Tyco 1489962-1

Note: Table 19 does not use all in-sequence part numbers.

C.3.4 MCB Gerber Files

The Gerber file for the Module Compliance Board is available in SFF-8434.

C.4 Specifications For Mated Host and Module Compliance Boards

Based on measurements of the Module Compliance Board (MCB) mated with the Host Compliance Board (HCB) the following specifications have been derived for the mated pair. Compliance to these limits help ensure the module and host specifications can be met. S-parameters are defined based on two ports mixed mode differential definition [see INF-8077i Appendix C], see Figure 21. All single port measurements are listed on the figure.

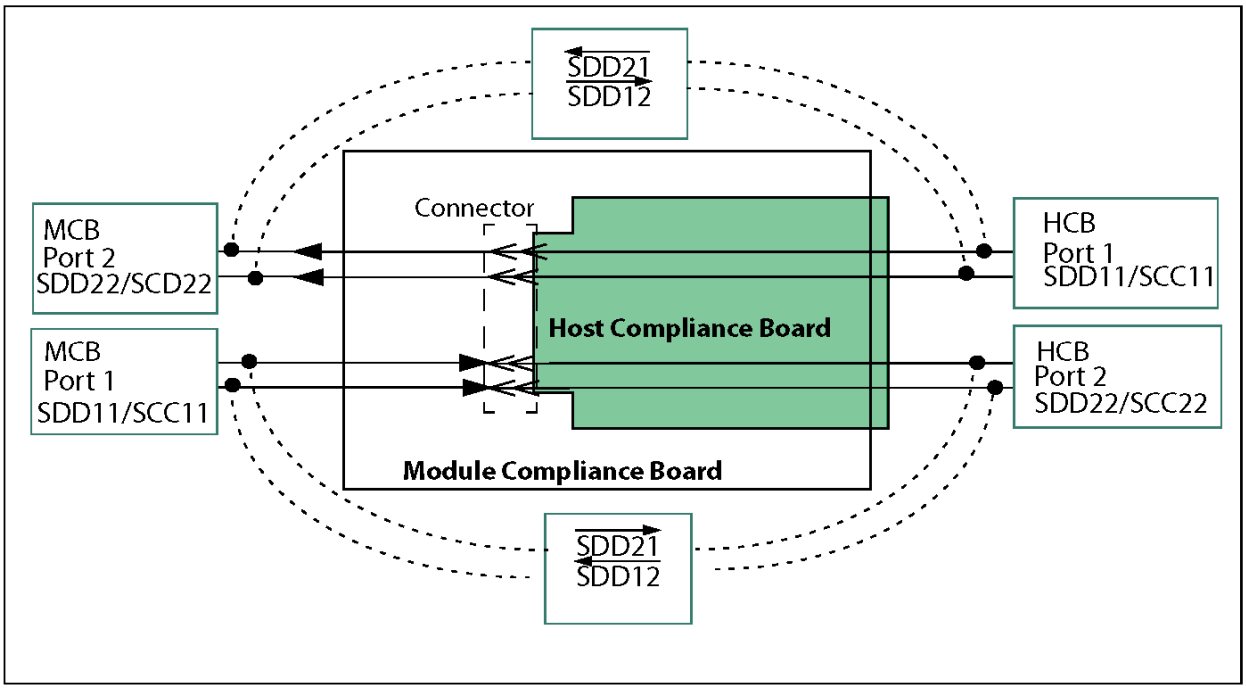


FIGURE 21 MEASUREMENTS PORT DEFINITION

The maximum values of SDD11 or SDD22 looking into the Module Compliance Board and Host Compliance Board are illustrated in Figure 22.

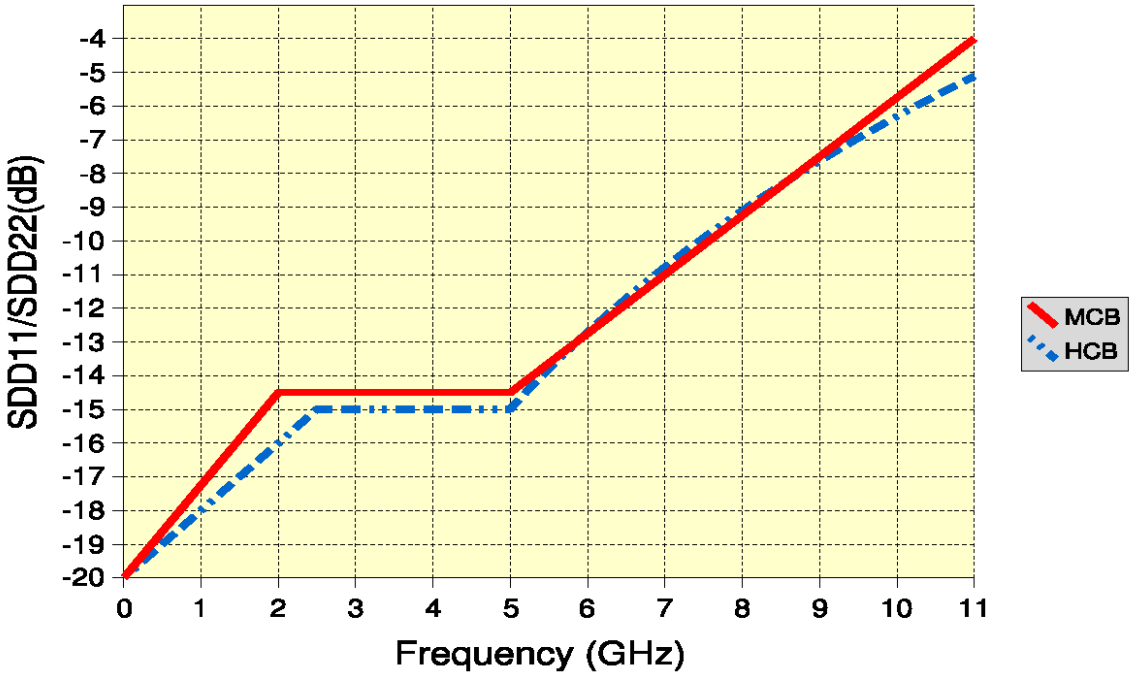


FIGURE 22 MAXIMUM DIFFERENTIAL RESPONSE OF MATED MCB AND HCB

The maximum values of SDD11 or SDD22 looking into the Module Compliance Board are given by the following equations:

$$SDDxx(dB) \le -20 + 2.75 \times f \qquad \text{f in GHz from 0.01 to 2}$$

$$SDDxx(dB) \le -14.5 \qquad \text{f in GHz from 2 to 5}$$

$$SDDxx(dB) \le -23.25 + 8.75 \times \left(\frac{f}{5}\right) \qquad \text{f in GHz from 5 to 11.1}$$

The maximum values of SDD11 or SDD22 looking into the Host Compliance Board are given by the following equations:

$$SDDxx(dB) \le -20 + 2 \times f \qquad \text{f in GHz from 0.01 to 2.5}$$

$$SDDxx(dB) \le -15 \qquad \text{f in GHz from 2.5 to 5}$$

$$SDDxx(dB) \le -13.8 + 28.85 \times \log_{10}\left(\frac{f}{5.5}\right) \qquad \text{f in GHz from 5 to 11.1}$$

The maximum and the minimum values of SDD21 or SDD12 looking into either the module compliance board or host compliance board are illustrated in Figure 23 and given by the equations below.

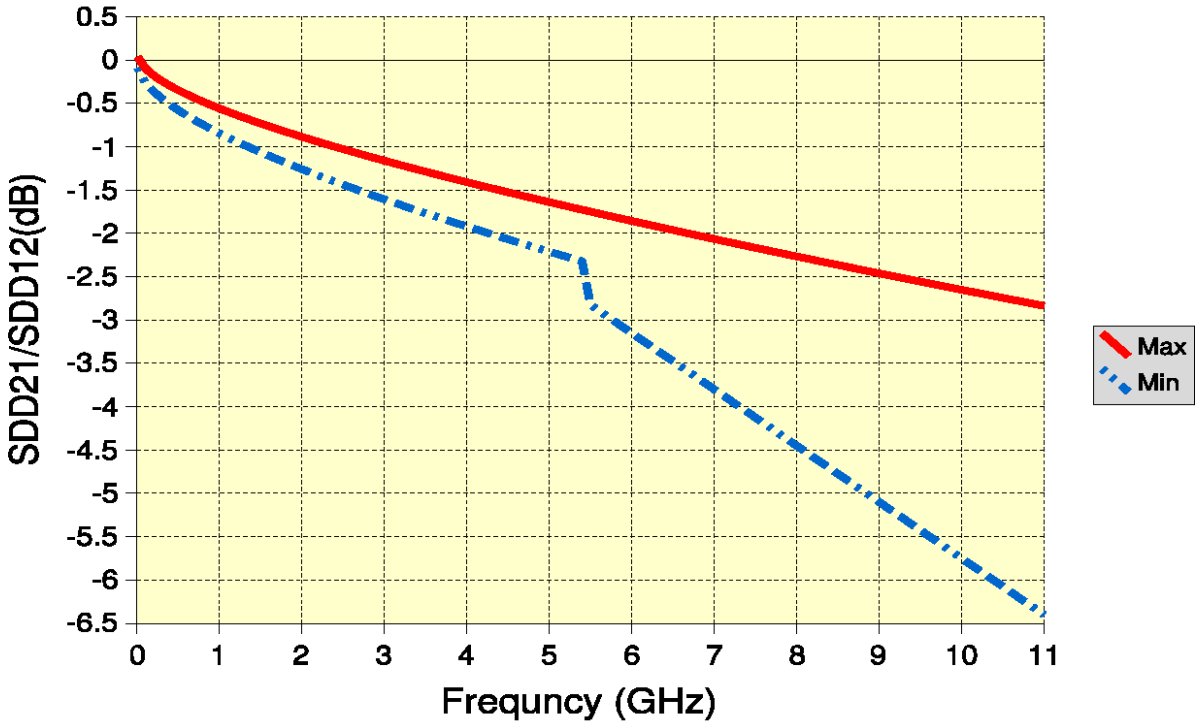


FIGURE 23 MATED MCB-HCB DIFFERENTIAL THROUGH RESPONSE LIMITS

$$SDDxx(dB) \le (-0.012 - 0.694 \times \sqrt{f} - 0.127 \times f) \qquad \text{f in GHz from 0.01 to 5.5}$$

$$SDDxx(dB) \le 0.75 - 0.65 \times f \qquad \text{f in GHz from 5.5 to 11.1}$$

$$SDDxx(dB) \le 0.0915 - 0.549 \times \sqrt{f} - 0.101 \times f \qquad \text{f in GHz from 0.01 to 11.1}$$

The maximum values of SCC11 or SCC22 looking into either the Module Compliance Board or Host Compliance Board are illustrated in Figure 24.

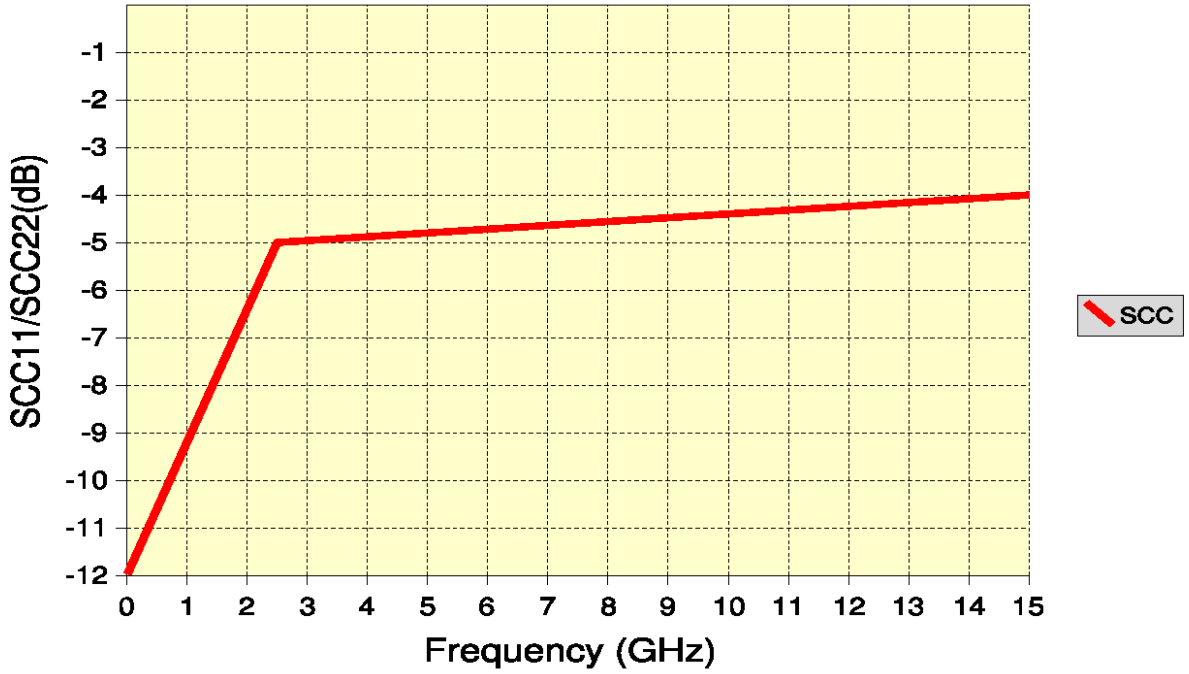


FIGURE 24 MAXIMUM COMMON MODE RESPONSE OF MATED MCB AND HCB

The SCC11 and SCC22 are also given by the following equations:

$$SCCxx(dB) \le -12 + 2.8 \times f \qquad \text{f in GHz from 0.01 to 2.5}$$

$$SCCxx(dB) \le -5.2 + 0.08 \times f \qquad \text{f in GHz from 2.5 to 15.}$$

The maximum values of Differential to Common Mode Response SCD21 and SCD12 looking into either the Module Compliance Board or Host Compliance Board are illustrated in Figure 25.

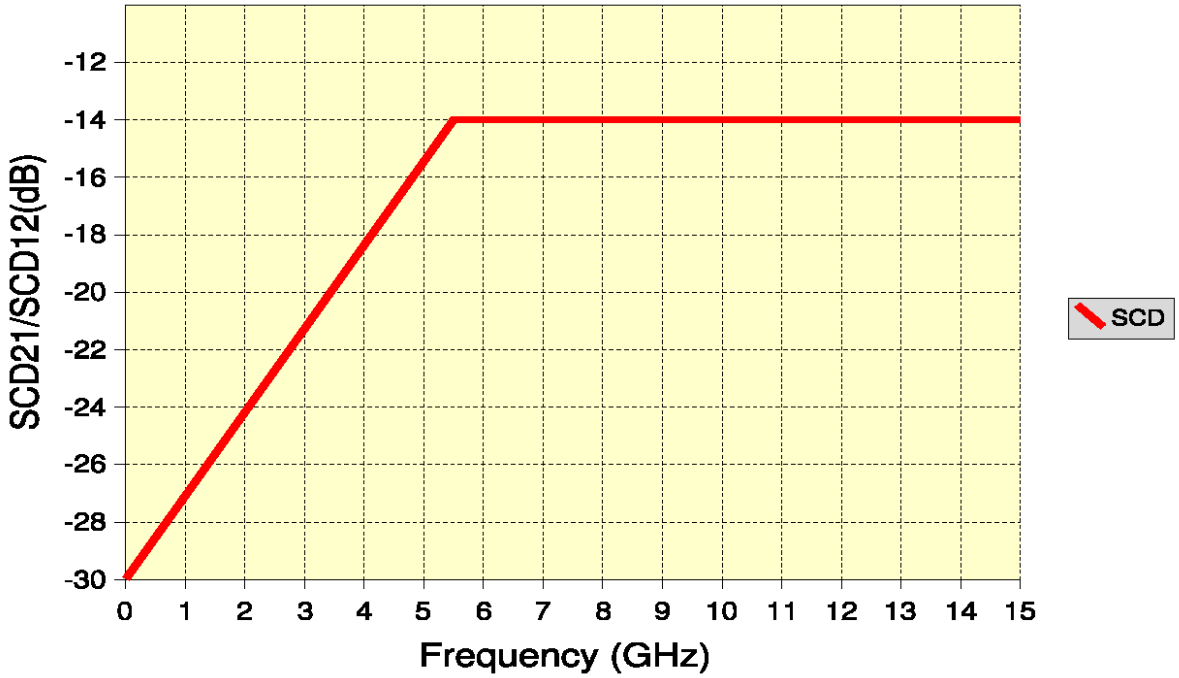


FIGURE 25 MAXIMUM DIFFERENTIAL TO COMMON MODE RESPONSE OF MATED MCB AND HCB

Mated response SCD21 and SCD12 of the mated Module and Host Compliance Board are given by:

$$SCDxx(dB) \leq -30 + 2.91 \times f \qquad \text{f in GHz from 0.01 to 5.5}$$

$$SCDxx(dB) \leq -14 \qquad \text{f in GHz from 5.5 to 15.}$$

When MCB Port 1 of the mated Module Compliance Board and Host Compliance Board is excited by the crosstalk source defined in Table 6, the RMS differential NEXT voltage at MCB Port 2 shall be less than 1 mV when measured in a 12 GHz bandwidth. The differential NEXT voltage from HCB Port 1 to HCB Port 2 is expected to be about the same. Compliance boards meeting this response are expected to pass the integrated NEXT requirement, however it is also expected that the curve can be exceeded due to frequency resonances while still passing the integrated NEXT requirement. The frequency domain curve shown in Figure 26 shows a recommended response which is described in the equations following the figure. Compliance boards meeting this NEXT response are expected to pass the NEXT voltage requirement, however it is also expected that the curve can be exceeded due to frequency resonances while still passing the NEXT voltage requirement.

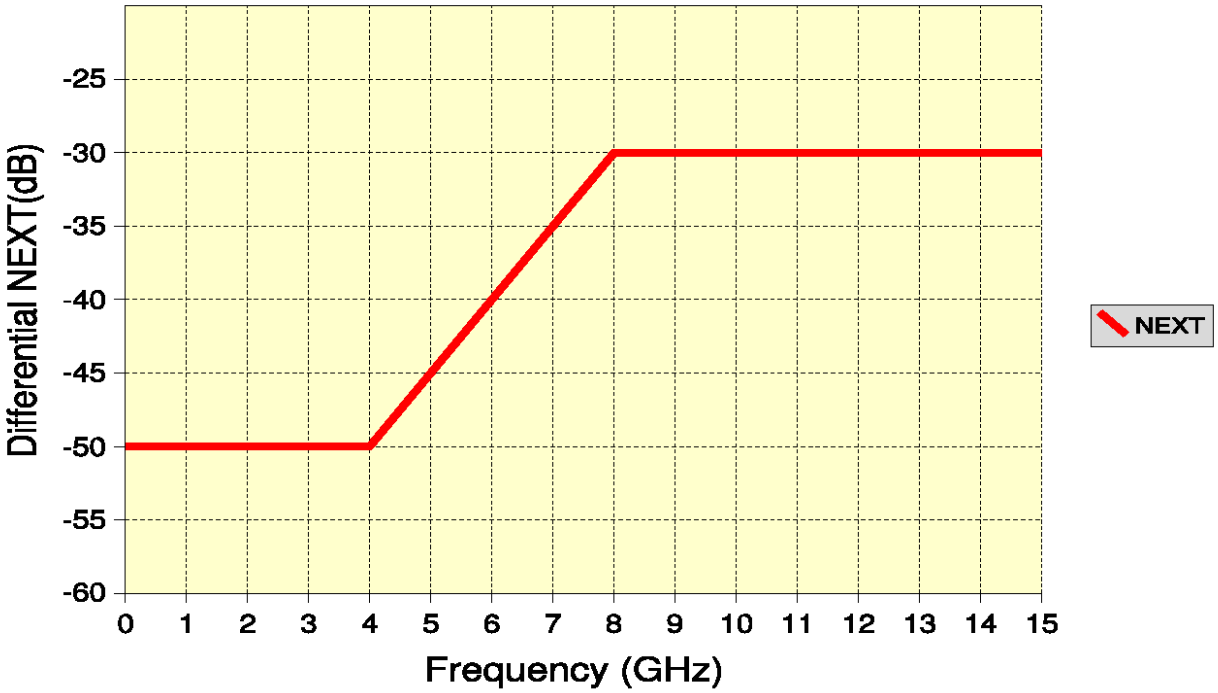


FIGURE 26 MAXIMUM DIFFERENTIAL NEXT RESPONSE OF MATED MCB AND HCB

The recommended NEXT response is also given by the following equations:

The recommended NEXT response is also given by the following equations:

$$NEXT(dB) \leq -50 \qquad \text{f in GHz from 0.01 to 4}$$

$$NEXT(dB) \leq -70 + 5 \times f \qquad \text{f in GHz from 4 to 8}$$

$$NEXT(dB) \leq -30 \qquad \text{f in GHz from 8 to 15.}$$

D. Test Methodology And Measurement (Normative)

D.1 Introduction

This appendix defines metrics for SFP+ high speed and power electrical interfaces and provides practical guidance for test implementation. Each parameter is defined in terms of a measurement procedure. The instruments for measurement are assumed to be ideal: accurate, precise, with infinite or defined bandwidth, zero or defined noise and so on. In practice, the necessary level of instrument performance and the approach to calibration and margining must be considered. Some guidance is given in the following sections.

All measurements are made differentially, with the exception of:
- AC Common Mode Generation Test D.15.2,
- Common Mode Tolerance Test D.15.3,
- Termination Mismatch D.16 ,

Accurate calibration of test equipment is assumed for all measurements. To avoid pessimistic WDP and jitter results, the scope may require correction for time base linearity errors.

D.1.1 Test Patterns

Test patterns used in this specification include the 8+8 square wave, PRBS9, IEEE 802.3 test patterns 1, 2 and 3, and any valid 64B/66B signal.

PRBS9 is defined in IEEE Std 802.3, 68.6.1 and a file for the sequence can be found at http://ieee802.org/3/aq/public/tools/TWDP/prbs9_950.txt. Test patterns 1, 2 and 3 are defined in IEEE Std 802.3, 52.9.1.1. Test pattern 3 is PRBS31 as defined by ITU-T or in IEEE Std 802.3, 49.2.8.

D.2 Eye Mask Compliance

This section defines what is meant by eye mask compliance and gives guidance for its determination. Mask templates and coordinates are given in sub-clauses in 3.5 SFP+ Host System Specifications and 3.6 SFP+ Module Specifications.

- The pattern(s) for eye mask testing is according to the relevant standard(s) listed in Table 1.
- The output being tested should comply over the range of operating conditions while the opposing direction bit stream, operates with the target crosstalk rise and fall and amplitude given in Table 6, Table 8, Table 11, and Table 12. The opposing direction bit stream (than the one being tested) shall be asynchronous PRBS31 or valid 64B/66B bit stream.

Testing may include guard banding, extrapolation, or other methods, but must ensure that mask violations do not occur at a rate exceeding the hit ratio limit given in the appropriate table.

- An AC coupling 3 dB corner frequency of 20 kHz is expected to be adequate to eliminate baseline wander effects, however high frequency performance is critical and must not be sacrificed by the AC coupling.
- All loads are specified at 100 Ohms differential.
- 0.0 UI and 1.0 UI on the time axis are defined by the eye crossing means at the average value (zero volts if AC coupled) of the signal. The average value might not be at the jitter waist.

A clock recovery unit (CRU) is used to trigger the scope for mask measurements as shown in Figure 27. The reference CRU has a high frequency corner bandwidth of 4 MHz and a slope of -20 dB/decade with peaking of 0.1 dB or less.

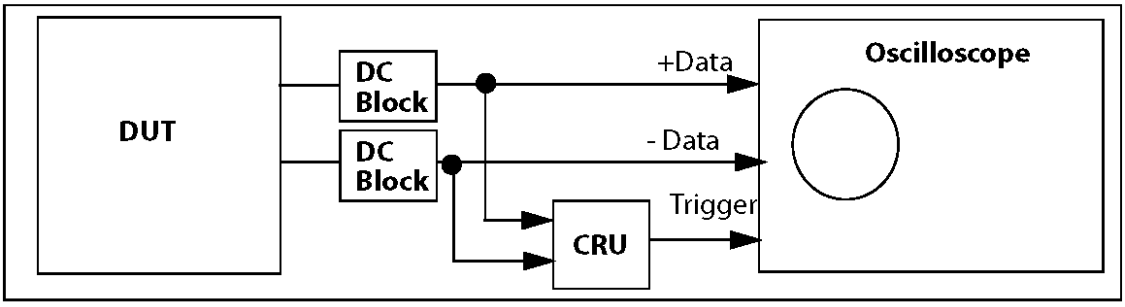


FIGURE 27 EYE MASK MEASUREMENT SETUP - BLOCK DIAGRAM

D.2.1 Example Calculations For 5X10^(-5) Hit Ratio

If an oscilloscope records 1350 samples/screen, and the timebase is set to 0.2 UI per division with 10 divisions across the screen, and the measurement is continued for 200 waveforms, then a transmitter with repeated measurement averaging to less than 6.75 hits is compliant. i.e.,

$$HitRatio = \frac{5 \times 10^{-5} \times 1350}{0.2 \times 10} = 6.75$$

Likewise, if a measurement is continued for 1000 waveforms, then repeated measurement averaging to less than 33.75 hits is compliant. An extended measurement is expected to give a more repeatable result, whereas a single reading of 6 hits in 200 waveforms would not give a statistically significant pass or fail.

D.3 Data Dependent Jitter (DDJ) And Pulse Width Shrinkage (DDPWS)

A high-resolution oscilloscope, time interval analyzer, or other instrument with equivalent capability may be used to measure DDJ and DDPWS. A repeating PRBS9 pseudo-random test pattern, 511 bits long, is used. For electrical jitter measurements, the measurement bandwidth is 12 GHz. If the measurement bandwidth affects the result, it can be corrected for by post-processing. However, a bandwidth above 12 GHz is expected to have little effect on the results.

DCD and Pulse Width Shrinkage (DDPWS) are components of DDJ.

Establish a crossing level equal to the average value of the entire waveform being measured. Synchronize the instrument to the pattern repetition frequency and average the waveforms or the crossing times sufficiently to remove the effects of random jitter and noise in the system. The PRBS9 pattern has 128 positive-going transitions and 128 negative-going transitions. The mean time of each crossing is then compared to the expected time of the crossing, and a set of 256 timing variations is determined. DDJ is the range (max-min) of the timing variations. Keep track of the signs (early/late) of the variations. Note, it may be convenient to align the expected time of one of the crossings with the measured mean crossing.

The following Figure 28 illustrates the method. The vertical axis is in arbitrary units, and the horizontal axis is plotted in UI. The waveform is AC coupled to an average value of 0, therefore 0 is the appropriate crossing level. The rectangular waveform shows the ideal crossing times, and the other is the waveform with jitter that is being measured. Only 32 UI are shown (out of 511). The waveforms have been arbitrarily aligned with (Delta t2 = 0) at 14 UI.

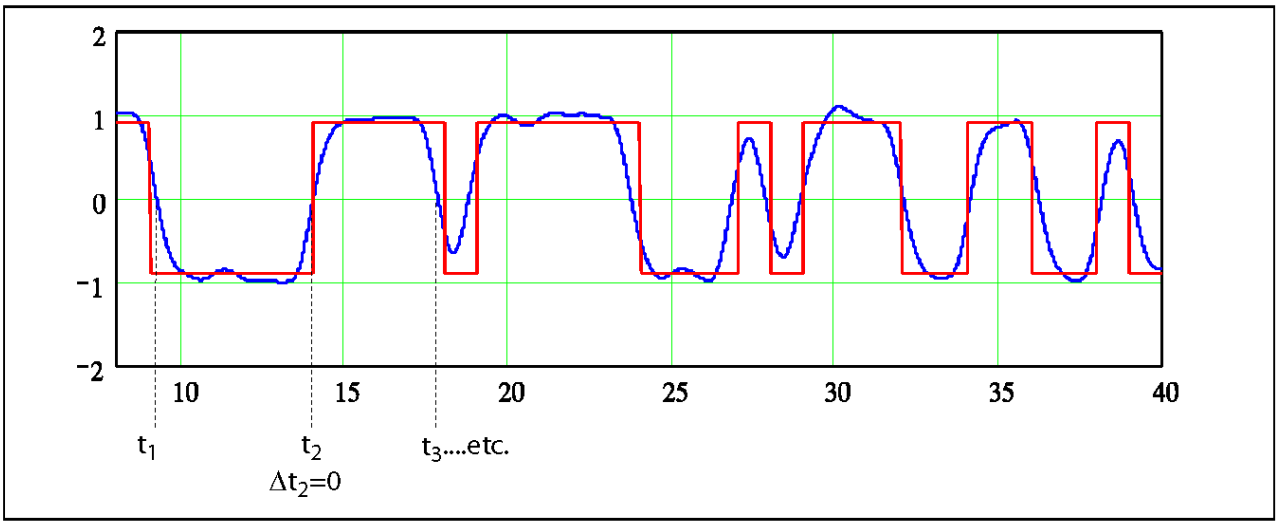


FIGURE 28 DDJ TEST METHOD

DDJ is defined as

$$DDJ = max(\Delta t_1, \Delta t_2, \ldots \Delta t_n) - min(\Delta t_1, \Delta t_2, \ldots \Delta t_n)$$

Every edge, 1...n, in a complete repetition of the pattern is measured (n = 256 in a PRBS9 pattern).

DDPWS is determined as the difference between one symbol period and the minimum of all the differences between pairs of adjacent edges:

DDPWS = T - min(t2-t1, t3-t2,..... tn+1-tn)

where T is one symbol period. Note that the difference from the next edge in the repeating sequence, tn+1, is also considered.

D.3.1 Duty Cycle Distortion (DCD)

DCD represents a deviation from the intended duty cycle. It is the difference between the mean position of all falling edges and the mean position of all rising edges with uncorrelated effects minimized through averaging. DCD is measured at the average value of the waveform.

D.4 Uncorrelated Jitter (UJ)

UJ as defined by IEEE 802.3 CL 68 is a measure of any jitter that is uncorrelated to the 64B/66B bit stream. The definition and test procedure for UJ are identical to those defined in IEEE 802.3 CL 68.6.8 with following considerations:

- The host transmitter shall comply while the host receiver is operating with asynchronous PRBS31 or valid 64B/66B signal and all other ports operating as in normal operation, including proper termination.
- The receive path input of the Host Compliance Board is connected to a pattern generator and calibrated through a Module Compliance Board. The amplitude and rise time are set to the target values stated in Table 6 at C''.
- For the purposes of this document the procedures defined for optical testing also apply to electrical testing. Optical terms (such as power) and units, such as in Figure 68-9 in IEEE 802.3, can be converted to corresponding electrical terms (such as voltage) and units, etc.
- The 4th-order Bessel-Thomson response is to be used only for optical measurements of UJ. UJ in the electrical domain is defined in a bandwidth of 12 GHz, unless specified by the application standard.
- PRBS9 is suitable as a test sequence for all applications unless specified otherwise.
- The bandwidth of the CRU is defined in IEEE 802.3 clause 68.6.8 or in the relevant standard for the application.

D.5 99% Jitter (J2) and Total Jitter (TJ)

Jitter is a property of the timing of a signal's edges. The time of occurrence of an edge is defined as when the signal crosses its average level (e.g., 0 V for A.C. coupled, ground terminated measurements). Jitter is defined using the CRU of section D.2 . The test pattern for Total Jitter (TJ) and 99% Jitter (J2) testing shall be either PRBS31 or a valid 64B/66B signal. These metrics of jitter are measured without averaging.

J2 is the same as J, "all but 1% for jitter", used in IEEE 802.3 Clause 52.9.9. It is defined as the time interval that includes all but 10^(-2) of the jitter distribution. If measured using an oscilloscope, it is the time interval from the 0.5th to the 99.5th percentile of the jitter distribution measured on the histogram.

TJ, as used in this document, is the Level 1 definition for TJ as described in the FC-MJSQ, where TJ is the crossing width, defined as the late time at which the

BER is 10^(-12) minus the early time at which the BER is 10^(-12). This is one unit interval (UI), minus the "jitter eye opening" defined in FC-MJSQ. TJ can be expressed as:

$$TJ=T-t1$$

Where t1 is the jitter eye opening at the CDF = 10-12, and T is one symbol period.

The CDF is a cumulative distribution function of the timings of the edges with a maximum close to 0.5 because the transition density is close to 50%.

A measurement using the BERT bathtub method must be corrected for the instrument's setup-and-hold time and noise. As PRBS31 is more demanding than a 64B/66B signal, a 10GBASE-R instance whose TJ is compliant using a 64B/66B signal is considered compliant even if it does not meet the required limit using PRBS31. A 10GBASE-W instance shall be compliant with PRBS31. It is not expected that the J2 value will differ between these patterns.

Both J2 and TJ are measured from side to side of the CDF, not from median to side of the CDF.

D.6 Rise And Fall Times

In this document, rise and fall times are defined as the time between the 20% and 80% times, or 80% and 20% times, respectively, of isolated edges. The normative test pattern is the OMA test pattern (eight ones, eight zeros). The 0% level and the 100% level are as defined by the xMA measurement procedure (see D.7 and IEEE Std 802.3, 68.6.2).

Alternatively, suitable edges exist in the PRBS9, within sequences of five zeros and four ones, and nine ones and five zeros, respectively. These are bits 10 to 18 and 1 to 14, respectively. In this case, the 0% level and the 100% level may be estimated as ZeroLevel and ZeroLevel + MeasuredxMA in the xWDP code (see Appendix G), or by the average signal within windows from -3 to -2 UI and from 2 to 3 UI relative to the edge. The PRBS9 methods are inaccurate for rise and fall times above 1.5 UI.

For electrical signals, the waveform is observed through a 12 GHz low pass filter response. For optical signals, the rise and fall times may be defined either without a filter response or through the standard 7.5 GHz Bessel-Thomson response; one or the other option is specified in each case.

NOTE: The rise and fall definition in this document is not the same as the rise and fall times typically reported by an oscilloscope from an eye diagram derived from a mixed frequency signal such as PRBS or a 64B/66B signal, which takes all the edges into account.

D.7 Voltage Modulation Amplitude (VMA)

VMA is the difference between the nominal one and zero levels of an electrical signal. It is analogous to the OMA of an optical signal (see IEEE Std 802.3 52.9.5 and 68.6.2). VMA is defined with the square wave test pattern of eight ones and eight zeros defined in IEEE Std 802.3, 68.6.1 (this is a subset of the square waves allowed in IEEE 802.3, 52.9.5), or in the case of a non-802.3 application, a test pattern defined by the relevant standard.

It can be measured as follows:

- The signal under test is set to carry the square wave pattern and is observed, typically with an oscilloscope triggered to the pattern. The bandwidth of this measurement system is at least 3/T, where T is the period between transitions. For the square wave test pattern (0000000011111111) this gives approximately 4 GHz at 10.3125 GBd; the 12 GHz bandwidth defined for other electrical quantities is convenient. Electrical measurements of VMA do not require a 7.5 GHz Bessel-Thomson filter.
- The square wave being measured is divided into two equal time intervals, 8 UI long, aligned to the average time of both edges.
- The time of occurrence of an edge is defined as when the square-wave signal crosses its average level (0 V for A.C. coupled measurements).
- The average voltage level in the central 20% of each time interval is measured.
- The difference between the two levels (a positive voltage) is the VMA.
- An estimate of the OMA or VMA of a PRBS9 waveform is provided by the variable MeasuredxMA calculated by the algorithm in Appendix G.

An example square wave signal with eight zeros and eight ones with the two measurement windows is shown in Figure 29.

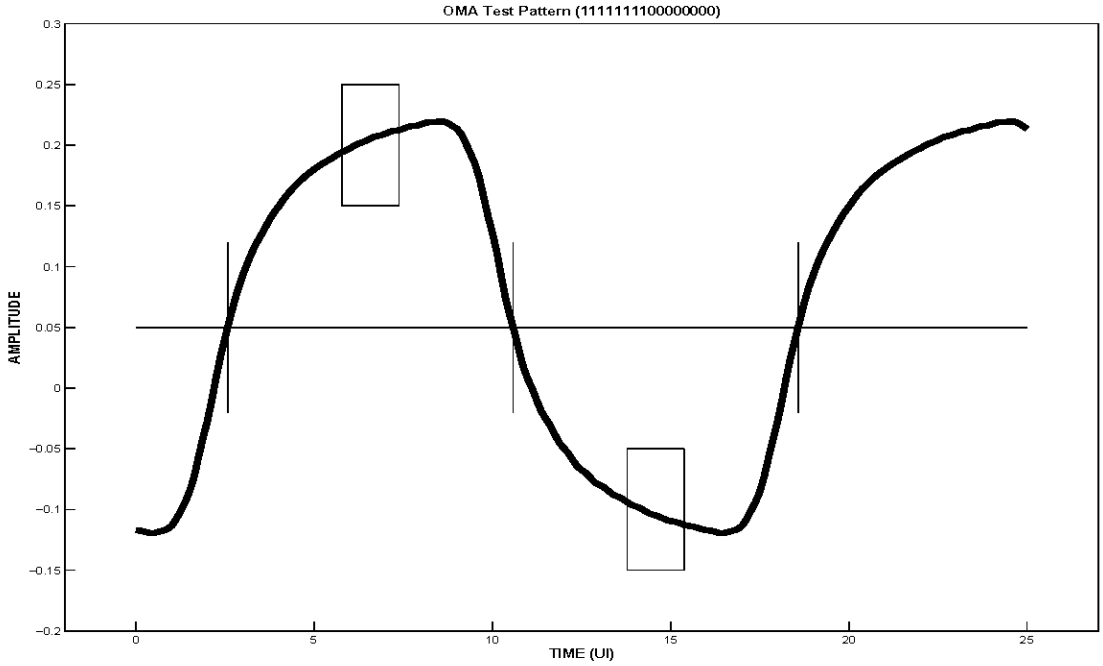


FIGURE 29 EXAMPLE XMA WAVEFORM SHOWING XMA MEASUREMENT WINDOWS

D.8 Relative Noise (RN)

RN is a measure of reciprocal SNR for a signal. RN is given by:

$$RN = \frac{2 \times noise(RMS)}{(xMA)}$$

where for this document, xMA is OMA if an optical signal is being measured, or VMA if an electrical signal is being measured, and noise(RMS) is measured on the same optical signal or electrical signal, respectively.

Important parts of the measurement procedure for RN can be found in IEEE Std. 802.3 CL 68.6.7 (LRM). Some comments:

- For purposes of this document, the definitions and procedures generally apply to both optical and electrical signals. Optical terms (such as power) and units can be converted to corresponding electrical terms (such as voltage) and units.
- The test pattern defined for OMA in IEEE 802.3 Clause 68, or other standard relevant for the application, shall be used regardless if the RN measurement is being done on an optical or an electrical signal.
- The 4th-order Bessel-Thomson response is to be used only for optical measurements of RN. The bandwidth of the Bessel-Thomson response is called out in the relevant standard for the application. RN in the electrical domain is defined in a bandwidth of 12 GHz.
- Location of histograms are shown in Figure 68-4 in 802.3 Clause 68.
- Noises at both logic levels should be measured: logicONEnoise(rms) and logicZEROnoise(rms). Apply the rms technique according to the equation:

$$noise(RMS) = \sqrt{(logicONEnoise(RMS)^2 + logicZEROnoise(RMS)^2)/2}$$

- The equation for RN is given above. A calculation of Qsq is not required, nor is a calculation in units of dB/Hz, such as for transmitter RIN. If logicONEnoise(RMS) equals logicZEROnoise(RMS) then RN equals 1/Qsq.

D.9 Waveform Distortion Penalty (WDP)

WDP is a waveshape metric for waveform filtering and/or nonlinear distortion. WDP uses the same procedure as defined for TWDP in IEEE 802.3 Clause 68.6.6 (LRM).

- For purposes of this document, the definitions and procedures generally apply to both optical and electrical signals. Optical terms (such as power) and units can be converted to corresponding electrical terms (such as voltage) and units, etc.
- WDP is not restricted to transmitter measurements (hence, the "T" is dropped).
- The 4th-order Bessel-Thomson response is to be used only for optical measurements of WDP, such as calibration of an optical receiver test system. The bandwidth of the Bessel-Thomson response is called out in the relevant standard for the application.
- The definition of electrical WDP assumes a measurement bandwidth of 12 GHz. A different measurement bandwidth can be corrected for by processing the captured waveform before the WDP calculation. However, a higher bandwidth is expected to have little effect on the result.
- PRBS9 is the normative test sequence for this specification.
- To improve measurement accuracy, uncorrelated jitter and noise should be reduced. For IEEE 802.3 CL 52, sinusoidal interference and sinusoidal jitter are turned off.
- Averaging should be used to further reduce instrumentation and measurement noise so their effect on the results are negligible.
- Specific code for calculating WDP is found in Appendix G

D.10 Electrical Compliance Signal at B'' for the SFP+ Module Transmitter

Figure 30 shows the test configuration for testing SFP+ transmitters. It applies to all SFP+ transmitter types.

The receive channel of the calibration setup is exercised by the upper crosstalk generator in Figure 28 to ensure that the crosstalk within the setup is acceptable. The crosstalk specifications of Table 11 are to be achieved through the mated host and module compliance boards and into appropriate test equipment.

The compliance signal at B'' has deliberate ISI and sinusoidal jitter. It is calibrated through the Host Compliance Board to deliver the DDJ or DDPWS, UJ, and Y1 or Y2 specified in Table 11. The compliance signal is applied to the module under test in place of the Host Compliance Board, with receive side active, so that the transmitted signal can be assessed as specified by the supported transmission standard e.g. 10GBASE-SR, 10GBASE-LR or 10GBASE-LRM. There are four conditions in all: large and small signals, under-compensated and over-compensated. The opposing direction bit stream shall be asynchronous PRBS31 or valid 64B/66B bit stream.

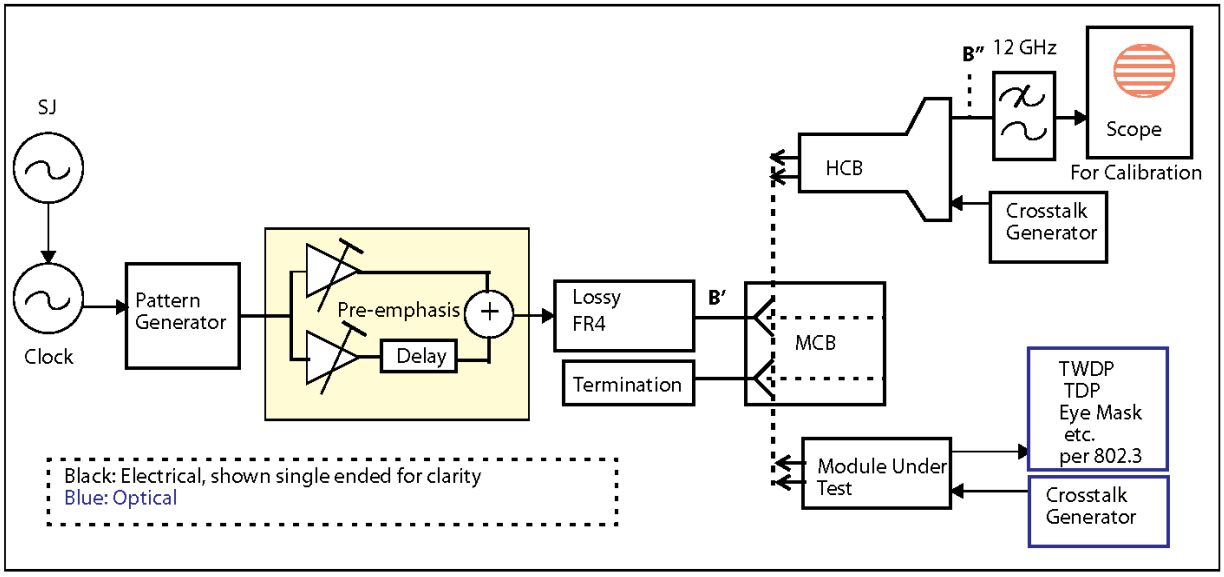


FIGURE 30 COMPLIANCE SIGNAL GENERATOR FOR MODULE TRANSMITTER

The emphasis settings are adjusted to give the specified DDJ (over-compensated) and DDPWS (under-compensated) at B'', in two test conditions. In the over-compensated condition the DDJ shall be equal to the target value in Table 11 while the DDPWS is between 0.045 UI and 0.055 UI. In the under-compensated condition DDPWS shall be equal to the target value in Table 11 while the DDJ is between 0.075 UI and 0.1 UI. The amplitude is adjusted so that an eye mask measurement shows that the compliance signal meets the specified Y1 or Y2 at a hit ratio of 5x10^(-5). The sinusoidal jitter (SJ) is adjusted to give the specified UJ. Otherwise, the compliance signal is clean and low noise. There are no deliberate Gaussian or "random" impairments other than crosstalk.

The single ended reflection coefficients looking to the right of the HCB and the single ended reflection coefficients looking to the left of the MCB as shown in Figure 30, shall be according to:

$$Sxx(dB) \leq 20 \qquad \text{f in GHz from 0.01 to 5.5}$$

$$Sxx(dB) \leq -25.8 + 1.053 \times f \qquad \text{f in GHz from 5.5 to 15.}$$

The compliance signal complies to the mask in 3.6.1, and has margin to the dimensions given by X1, X2 (jitter margin). The large signal has margin to the dimension given by Y1 and approaches Y2 closely, while the small signal approaches Y1 closely and has margin to Y2.

The frequency of the SJ is significantly higher than the bandwidth of the clock recovery unit used to assess the signal transmitted by the module (specified as 4 MHz). Care should be taken that this frequency does not beat against the sampling frequency used to measure the averaged waveform in a TWDP measurement. It must not have a harmonic relationship to the pattern repetition frequency.

The patterns to be used for calibration are specified by the appropriate appendix, e.g. D.3 . The patterns to be used with the module, both transmitted and received, are defined by the supported transmission standard. Other characteristics of the compliance signal are defined by the supported transmission standard.

Note that TJ is not intended to be near the maximum TJ allowed in Table 11, and apart from deliberate SJ, there should be much less UJ than the maximum allowed in

Table 11. It is recommended that adequate averaging be used in TWDP, DDJ and DDPWS measurements to average the effect of the uncorrelated jitter. Table 20 lists the estimated parameter values for an ideal stressed signal generator.

TABLE 20 ESTIMATED PARAMETER VALUES FOR AN IDEAL STRESSED SIGNAL GENERATOR

Parameter	Value	Unit
Delay	1	UI
Filter bandwidth	For Further Study	GHz
VMA Min at B''	For Further Study	mV
VMA Max at B''	For Further Study	mV
Rise times at B''	For Further Study	ps

D.11 Test Method for a Host Receiver for a Limiting Module

This clause provides guidance for jitter tolerance testing at the RX host compliance point C. Compliance is required with input jitter, vertical eye opening (Y1), and vertical peak level (Y2) as specified in Table 8. Compliance is defined at the error rate(s) set by the appropriate optical standard. There are two test conditions; once each for the sensitivity and overload vertical eye parameters conditions.

Further information on definitions and test methods for stressed-eye jitter tolerance are contained in the references (FC-MJSQ and OIF-CEI).

D.11.1 Test Equipment and Setup

A test source is used to continuously generate an appropriate test signal. The test signal shall be appropriately conditioned within the guidelines outlined in D.11.2 to exhibit the appropriate jitter stress.

An RF attenuator or other output amplitude control of the test source may be required to set the vertical eye opening of the stressed eye.

The test equipment measured at C looking into the low pass filter shall have better than 20 dB return loss up to 12 GHz.

The output return loss properties of the test system when measured at C'' with the Module Compliance Board shall be 2 dB better than the specifications of Table 12 up to 8 GHz and 1 dB better up to 11 GHz.

It is required that the receiver under test include a mechanism to allow measurement of BER performance.

D.11.2 Stressed-Eye Jitter Characteristics

This section describes required test signal characteristics along with considerations and suggested approaches for test signal generation. The test signal is generated by the functions shown in Figure 31 or by equivalent means. Figure 32 illustrates how the jitter parameters in Table 8 map to the jitter components in the stressed-eye test signal.

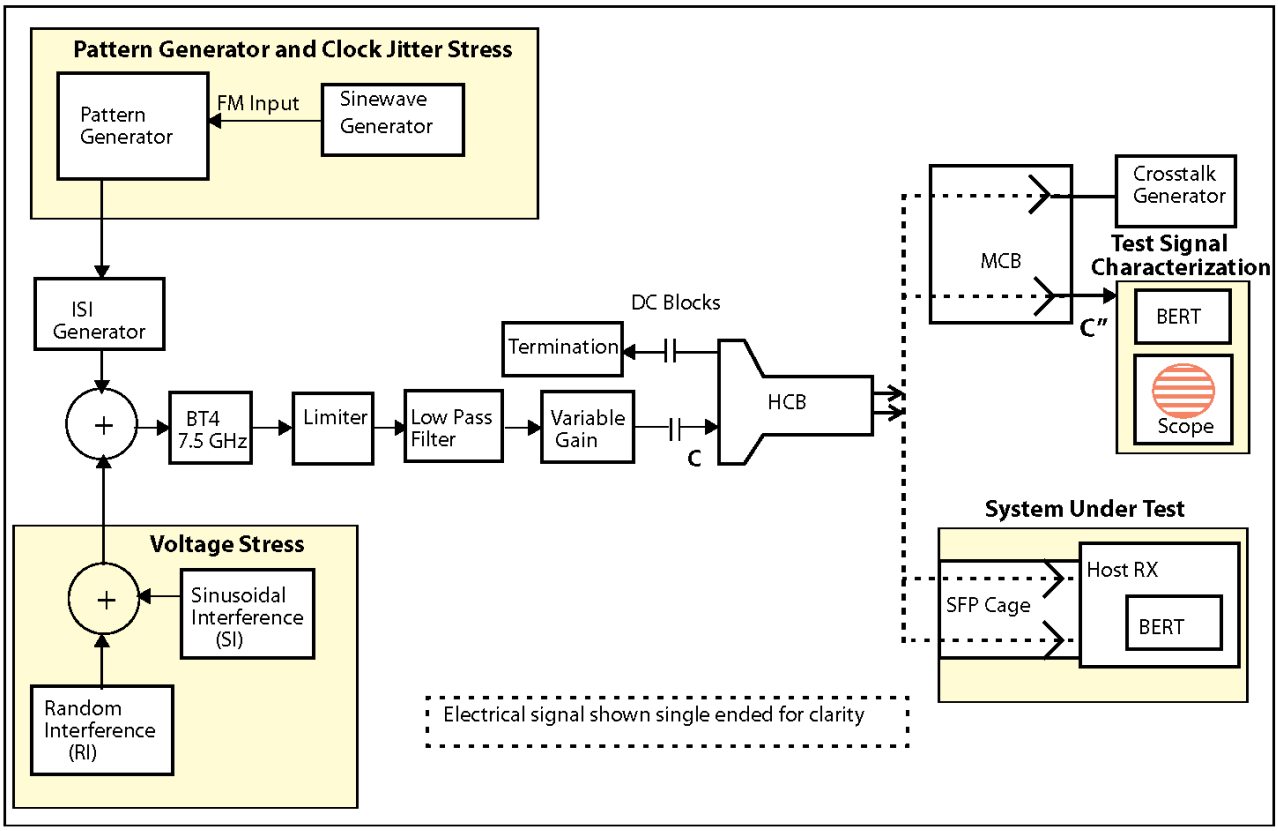


FIGURE 31 JITTER TOLERANCE TEST CONFIGURATION

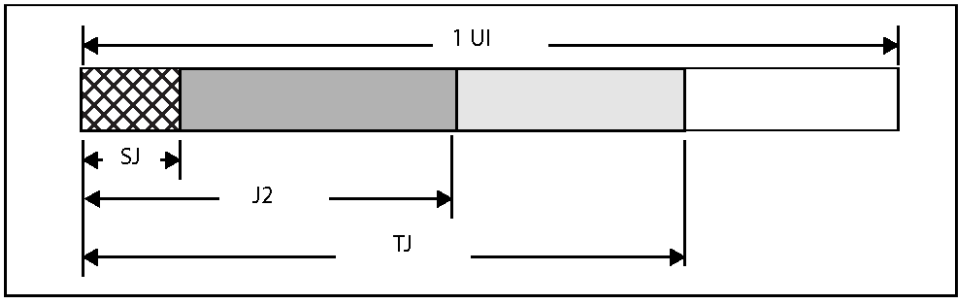


FIGURE 32 STRESSED EYE JITTER COMPONENTS

The 0.05 UI SJ component of 99% Jitter (J2) is defined for frequencies much higher than the CDR bandwidth (e.g. ~20 MHz). At lower frequencies the CDR must track additional applied SJ as detailed in Figure 10 and IEEE 802.3 CL52.8.1.

The balance of the J2 is composed of a combination of the following forms of jitter: ISI, sinusoidal interference (SI), and random interference (RI) all passed through a limiting function.

The signal at C'' shall have DDPWS as defined by Table 8. Magnitude of any DCD (see D.3.1) in the test shall not exceed 0.02 UI.

ISI jitter creation may be achieved by the ISI generator through the use of a low pass filter, length of FR4 trace, length of coax cable or other equivalent method. It is required that this signal be passed through a limiter function to ensure that the resulting jitter is not totally equalizable jitter. A suitable limiter function may be implemented using a discrete limiting amplifier followed by a low pass

filter and an attenuator. The low pass filter emulates the bandwidth and/or slew rate of a practical limiter. The attenuator is used to set the output amplitude to minimum and maximum values allowed by the eye mask coordinates of Table 8.

A voltage stress is to be applied before the limiter. This stress is composed of a single tone sinusoidal interferer (SI) in the frequency range 100 MHz to 2 GHz and a broadband noise source (RI) with a minimum power spectrum of -3 dB at 6 GHz and minimum 7 crest factor. It is the intent that this combination of voltage stress and limiting function introduce pulse-shrinkage jitter behavior. However no more than 20% of the J2 is created by the sinusoidal interferer.

Jitter generation mechanisms for the pattern generator are typically based on phase modulation of the clock source, edge modulation of a variable delay line or a combination thereof.

Any approach that modulates or creates the appropriate levels and frequencies of the jitter components is acceptable.

D.11.3 Calibration

Calibration of the test signal is to be performed using the guidelines for test setup in D.11.1 and illustrated in Figure 31. The aim of the calibration is to achieve a test signal exhibiting jitter stress in accordance with Table 8.

The test signal should be calibrated differentially into standard instrumentation loads. If complementary single-ended signals are used they should be carefully matched in both amplitude and phase.

For improved visibility for calibration, it is imperative that all elements in the signal path (cables, DC blocks, etc.) have wide and flat frequency response as well as linear phase response throughout the spectrum of interest. Baseline wander and overshoot/undershoot should be minimized.

An AC coupling 3 dB corner frequency of 20 kHz is expected to be adequate to eliminate baseline wander effects, however high frequency performance is critical and must not be sacrificed by the AC coupling.

Jitter requirements are defined for a probability level of 1x10^(-12). To calibrate the jitter, methods given in CEI 2.C Annex and MJSQ Chap 8 are recommended. Given random jitter and the nature of the long test patterns, low probability jitter events will likely be present. It is recommended for jitter calibration that a technique that can accurately measure low probability events should be used to avoid overly stressful test conditions.

It is recommended that the actual compliance test pattern be used during calibration. For jitter stress calibration it is permissible, however, to use any appropriate test pattern which still results in the creation of a compliance test pattern with the appropriate jitter stress.

D.11.4 Calibration Procedure

The vertical eye opening and peak level should be set approximately to the levels specified in Table 8.

With an applied calibration test pattern and no additional jitter stress applied; the intrinsic jitter of the test source due to intrinsic noise and finite bandwidth effects should be measured and calibrated. The 99% jitter (J2) shall be <0.15 UI and TJ <0.25 UI.

SJ should be added until the J2 component of jitter increases by 0.05 UI above the measured reference level. This should be high frequency SJ well above the CDR

bandwidth. The SJ frequency should be asynchronous to the characteristic frequency of the signal.

Next, additional high probability jitter as specified in D.11.2 should be added by the ISI generator until at least 80% of the J2 has been created. The Sine Interferer amplitude should then be turned on and adjusted until the required level of J2 is achieved. The frequency of any Sine interferer should be asynchronous to the characteristic frequency of the signal.

A compliant test signal exhibits data dependent pulse width shrinkage as specified in Table 8. Data dependent pulse width shrinkage is defined in D.3 . This is measured with noise and clock-jitter sources turned off.

Once the required level of J2 has been achieved turn on the crosstalk source that should be set such that at the output of the Host Compliance Board the amplitude and the rise and fall times should be as given in Table 8. The crosstalk pattern should be PRBS31 or valid 64B/66B signal and should be asynchronous with the data. Then the RI (random interference) should be added until the required value of TJ is achieved at a probability of 1x10^(-12).

If necessary the sine interferer should be readjusted to obtain the required level of J2 and if the sine interferer is changed then the random interferer should be readjusted to obtain the required level of TJ. Iterative adjustments of the sine interferer and random interferer should be made until the required values of both J2 and TJ are achieved.

If necessary, the vertical eye opening should be readjusted to required levels.

It should be verified that the vertical eye opening and peak level specification is met.

Care must be taken when characterizing the signal used to make receiver tolerance measurements. The intrinsic noise and jitter introduced by the calibration measurement equipment (e.g. filters, oscilloscope and BERT) must be accounted for and controlled. If equipment imperfections affect the results materially, corrections such as RSS deconvolution of Gaussian noise and jitter should be used.

D.11.5 Test Procedure

Testing should be performed differentially through a Host Compliance Board (see C.2 .

Using a test signal calibrated conforming to D.11.1 and calibrated as per D.11.4, operate the system with an appropriate compliance test pattern for the relevant application (10G Ethernet, 10GFC, or 10G Ethernet with FEC).

All signals and reference clocks that operate during normal operation shall be active during the test including the other host signal path in the duplex pair. The other signal path shall be asynchronous.

The opposing direction bit stream (than the one being tested) shall be asynchronous PRBS31 or valid 64B/66B signal.

The sinusoidal jitter is stepped across frequency and amplitude range according to Figure 10 while monitoring the BER. The BER shall remain < 1x10^(-12).

D.12 Limiting Module Receiver Compliance Tests

Compliance to the specifications at C' Table 12 and Table 13 must be met over the range of input optical signals specified by standards supported e.g. IEEE 802.3 Clause 52 and calibration procedure defined in Clause 52.9.9.

This test includes the effects of crosstalk within the module and within the Module Compliance Board. The module transmit path is operational. The transmit path input of the Module Compliance Board is connected to a pattern generator and calibrated through a Host Compliance Board. The amplitude and rise/fall times are given in Table 12. Testing for compliance at point C' is done through a Module Compliance Board.

The pattern for the crosstalk source is PRBS31 or a valid 64B/66B sequence. The crosstalk source is asynchronous to the TP3 test source.

The minimum test conditions (vertical eye closure penalty, VECP[min] and stressed eye jitter, J(min) for stressed receiver sensitivity defined in IEEE 802.3 clause 52 were chosen as sufficient to ensure compliant receivers. Consequently, test conditions more severe than the minimum requirements represent an overstress condition for which compensation is appropriate.

Compensation for overly stressful VECP is straightforward; the stressed receiver sensitivity (SRS) maximum can be adjusted one-for-one for any VECP overstress (or a small amount of under-stress).

SRS[compensated, dBm] = SRS[max, dBm] + dVECP[overstress, dBo]

where

dVECP[overstress] = VECP[measured, dBo] - VECP[min, dBo].

Compensation for overly stressful jitter is less straightforward since definition permits compositions over a trade-off range of deterministic and random jitter. Further, there is no generally accepted practice for compensating deterministic jitter and the only recourse is re-calibrating the test source. Fortunately, most cases of overly stressful jitter are expected to be due to excessive random jitter.

Where the jitter composition is known or can be measured, any excess random jitter can be backed out of the measured result, or specifications in Table 13, Total Jitter and Eye Mask X1 coordinate, can be adjusted to accommodate the excess input signal.

D.13 Test Method for a Host Receiver with a Linear Module

A compliance setup for a host for use with a linear module receiver is shown in Figure 33. The host input at point C is tested for BER compliance with test signals that represent the worst case waveshape and noise properties expected from the output of a module during compliant operation.

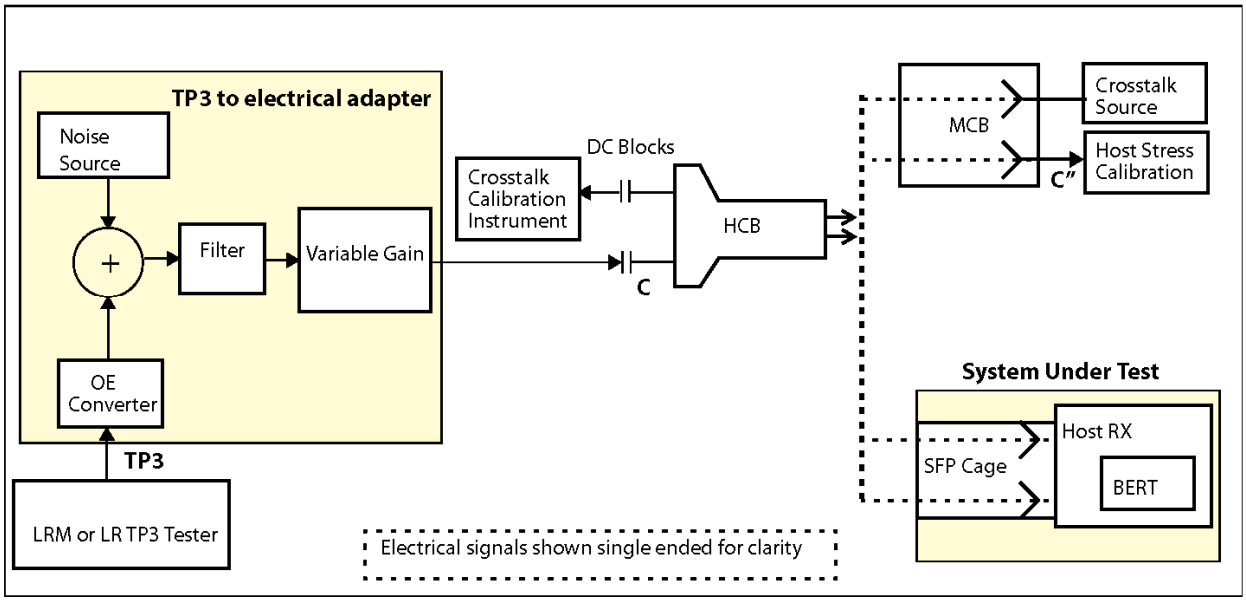


FIGURE 33 TP3 TO ELECTRICAL ADAPTOR FOR HOST THAT OPERATES WITH LINEAR MODULES

D.13.1 Test Description and Procedure for Host Receiver for Linear Module

Compliance shall be achieved for each of the three TP3 pulse shapes defined for 10GBASE-LRM in IEEE 802.3 Clause 68.6.9 and for the one 10GBASE-LR stressed receiver conformance test signal defined in IEEE Std 802.3 Clause 52.9.9. Compliance shall be achieved over the range of VMA in Table 9. The TP3 tester block is the same test system as defined by the LRM or LR standard for testing the TP3 compliance point. LRM and LR are chosen because this combination of tests includes both high distortion with low noise, and low distortion with high noise. Testing with an SR equivalent input is not required as the noise and distortion are between those for LR and LRM.

The TP3 to electrical adapter as shown in Figure 33 converts the TP3 test signal(s) into electrical signal(s) with output VMA, noise (RN) and distortion (WDP) properties defined in Table 9.

The specifications given in Table 9 are as measured during calibration at C'' through the Module Compliance Board.

The noise source, in conjunction with the other blocks, is intended to represent the additive noise properties of a worst-case linear module. The magnitude of the noise is calibrated such that the RN values at C'' are consistent with Table 9. The spectrum of the noise source at the summing point is white with a 3 dB frequency of at least 10 GHz. The noise measured at C'' represents the noise of the module and the optical signal combined. The noise source crest factor should be at least 6.

The filter and gain blocks are intended to represent the deterministic dWDP and gain Table 9, including LR, the filter has a bandwidth of 7.5 GHz. For the high WDP cases in Table 9, the frequency response of the filter is set such that the WDP value specified in Table 9 at C'' for the split-symmetrical LRM stressor is achieved. This bandwidth is expected to be approximately 4.5 GHz. In all cases, the overall response of the adapter has a Bessel Thomson response.

The gain block and/or the input optical power level can be used to adjust VMA.

During calibration and host compliance testing, crosstalk source see Figure 33 shall be an asynchronous PRBS31 or 64B/66B signal.

Care must be taken to not induce greater than 0.02 UI of DCD at C''

A balun or other means provides a differential signal.

The test signal output shall be AC coupled. An AC coupling 3 dB corner frequency of 20 kHz is expected to be adequate to eliminate baseline wander effects, however high frequency performance is critical and must not be sacrificed by the AC coupling.

The output return loss properties of the test system when measured with Module Compliance Board shall be at least 2 dB better than the specifications of Table 12 up to 8GHz and 1 dB better up to 11GHz.

Any implementation of the measurement configuration may be used, provided that the resulting signal and noise match those defined in Table 9.

Under all specified test conditions, a BER of better than 1x10^(-12) shall be achieved. The transmitter of the port under test and all other ports operate in normal operation, including termination. The transmitter of the port being tested is terminated through the Host Compliance Board with a DC block and 50 Ohms at each Tx SMA connector.

D.13.2 Host Linear Tester Calibration

The output of the Host Compliance Board is plugged through the Module

Compliance Board into laboratory equipment for calibration.

Calibration should be done with all tester elements in place, although some components may be shut down, such as jitter and noise, while other elements are being calibrated - see below. After calibration is completed, all components are set to their calibrated levels for testing.

RN of the host test system is adjusted via the magnitude of the adapter's noise source. Calibration should use the RN measurement methods given in section D.8 . RN values are given in Table 9 for each test condition. The crosstalk source must be calibrated to the requirements in Table 7 and running during calibration of RN. After calibration and during host compliance testing, the crosstalk calibration instrument can be removed and replaced with 50 Ohm terminations, although DC blocking must be maintained.

WDP of the host test system is set via the filter in the adapter. If the calibration is off by a small amount, the ISI generator in the TP3 tester can be adjusted to obtain the required values.

Although WDP is a characteristic of an electrical signal in this case, its units are in dBo to better align with WDPo out of a linear optical module, which is also given in dBo.

After calibration, the Host Compliance Board is plugged into the host receiver under test for compliance testing.

D.14 Linear Module Receiver Compliance Tests

Linear module receiver compliance tests ensure that noise generation, wave-form filtering and other distortion due to the module are kept within acceptable bounds when tested with the optical input signals as specified in the standards supported by the module, e.g. IEEE 802.3 CL 52 and/or CL 68.

D.14.1 Linear Module Receiver Noise Compliance Test

The module receiver can be tested for noise compliance by measuring how much noise it passes and adds to an input test signal. Figure 34 is a block diagram of a test system that defines the module receiver noise test.

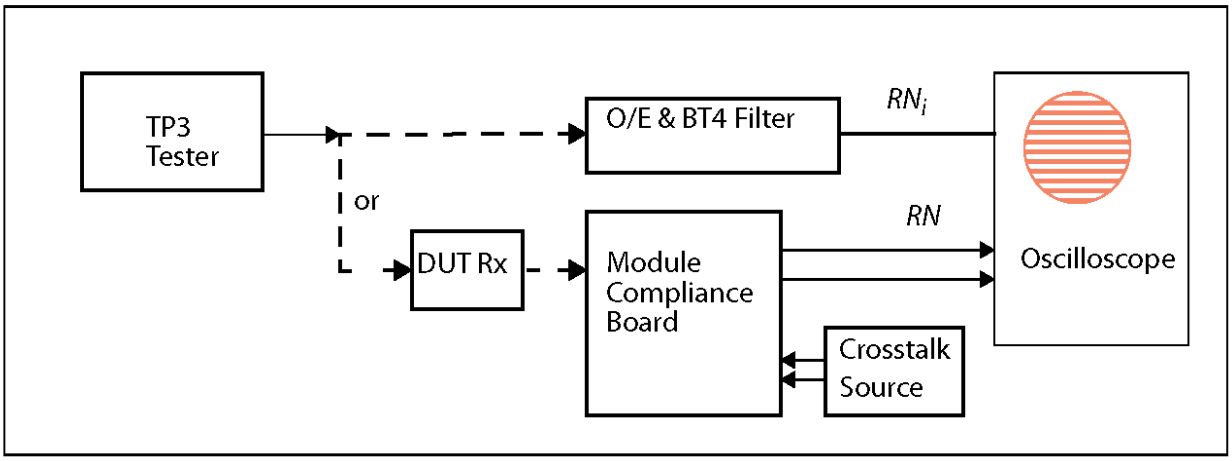


FIGURE 34 LINEAR MODULE RECEIVER NOISE TEST

This test includes the effects of crosstalk within the module and the Module Compliance Board. The transmit path input of the Module Compliance Board is connected to a crosstalk source and calibrated through a Host Compliance Board. The crosstalk amplitude and rise/fall times are set to the values given in Table 12. The pattern for the crosstalk source is PRBS31 or a valid 64B/66B signal. The crosstalk source is asynchronous to the TP3 test source. After calibration, the Host Compliance Board is replaced with the module under test. The module transmit path is operational during compliance testing.

The TP3 tester should be set to the OMA/VMA pattern for this test as defined in D.7 .

The waveform shaping stress of the TP3 tester is enabled. The sinusoidal jitter and/or sinusoidal interference of the TP3 tester should be disabled or set to very low magnitudes for this test.

RNi of the TP3 tester is set to the level specified by Table 21.

The TP3 tester is connected into the module under test. The module is plugged into the Module Compliance Board, which in turn is connected to the oscilloscope. The relative noise of the module output signal, RN, is then measured. The relative noise measurement method is described in D.8 .

Relative noise of the TP3 test signal RNi is characterized through a reference O/E converter and 4th-order Bessel Thomson filter and a digital oscilloscope. If the noise of the TP3 test source does not match the target value in Table 21, RN can be corrected using the following equation:

$$RN = \sqrt{(RN_{measured})^2 - 1.24 \times RN_i(\mathrm{target}) \times (RN_i - RN_i(\mathrm{target}))}$$

where RNmeasured includes the effect of actual TP3 tester noise at the module output, RNi is the actual TP3 tester noise, and RNi(target) is the target test noise given in Table 21 for the test conditions. The resulting noise result is to be compared against the compliance limit specified in Table 14. Compliance must be met over the range of optical power specified by the standards supported by the module.

TABLE 21 TARGET RNi VALUES

Application	RNi (target)
LRM pre-cursor	0.0219
LRM split-symmetrical	0.0269
LRM post-cursor	0.0213
LR	0.014
SR	0.020

For LRM, RNi should be within 1 dBo of the appropriate value given in Table 21. For LR and SR, RNi should be no more than 1 dBo greater than the appropriate value in Table 21; any lower value is allowable.

This procedure is described for an oscilloscope as the measuring instrument. However, noise generated by a practical scope can affect the result. The noise due to the scope is calibrated out of the result by subtracting the square of the scope's noise from the noise of the RN measurement as appropriate, so as to obtain the relative noise associated with the signal under test. For electrical scope noise measurement, the scope inputs are terminated with 50 Ohms termination. For optical scope noise measurement, the scope input should have zero light.

D.14.2 Linear Module Receiver Distortion Penalty Compliance Test

This section defines dWDP, a measure of waveform filtering and other distortion associated with the linear optical receiver. The block diagram dWDP test system that defines linear module receiver distortion test is shown in Figure 35.

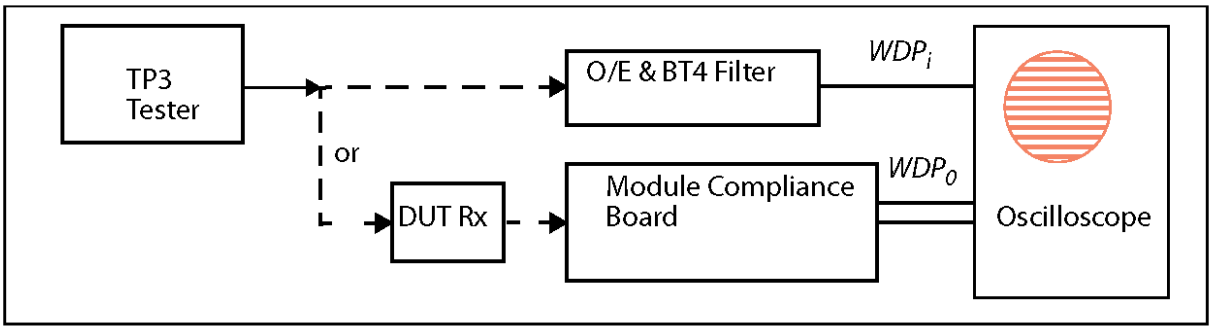


FIGURE 35 MODULE RECEIVER WAVEFORM PENALTY COMPLIANCE TEST

- WDPi and WDPo in Figure 35 are measured using the WDP method defined in D.9 . WDPi of the TP3 test signal is first characterized through an O/E converter and 4th-order Bessel Thomson filter and a digital oscilloscope. For 10GBASE-LRM, this signal should represent the waveforms described in IEEE Std. 802.3 CL 68.6.9, and for 10GBASE-LR, this signal represents the waveform described in IEEE Std. 802.3 CL 52.9.9.
- The TP3 tester is removed from the O/E converter and connected into the module under test. The module in turn is plugged into a Module Compliance Board which in turn is connected to the oscilloscope. WDPo of the module output signal is then measured.

Although WDPo is based upon measurements of an electrical signal, its units for a linear optical module output are in dBo to allow a direct comparison with the optical input signal in the equation for dWDP below.

The distortion contributed by the module is determined by the following equation:

$$dWDP = WDP_o - WDP_i$$

dWDP is to be compared against the compliance limit specified in Table 14. Each dWDP must comply for each specified TP3 condition. The TP3 tester is the same test system as defined by the relevant standard for testing the TP3 compliance point.

D.14.3 Linear Module Receiver Output Differential Peak-Peak Voltage

A compliant TP3 stress receiver tester for the relevant application (SR, LR, or LRM) is connected to the module receiver input. The OMA test pattern for the application should be used, and all stress impairments such as sine jitter, sine interference, ISI, and noise should be turned off. The rise/fall time should be 47 ps 20-80%. When observed through a 7.5 GHz reference O/E converter, the input waveform should have no overshoot or ripple.

The output of the module is measured with a Module Compliance Board connected into an oscilloscope. The measurement bandwidth is 12 GHz. A wider measurement bandwidth is expected to have only a minor effect on the result. If the measurement bandwidth affects the results, it can be corrected for by post processing. Averaging is used to eliminate noise from the measurement. The peak to peak swing of the differential signal is measured and compared against the limit in Table 14.

D.15 AC Common Mode Voltage

The SFI transmitter and channel limit but do not eliminate AC common mode voltage generation. SFI receivers, both module and host, must operate fully with the maximum allowed input common mode voltage. Common mode voltage often gets generated due to the crossing points of the driver outputs (P and N) being shifted from 50%, impedance mismatch, mismatch of the PCB traces, or mode conversion.

D.15.1 Definition of AC Common Mode Voltage

The common mode voltage at any time is the average of signal+ and signal- at that time. The RMS AC common mode voltage is calculated by applying the histogram function over one UI to the common mode signal. As AC common mode generation is very sensitive to the cable or scope delay mismatch, it is recommended to delay match the scope inputs for any measurements.

D.15.2 AC Common Mode Generation Test

The test pattern for AC common mode generation is either pattern 1 (BnBi) or pattern 3 (PRBS31) as defined in IEEE CL 52.9.1.1. It is expected that any 64B/66B scrambled signal should give a similar result.

D.15.3 AC Common Mode Tolerance Test

The test pattern for AC common mode tolerance is either pattern 1 (BnBi) or pattern 3 (PRBS31) as defined in IEEE CL 52.9.1.1. It is expected that any 64B/66B coded signal should give a similar result.

If the transmitter output does not generate a sufficient amount of AC common mode then the method to generate additional amounts is by adjusting the P and N delay until the right amounts is generated.

D.16 Termination Mismatch

Termination mismatch is defined as the percent difference between the complimentary Zp and Zn resistors as shown in Figure 18. Termination mismatch is defined as:

$$\Delta Z_M = 2 \times \frac{Z_p - Z_n}{Z_p + Z_n} \times 100$$

Alternatively, the termination mismatch can be measured by applying a low frequency test tone to the differential inputs as shown in Figure 36. The test frequency must

be high enough to overcome the high pass effects of the AC coupling capacitor. The measured differential output or input impedance is designated by Zdiff.

Low frequency termination mismatch is then given by:

$$\Delta Z_M = 2 \times \frac{I_p - I_n}{I_p + I_n} \cdot \frac{Z_{diff} + 100}{Z_{diff}} \cdot 100$$

where Ip and In are the current flowing into the SFI port as shown in Figure 36. Zs is the effective series impedance between the driver terminations Zp and Zn and the AC Ground.

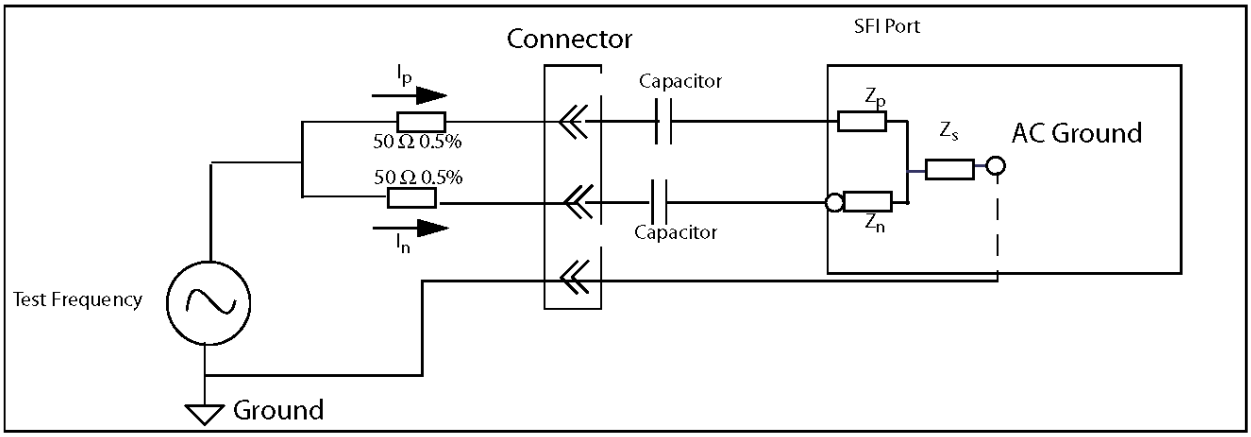


FIGURE 36 AC TERMINATION MISMATCH MEASUREMENT

E. SFP+ Direct Attach Cable Specifications "10GSFP+Cu" (Optional)

A passive copper cable compliant to this appendix is identified using the 2-wire management defined in SFF-8419 and memory map of SFF-8472.

This appendix describes additional requirements or exceptions to the linear host specification of Section 3 to implement passive direct attach SFP+ cable assemblies.

The compliance points for SFP+ Direct Attach Cable (10GSFP+Cu) are the same as host compliance test points 3.3.1 and the module compliance test points in 3.3.2.

All SFI test equipment must have 50 Ohms single ended impedance on all test ports.

Each Tx_Disable contacts of 10GSFP+Cu passive cable assemblies shall be pulled to VccT with a 4.7 kOhms to 10 kOhms in the module. The Rx_LOS contacts in the module shall be pulled low in the module for 10GSFP+Cu passive cable assemblies. Direct connection of Rx_LOS to VeeR is allowed.

Active cable assemblies must operate with existing linear or limiting specifications of Section 3.

This specification does not assume additional transmit pre-emphasis beyond the level required to meet the jitter specifications at point B (see Table 6) and TWDPc specification (see Table 22) at point B. Increasing the transmit pre-emphasis may increase cable reach, however it may increase transmitter DDJ and is outside the scope of this specification.

Warning: 10GSFP+Cu can only be used on systems with common grounds. Connecting systems with different ground potential with SFP+ direct attach cable results in a short and may cause damage.

E.1 10GSFP+Cu Direct Attach Construction

10GSFP+Cu cable assemblies are effectively constructed out of a pair of SFP+ modules with the OE components replaced with copper cabling as shown in Figure 37. SFP+ Edge card connector contacts are defined in SFF-8419 SFP+ Module and Host Electrical Contact Definition. The cable assembly shall incorporate DC blocking capacitors with at least 4.3 V rating on the RX side and with high pass pole of between 20 kHz and 100 kHz. The drain wire is connected to VeeT and to VeeR. The cable shield directly connects the module A and B cases.

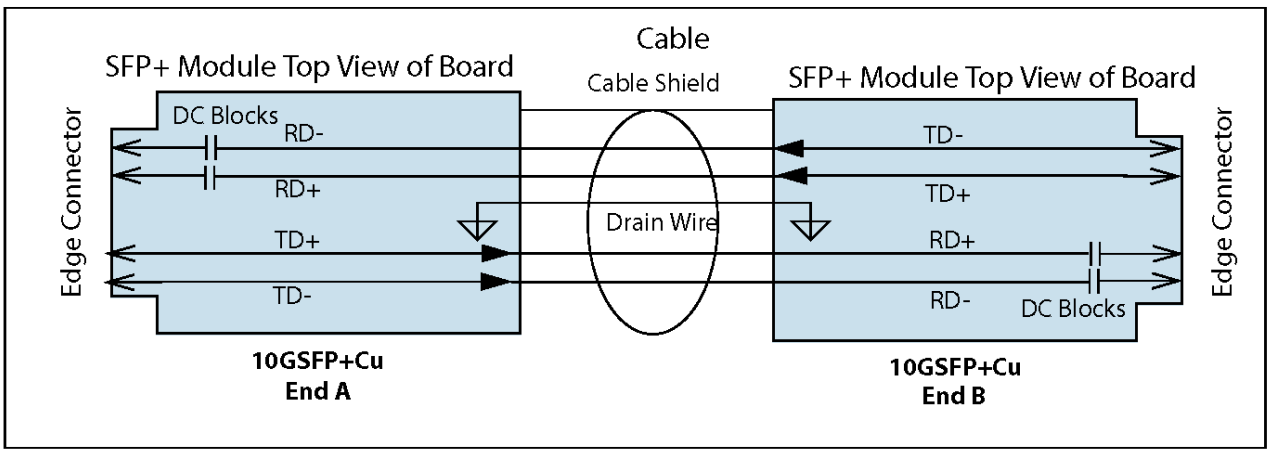


FIGURE 37 10GSFP+CU DIRECT ATTACH BLOCK DIAGRAM

E.2 SFP+ Host Output Specifications For Passive Direct Attach Cables

SFP+ host supporting direct attach cables must meet transmitter output specifications in Table 5 and jitter specifications in Table 6 at reference point B. In addition SFP+ host transmitter must meet the specifications in Table 22.

TABLE 22 SFP+ HOST TRANSMITTER OUTPUT SPECIFICATIONS AT B FOR CU

Parameters- B	Symbol	Conditions	Min	Target	Max	Units
Voltage Modulation Amplitude (p-p)	VMA	See D.7	300			mV
Transmitter Qsq	Qsq	*1	63.1			
Output AC Common Mode Voltage		See D.3			12.0	mV (RMS)
Host Output TWDPc	TWDPc	*2 *3			10.7	dBe
*1 Qsq= 1/RN if the one level and zero level noises are identical and see D.8 .						
*2 Host electrical output measured with LRM 14 taps FFE and 5 taps DFE Equalizer with PRBS9 for copper direct attach stressor, see Appendix G.						
*3 The stressor for TWDPc is given in Table 23 and is included in the code in Appendix G.						

TWDPc is the host transmitter penalty for copper cable stressor shown in Figure 38 and given in Table 23. Code to calculate TWDPc using this stressor is given in Appendix G.

E.2.1 Transmitter Stressor

For TWDPc compliance, a simulated cable response is required. The response is modeled as a set of delta functions with specific amplitudes and delays. The copper stressor was created from measurements of commonly available direct attach SFP+ cables with the transmitter response de-convolved. The stressor is shown in Figure 38 and the values are listed in Table 23. The sum of all stressor components is normalized to an approximate value of 1.

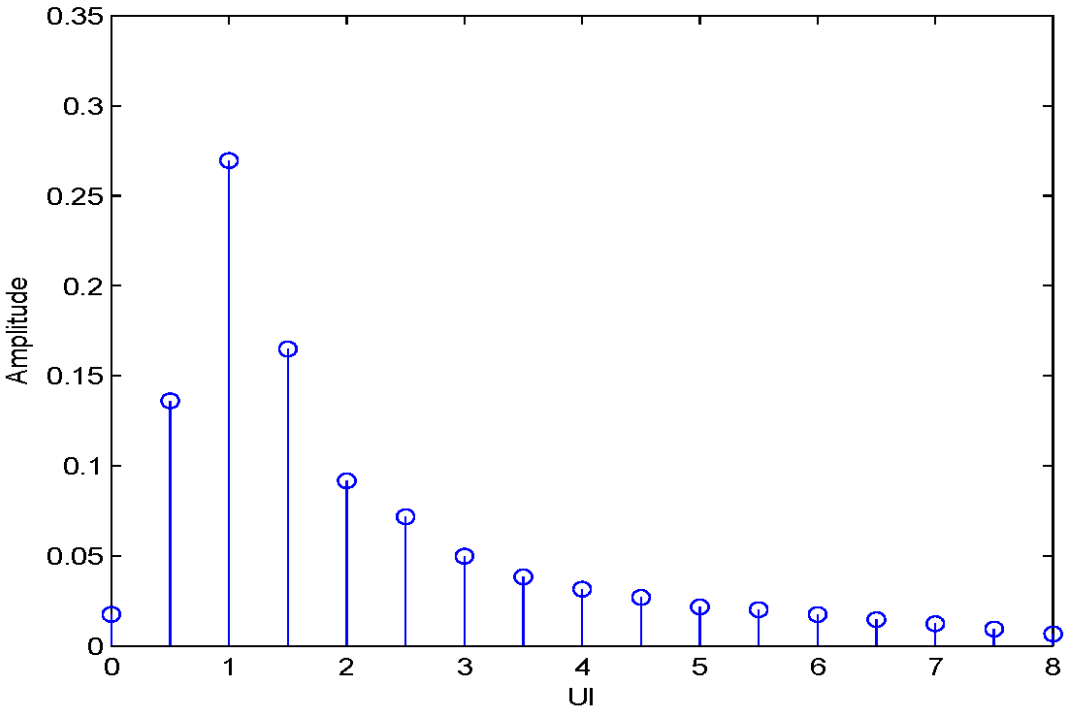


FIGURE 38 10GSFP+CU TWDPC STRESSOR IMPULSE RESPONSE

TABLE 23 10GSFP+CU TWDPC STRESSOR

Delay (UI)	Delay (ns)	Amplitude		Delay (UI)	Delay (ns)	Amplitude
0	0	0.0175		4.5	0.43637	0.0270
0.5	0.04849	0.1360		5.0	0.48485	0.0216
1	0.09697	0.2695		5.5	0.53334	0.0202
1.5	0.14546	0.1649		6.0	0.58182	0.0174
2	0.19394	0.0917		6.5	0.63031	0.0146
2.5	0.24243	0.0717		7.0	0.67879	0.0123
3.0	0.29091	0.0498		7.5	0.72728	0.0094
3.5	0.33940	0.0383		8.0	0.77576	0.0066
4.0	0.38788	0.0315				

E.3 SFP+ Host Receiver Supporting 10GSFP+Cu Input Compliance Test Signal Calibrated at C''

A host that is to support the direct attach copper option is to meet the required 1x10^(-12) BER when tested with the stressed signal described in E.3.1 in addition to the requirements of 3.5.2 relating to a host receiver supporting linear module.

E.3.1 Copper Host Receiver Specifications

The SFP+ host receiver stress generator is described by a set of tapped delay lines described in E.3.2, a suitable length of copper cable is expected to generate the stressor described here. The stress generator must meet the target WDPc (Waveform Distortion Penalty for copper) as given in Table 24. The stressor generator shall implement the noise model as captured in Figure 39 using the parameters given in Table 24. The noise model contains two noise sources: Qsq noise which is relative to the transmitter signal level and shaped by the channel response and No fixed noise (modeling cable NEXT) added post channel. The added noise sources Qsq and No are white and Gaussian in this test.

The sensitivity test shall be made with the minimum VMA and the overload test shall be made with the maximum p-p voltage as given in Table 24.

TABLE 24 10GSFP+ HOST RECEIVER INPUT STRESS GENERATOR AT C''

Parameters- C"	Symbol	Conditions	Min	Target	Max	Units
Waveform Distortion Penalty of the ISI Generator	WDPc	*1 *2		9.3		dBe
Transmitter Qsq	Qsq	*4, *5		63.1		
Post channel fixed noise source	No	*3		2.14		mV(RMS)
Differential Voltage Modulation Amplitude	VMA	*4, D.7		180		mV
Differential Peak-Peak Voltage Overload				700		mV
Input AC Common Mode Voltage		*6, D.15.2			13.5	mV(RMS)
*1 Copper stressor as defined in Table 25. WDPc is measured with reference receiver with 14 FFE taps and with 5 DFE taps, see Appendix G.						
*2 WDPc for the stress is smaller than the transmitter TWDPc due to the VMA loss in the host stressor.						
*3 No is the RMS voltage measured over one symbol period at the output of the MCB in a 12 GHz bandwidth. The source for Qsq should be disabled during this calibration.						
*4 Square pattern with eight ONEs and eight ZEROs.						
*5 Qsq= 1/RN if the one level and zero level noises are identical and see D.8 . Qsq is calibrated at the output of the MCB in a 12 GHz bandwidth with the ISI of the channel model in Figure 39 disabled. The source for No should be disabled during this calibration.						
*6 AC common mode target value is achieved by adjusting relative delay of the P and N signals.						

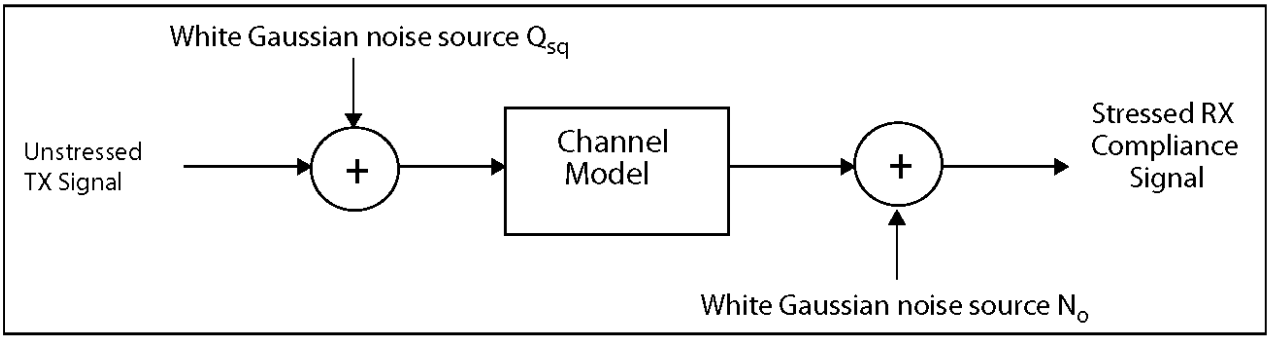


FIGURE 39 BLOCK DIAGRAM OF COPPER STRESSOR NOISE MODEL

E.3.2 Copper Host Stress Generator 1 UI Pulse Response

Copper host stressor was created from measurements of commonly available direct attach SFP+ cables. The response of the copper host stress generator 1 UI pulse response is shown in Figure 40 and the pulse response values are listed in Table 25.

A suitable length of copper cable is an acceptable substitute to the stressor of Table 25 provided it has the same WDPc. The RMS fit between the tabulated pulse response in Table 25 and the measured isolated pulse response should be minimized to get the target WDPc values as listed in Table 24.

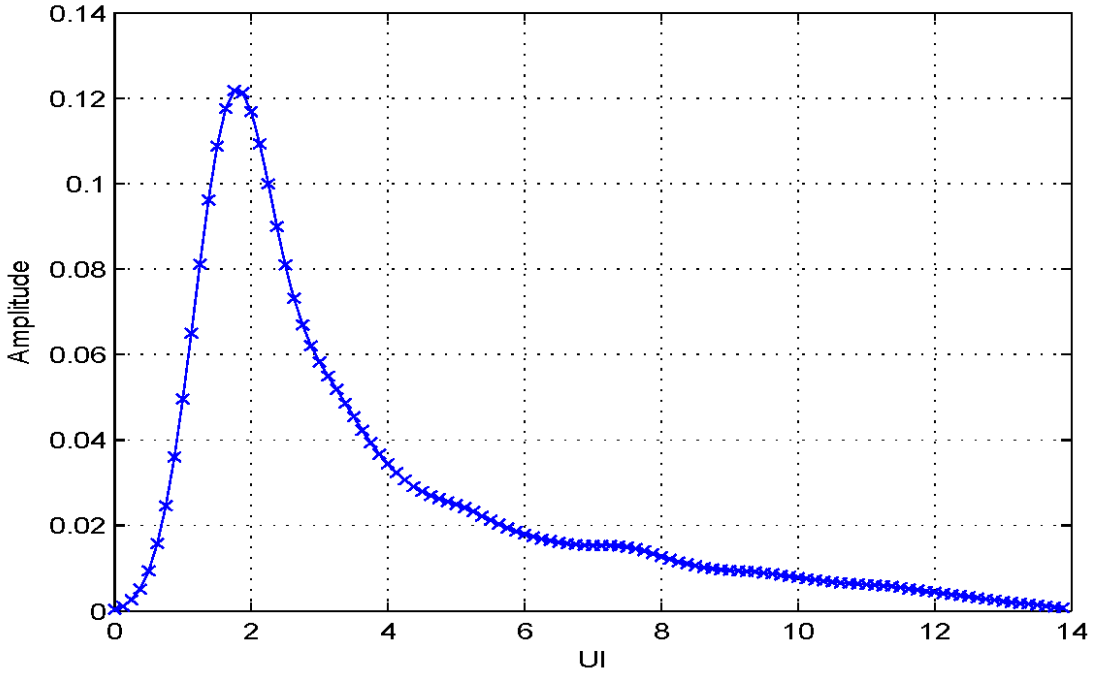


FIGURE 40 STRESS GENERATOR 1UI PULSE RESPONSE WITH 8X OVER-SAMPLING

TABLE 25 STRESS GENERATOR 1 UI PULSE RESPONSE WITH 8X OVER-SAMPLING

Delay (UI)	Delay (ns)	Ampli-tude		Delay (UI)	Delay (ns)	Ampli-tude		Delay (UI)	Delay (ns)	Ampli-tude
0	0.0000	0.0004		4.625	0.4485	0.0270		9.25	0.8970	0.0093
0.125	0.0121	0.0011		4.75	0.4606	0.0263		9.375	0.9091	0.0092
0.25	0.0242	0.0026		4.875	0.4727	0.0256		9.5	0.9212	0.0089
0.375	0.0364	0.0051		5	0.4848	0.0249		9.625	0.9333	0.0087
0.5	0.0485	0.0094		5.125	0.4970	0.0242		9.75	0.9455	0.0084
0.625	0.0606	0.0158		5.25	0.5091	0.0233		9.875	0.9576	0.0082
0.75	0.0727	0.0246		5.375	0.5212	0.0222		10	0.9697	0.0079
0.875	0.0848	0.0360		5.5	0.5333	0.0212		10.125	0.9818	0.0076
1	0.0970	0.0496		5.625	0.5455	0.0204		10.25	0.9939	0.0073
1.125	0.1091	0.0650		5.75	0.5576	0.0194		10.375	1.0061	0.0070
1.25	0.1212	0.0811		5.875	0.5697	0.0187		10.5	1.0182	0.0068
1.375	0.1333	0.0962		6	0.5818	0.0180		10.6250	1.0303	0.0066
1.5	0.1455	0.1088		6.125	0.5939	0.0174		10.7500	1.0424	0.0065
1.625	0.1576	0.1176		6.25	0.6061	0.0169		10.8750	1.0545	0.0063
1.75	0.1697	0.1218		6.375	0.6182	0.0165		11.0000	1.0667	0.0062
1.875	0.1818	0.1213		6.5	0.6303	0.0161		11.1250	1.0788	0.0061
2	0.1939	0.1169		6.625	0.6424	0.0157		11.2500	1.0909	0.0059
2.125	0.2061	0.1093		6.75	0.6545	0.0155		11.3750	1.1030	0.0058
2.25	0.2182	0.1000		6.875	0.6667	0.0154		11.5000	1.1152	0.0055
2.375	0.2303	0.0899		7	0.6788	0.0153		11.6250	1.1273	0.0052
2.5	0.2424	0.0810		7.125	0.6909	0.0153		11.7500	1.1394	0.0049
2.625	0.2545	0.0732		7.25	0.7030	0.0153		11.8750	1.1515	0.0046
2.75	0.2667	0.0670		7.375	0.7152	0.0153		12.0000	1.1636	0.0044
2.875	0.2788	0.0620		7.5	0.7273	0.0150		12.1250	1.1758	0.0041
3	0.2909	0.0583		7.625	0.7394	0.0146		12.2500	1.1879	0.0039
3.125	0.3030	0.0549		7.75	0.7515	0.0141		12.3750	1.2000	0.0037
3.25	0.3152	0.0519		7.875	0.7636	0.0134		12.5000	1.2121	0.0034
3.375	0.3273	0.0486		8	0.7758	0.0128		12.6250	1.2242	0.0030
3.5	0.3394	0.0455		8.125	0.7879	0.0121		12.7500	1.2364	0.0028
3.625	0.3515	0.0423		8.25	0.8000	0.0115		12.8750	1.2485	0.0026
3.75	0.3636	0.0394		8.375	0.8121	0.0110		13.0000	1.2606	0.0022
3.875	0.3758	0.0367		8.5	0.8242	0.0106		13.1250	1.2727	0.0020
4	0.3879	0.0345		8.625	0.8364	0.0101		13.2500	1.2848	0.0018
4.125	0.4000	0.0324		8.75	0.8485	0.0099		13.3750	1.2970	0.0016
4.25	0.4121	0.0307		8.875	0.8606	0.0097		13.5000	1.3091	0.0014
4.375	0.4242	0.0291		9	0.8727	0.0095		13.6250	1.3212	0.0012
4.5	0.4364	0.0280		9.125	0.8848	0.0094		13.7500	1.3333	0.0009
								13.8750	1.3455	0.0008

E.4 SFP+ Passive Direct Attach Cable Assembly Specifications

Passive direct attach cables are tested with a pair of Module Compliance Boards at compliance point B' and C'. SFP+ passive cable assemblies need to meet specification in Table 26.

VCR, VMA, Vcm, and dWDP may be derived using frequency based methodologies that yield equivalent results e.g., utilizing frequency dependent crosstalk and insertion loss transfer functions with transmitter behavioral models.

TABLE 26 10GSFP+CU CABLE ASSEMBLY SPECIFICATIONS AT B' AND C'

Parameter - C' (Cable Output)	Symbol	Conditions	Min	Target	Max	Units
Single Ended Input and Output Voltage Tolerance			-0.3		4.0	V
Output AC Common Mode Voltage	Vcm	*1			13.5	mV (RMS)
Difference Waveform Distortion Penalty	dWDPc	*2, *9, E.4.1, E.4.2 and D.14.2			6.75	dBe
VMA Loss	L	See *3, *9, D.7 , E.4.4			4.4	dBe
VMA Loss to Crosstalk Ratio	VCR	*1, D.7 , E.4.1, E.4.4	32.5			dB
Differential Output/Input Reflection Coefficient 4	SDDxx	0.01-4.1 GHz			*5	dB
		4.1-11.1 GHz			*6	dB
Common Mode Output/Input Reflection Coefficient 7	SCCxx	0.01-2.5 GHz			*10	dB
		2.5-11.1 GHz			-3	dB
Parameter - B'' (Input Test Conditions)	**Symbol**	**Conditions**	**Min**	**Target**		**Units**
Input AC Common Mode Voltage	Vcm	*1, D.15.2		12		mV (RMS)
Signal Rise and fall time Time	Tr/tf	See D.6		34		ps
Crosstalk Source Rise/Fall time (20% to 80%)	Tr, Tf	See D.6		34		ps
Crosstalk Source Amplitude Differential (p-p)				700		mV
WDPi		*8		2.4		dBe
*1 When input common mode voltage is 12.0 mV RMS and when input rise and fall times are 34ps and the amplitude is the max amplitude allowed by Table 6.						
*2 Defined with reference receiver with 14 T/2 spaced FFE taps and 5 T spaced DFE taps, see Appendix G.						
*3 VMA loss is the ratio of VMA measured at input and output, respectively.						
*4 Reference differential impedance is 100 Ohms. The dB value listed here are the same as dBe.						
*5 Reflection Coefficient given by equation SDDxx(dB)= -12 + 2 × SQRT(f), with f in GHz.						
*6 Reflection Coefficient given by equation SDDxx(dB)= -6.3 + 13 x log10(f/5.5), with f in GHz.						
*7 Common mode reference impedance is 25 Ohms. The dB value listed here are the same as dBe						
*8 Adjust DDJ and/or DDPWS by adjusting pre-emphasis until the target WDPi is achieved.						
*9 With input test condition given by parameters B'' given in this table.						
*10 Reflection coefficient given by equation SCCxx(dB) < -7 + 1.6 xf, with f in GHz.						

E.4.1 SFP+ Direct Attach Cable Test Setup

Direct attach cable testing methodology is based on the SFP+ test methodology as defined in section 3.3. The cable is measured through a pair of Module Compliance Boards as shown in Figure 41. This diagram shows the block dia-gram for testing NEXT on cable A end and for measuring WDP on path 1. To measure NEXT on B end and WDP on path 2 the cable end A and B are reversed. The Compliance Signal Generator is described in Figure 30.

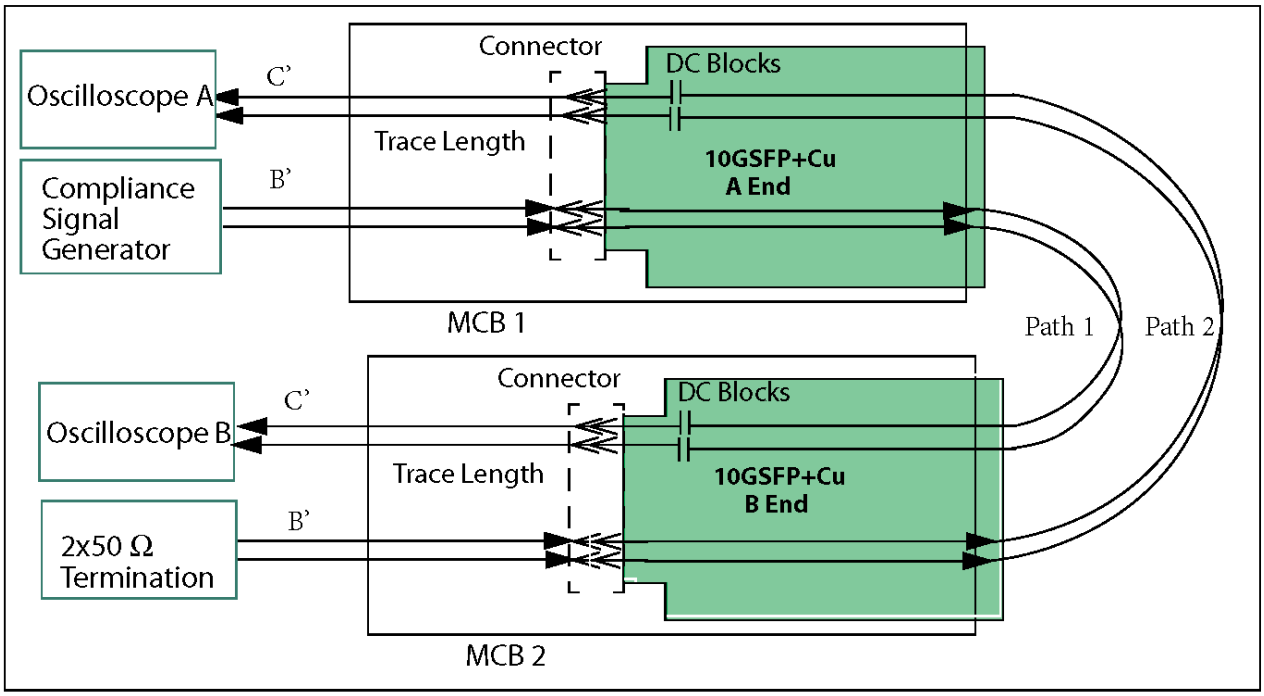


FIGURE 41 10GSFP+ CABLE TEST SETUP

WDPi and WDPO in Figure 42 use the WDP method defined in D.9 . WDPi for copper is measured by plugging Host Compliance Board into the Module Compliance Board 1 and then meeting the target WDPi as listed in Table 26. WDPO is measured by plugging one end of the cable in to Module Compliance Board 1 and the other end in to the Module Compliance Board 2. B'' Stress Generator can be the test system described in D.10 .

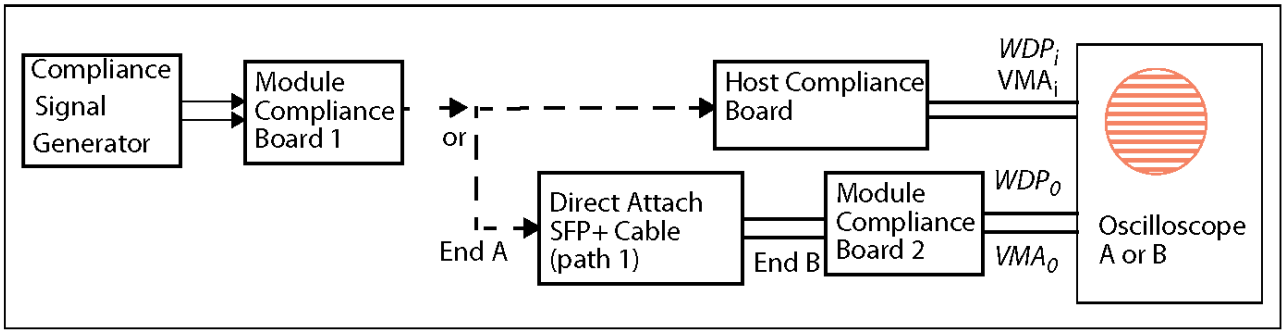


FIGURE 42 10GSFP+CU CABLE NEXT DWDP TEST SETUP

E.4.2 Cable dWDP Test Procedure

The measurement procedure for dWDP is described below:

- The compliance signal generator is set to the PRBS9.
- To improve measurement accuracy, uncorrelated jitter and noise should be reduced.
- Averaging should be used to further reduce instrumentation and measurement noise so their effect on the results are negligible.
- To calibrate WDPi per Table 26, refer to Figure 42. Plug a Host Compliance Board into the Module Compliance Board connected to the pattern generator. Adjust input rise and fall times to the target value as in Table 26. Adjust DDJ and DDPWS to obtain WDPi given by Table 26. Varying pre-emphasis as described in D.10 is an acceptable method.
- Unplug the Host Compliance Board and connect the cable assembly to the Module Compliance Board as shown in Figure 42. Measure WD Po.
- dWDP = WDPo - WDPi

E.4.3 Cable NEXT Measurement Procedure

Cable NEXT is measured based on the following procedure using the test setup shown in Figure 41:

- The Compliance Signal Generator should be calibrated via a Host Compliance Board inserted into the Module Compliance Board. The output of the Host Compliance Board is point B''.
- The Compliance Signal Generator amplitude and rise and fall times at B'' are calibrated to the crosstalk target values as defined in Table 26.
- The Compliance Signal Generator DDJ and DDPWS at B'' should meet or be less than the target specified in Table 11.
- The pattern for the Compliance Signal Generator is PRBS31.
- Module Compliance Board B outputs and inputs are terminated in 50 Ohms.
- NEXT is the RMS voltage measured by Oscilloscope A in a bandwidth of 12 GHz. Oscilloscope A should be free running (not triggered).
- The inherent Oscilloscope noise may be corrected by the RSS of Gaussian noise from the measured NEXT result.
- The far end Module Compliance Board outputs and input are termi-nated in to 50 Ohms.
- This measurement is then repeated for the other cable end.

E.4.4 VMA to Crosstalk Ratio (VCR)

Cable VMA loss (L) for cable path 1 can be measured using the test setup shown in Figure 42. VMA loss (L) for cable path 2 is measured by reversing cable end A with B.

$$L(dBe) = 20\log\left(\frac{VMA_i}{VMA_o}\right)$$

Where VMAi is the measured VMA at B'' and VMAo is measured at C'.

VMA/2 to crosstalk ratio (VCR) is the ratio of the transmitter minimum VMA at B'' Table 22 divided by the cable NEXT which already incorporates reflective FEXT. The factor 0.3 in the VCR equation (20*log10(VMAMIN/(2*NEXT*(1+C)))-L) accounts for SFP+ finite host return loss.

$$VCR(dBe) = VNR - L - K - 20\log 10(1 + C)$$

where

$$C = 0.3 \times 10^{\left(-\frac{2L}{20}\right)}$$

The procedure to measure NEXT is described in E.4.3.

$$VNR = 20\log 10\left[\frac{\frac{(NEXTaggressorVMA)}{2}}{NEXT}\right]$$

$$K(dBe) = 20\log 10\left(\frac{VMAmax}{VMAmin}\right) = 20\log 10\left(\frac{700}{300}\right) = 7.36$$

F. 1.25 GBd Operation Support (Optional)

F.1 Introduction

SFP+ host may be designed to operate at 1.25 GBd Ethernet rate using the classic SFP modules based on INF-8074i. Although IEEE Std 802.3, clauses 38 and 59 (1000BASE-SX, 1000BASE-LX and 1000BASE-LX10 PMDs) do not define the electrical levels for the module, INF-8074i specifies those levels which are reproduced here for reference Table 27.

Host transmitter output levels B and host receiver input tolerance levels at C are respectively given by Table 28 and Table 29 for SFP+ host operating at 1.25 GBd. Note: levels specified here may not be fully compliant with all classic SFP modules, but are expected to include a large percentage of existing 1.25 GBd classic modules. In order to be fully compliant to all classic SFP modules the max host receiver input tolerance level has to be 2000 mV, however this is not considered practical for modern 10 Gb/s SerDes.

TABLE 27 INF-8074I VOLTAGE LEVELS FOR REFERENCE ONLY

Parameters - B'	Symbol	Conditions	Min	Max	Units
SFP Module Input Differential at B'	Vin	*1	500	2400	mV (p-p)
SFP Module Output Differential at C'	Vout		370	2000	mV (p-p)
*1 INF-8074i recommends value between 500-1200 mV differential p-p be used for best EMI performance.					

F.2 SFP+ Host Operation Guideline For Supporting Classic SFP

SFP+ host must support TP1 and TP4 jitter specifications per IEEE CL 38.5 and CL 59.6 at point B and C respectively.

SFP+ host output pre-emphasis level may need to be adjusted for optimum output eye diagram for 1.25 GBd operation.

The module maximum input at B is given in Table 28 and is the same value as in INF-8074i. However, to provide compatibility with SFP+ hosts the module maximum output in Table 29 is much lower than the value specified in INF-8074i. An SFP module meeting the specifications of Table 30 will interoperate with SFP+ hosts.

TABLE 28 SFP+ HOST TRANSMITTER REQUIREMENTS TO SUPPORT 1.25 GBD MODE

Parameters - B	Symbol	Conditions	Min	Value	Units
Host Output VMA Differential	Vout		500		mV
Eye Mask	Y1	See D.2 and Figure 43		150	mV
Eye Mask	Y2			500	mV

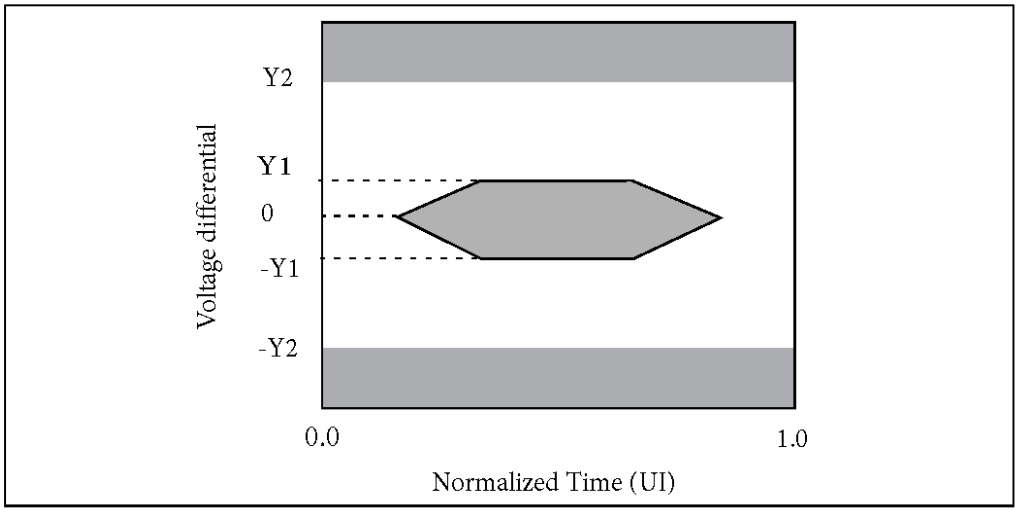


FIGURE 43 SFP+ HOST TRANSMITTER OUTPUT MASK FOR 1.25 GBD OPERATION

TABLE 29 SFP+ HOST RECEIVER REQUIREMENTS TO SUPPORT 1.25 GBD MODE

Parameters - B	Symbol	Conditions	Min	Value	Units
Host Input VMA Differential	Vout		370		mV
Eye Mask	Y1	See D.2 and Figure 44		125	mV
Eye Mask	Y2			600	mV

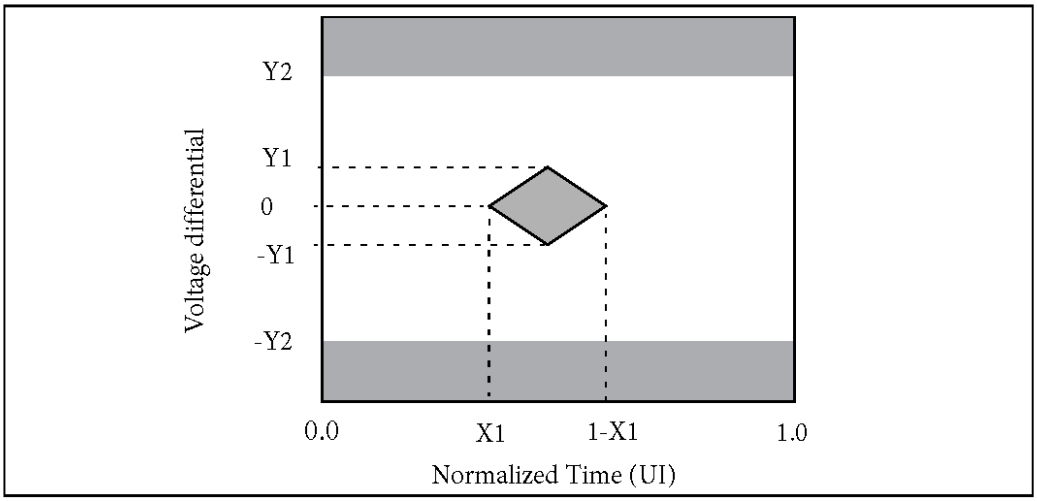


FIGURE 44 SFP+ HOST RECEIVER INPUT MASK FOR 1.25 GBD OPERATION

TABLE 30 SFP MODULE INPUT AND OUTPUT RANGES THAT CAN BE SUPPORTED BY THE SFP+ HOST

Parameters - Module	Symbol	Conditions	Min	Max	Units
SFP Module Input at B'	Vin		500 *1	2400 *1	mV (p-p)
SFP Module Output at C'	Vout		370 *1	1200	mV (p-p)
*1 Values are identical to the SFP classic INF-8074i specification.					

G. Matlab Code For TWDP

```
%%%%%%%%%%%%%%%%% MATLAB (R) Code for xWDP Computation %%%%%%%%%%%%%%%%%
%% SFF-8431 TWDP Code - PAlloc for Cu is now 14.0 dBe.
%% Based on original TWDP methodology described in IEEE Std 802.3aq(TM)-2006
%% Reference: N. L. Swenson, P. Voois, T. Lindsay, and S. Zeng, "Standards
%% compliance testing of optical transmitters using a software-based equalizing
%% reference receiver", paper NWC3, Optical Fiber Communication Conference and
%% Exposition and The National Fiber Optic Engineers Conference on CD-ROM
%% (Optical Society of America, Washin[gton, DC), Feb. 2007.
function [xWDP,MeasuredxMA]=SFF8431xWDP(WaveformFile,EqNf,EqNb,SymbolRate,Usage)
%% Example calling syntax:
%%   [xWDP,MeasuredxMA]=SFF8431xWDP('wavefile.txt',14,5,10.3125,'Optical_WDP')
%% The fields in the example given above should be replaced by the actual values
%% being used. WaveformFile should be the actual path\filename for each waveform
%% tested. The waveform consists of exactly N samples per unit interval T, where
%% N is the oversampling rate. The waveform must be circularly shifted to align
%% with the data sequence. The file format for the measured waveform is ASCII
%% with a single column of chronological numerical samples, in signal level,
%% with no headers or footers.
%% EqNf is the # of T/2-spaced feedforward equalizer taps; EqNb is the # of
%% T-spaced feedback equalizer taps.
%% SymbolRate is in gigabaud.
%% Options for Usage are 'Optical_WDP', 'Copper_WDP', and 'Copper_TWDP'.
%% 'Optical_WDP' is used in support of Section 3 for
%%    measuring WDPi at the output of an optical TP3 tester,
%%    measuring WDPo at C' of a linear optical module receiver, and
%%    calibrating WDP at C'' for testing a host that supports linear optical
%%    modules.
%% 'Copper_WDP' is used in support of Annex E for
%%    measuring WDPi and calibrating WDP at B'' for testing a copper cable
%%    assembly, measuring WDPo at C' of a copper cable assembly (C), and
%%    calibrating WDP at C'' for testing a host that supports copper cable
%% assemblies 'Copper_TWDP' is used for measuring TWDP at B of a host that
%% supports copper cable assemblies.

%% Transmit data file: The transmit data sequence is the 511 bit PRBS9 TWDP test
%% patterns defined in Table 686. The file format is ASCII with a single column
%% of chronological ones and zeros with no headers or footers.
TxDataFile = 'prbs9_950.txt';
%% Program constants %%
OverSampleRate = 16; % Oversampling rate, must be even
SymbolPeriod = 1/SymbolRate; % Symbol period is in ns
Q0 = 7.03; % BER = 10^(-12)
%% Load input waveform and data sequence, generate filter and other matrices
yout0 = load(WaveformFile);
XmitData = load(TxDataFile);
PtrnLength = length(XmitData);
TotLen = PtrnLength*OverSampleRate;
Fgrid = [-TotLen/2:TotLen/2-1].'/(PtrnLength*SymbolPeriod);
%% Compute response of 7.5 GHz 4th order Butterworth antialiasing filter
a = [1 123.1407 7581.811 273453.7 4931335]; % Denominator polynomial
b = 4931335; % Numerator for frequency response
ExpArg = -j*2*pi*Fgrid;
H_r = b./polyval(a,-ExpArg);
%% Get usage parameters for the application
[H_chan,Delays,PAlloc,dBscale] = GetParams(Usage,ExpArg);
N0 = SymbolPeriod/2 / (Q0 * 10^(PAlloc/dBscale))^2;
%% Set search range for equalizer delay, specified in symbol periods. Lower end
```

```
%% of range is minimum channel delay. Upper end of range is the sum of the
%% lengths of the FFE and channel. Round up and add 5 to account for the
%% antialiasing filter.
EqDelMin = floor(min(Delays)/SymbolPeriod);
EqDelMax = ceil(EqNf/2 + max(Delays)/SymbolPeriod);
ONE=ones(PtrnLength,1);
%% Normalize the received xMA (OMA or VMA) to 1. Estimate the xMA of the captured
%% waveform by using a linear fit to estimate a pulse response, synthesize a
%% square wave, and calculate the xMA of the synthesized square wave per IEEE
%% 802.3, clause 52.9.5.
ant=4; mem=40; % Anticipation and memory parameters for linear fit
X=zeros(ant+mem+1,PtrnLength); % Size data matrix for linear fit
Y=zeros(OverSampleRate,PtrnLength); % Size observation matrix for linear fit
for ind=1:ant+mem+1
    X(ind,:)=circshift(XmitData,ind-ant-1)'; % Wrap appropriately for lin fit
end
X=[X;ones(1,PtrnLength)]; % The all-ones row is included to compute the bias
for ind=1:OverSampleRate
    Y(ind,:)=yout0([0:PtrnLength-1]*OverSampleRate+ind)'; % Each column is 1 bit
end
Qmat=Y*X'*(X*X')^(-1); % Coefficient matrix resulting from linear fit. Each
%% column (except the last) is one bit period of the pulse response. The last
%% column is the bias.
SqWvPer=16; % Even number; sets the period of the sq wave used to compute xMA
SqWv=[zeros(SqWvPer/2,1);ones(SqWvPer/2,1)]; % One period of sq wave (column)
X=zeros(ant+mem+1,SqWvPer); % Size data matrix for synthesis
for ind=1:ant+mem+1
    X(ind,:)=circshift(SqWv,ind-ant-1)'; % Wrap appropriately for synthesis
end
X=[X;ones(1,SqWvPer)]; % Include the bias
Y=Qmat*X;Y=Y(:); % Synthesize the modulated square wave, put into one column
Y=AlignY(Y,SqWvPer,OverSampleRate);
avgpos=[0.4*SqWvPer/2*OverSampleRate:0.6*SqWvPer/2*OverSampleRate];
ZeroLevel=mean(Y(round(avgpos),:)); % Average over middle 20% of "zero" run
% Average over middle 20% of "one" run, compute xMA
MeasuredxMA=mean(Y(round(SqWvPer/2*OverSampleRate+avgpos),:))-ZeroLevel;
%% Subtract zero level and normalize xMA
yout0 = (yout0-ZeroLevel)/MeasuredxMA;
%% Compute the noise autocorrelation sequence at the output of the front-end
%% antialiasing filter and rate-2/T sampler.
Snn = N0/2 * fftshift(abs(H_r).^2) * 1/SymbolPeriod * OverSampleRate;
Rnn = real(ifft(Snn));
Corr = Rnn(1:OverSampleRate/2:end);
C = toeplitz(Corr(1:EqNf));
%% Compute the minimum slicer MSE and corresponding xWDP
X = toeplitz(XmitData, [XmitData(1); XmitData(end:-1:end+1-EqNb)]);
Xtil = toeplitz(circshift(XmitData,EqDelMin), ...
    XmitData(mod(-EqDelMin:-1:-(EqDelMax+EqNb),PtrnLength)+1));
Rxx = X'*X; % Used in MSE calculation
%% Propagate the waveform through channel.
yout = real(ifft(fft(yout0) .* fftshift(H_chan)));
%% Process signal through front-end antialiasing filter %%%%%%%%%%%%%%%%%%
yout = real(ifft(fft(yout) .* fftshift(H_r)));
%% Compute MMSE-DFE %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%% The MMSE-DFE filter coefficients computed below minimize mean-squared error
%% at the slicer input. The derivation follows from the fact that the slicer
%% input over the period of the data sequence can be expressed as Z = (R+N)*W -
%% X*[0 B]', where R and N are Toeplitz matrices constructed from the signal and
%% noise components, respectively, at the sampled output of the antialiasing
```

```
%% filter, W is the feedforward filter, X is a Toeplitz matrix constructed from
%% the input data sequence, and B is the feedback filter. The computed W and B
%% minimize the mean square error between the input to the slicer and the
%% transmitted sequence due to residual ISI and Gaussian noise. Minimize MSE
%% over 2/T sampling phase and FFE delay and determine BER.
MseOpt = Inf;
for jj= [0:OverSampleRate-1]-OverSampleRate/2 % sampling phase
    %% Sample at rate 2/T with new phase (wrap around as required)
    yout_2overT = yout(mod([1:OverSampleRate/2:TotLen]+jj-1,TotLen)+1);
    Rout = toeplitz(yout_2overT, [yout_2overT(1); yout_2overT(end:-1:end-EqNf+2)]);
    R = Rout(1:2:end, :);
    RINV = inv([R'*R+PtrnLength*C R'*ONE;ONE'*R PtrnLength]);
    R=[R ONE]; % Add all-ones column to compute optimal offset
    Rxr = Xtil'*R; Px_r = Rxr*RINV*Rxr';
    %% Minimize MSE over equalizer delay
    for kk = 1:EqDelMax-EqDelMin+1
        SubRange = [kk:kk+EqNb];
        SubRange = mod(SubRange-1,PtrnLength)+1;
        P = Rxx - Px_r(SubRange,SubRange);
        P00 = P(1,1); P01 = P(1,2:end); P11 = P(2:end,2:end);
        Mse = P00 - P01*inv(P11)*P01';
        if (Mse<MseOpt)
            MseOpt = Mse;
            B = -inv(P11)*P01'; % Feedback filter
            XSel = Xtil(:,SubRange);
            W = RINV*R'*XSel*[1;B]; % Feedforward filter
            Z = R*W - XSel*[0;B]; % Input to slicer
            %% Compute BER using semi-analytic method %%%%%%%%%%%%%%%%%%
            MseGaussian = W(1:end-1)'*C*W(1:end-1);
            Ber = mean(0.5*erfc((abs(Z-0.5)/sqrt(MseGaussian))/sqrt(2)));
        end
    end
end
%% Compute equivalent SNR %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%% This function computes the inverse of the Gaussian error probability
%% function. The built-in function erfcinv() is not sensitive enough for low
%% probability of error cases.
if Ber>10^(-12) Q = sqrt(2)*erfinv(1-2*Ber);
elseif Ber>10^(-323) Q = 2.1143*(-1.0658-log10(Ber)).^0.5024;
else Q = inf;
end
%% Compute penalty %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
RefSNR = dBscale * log10(Q0) + PAlloc;
xWDP = RefSNR-dBscale*log10(Q);
%% End of main function
%% GetParams subFunction
function [H_chan,Delays,PAlloc,dBscale] = GetParams(Usage,ExpArg);
    switch Usage
        case 'Optical_WDP' % Identity channel for optical
            Delays = 0;
            H_chan = 1;
            PAlloc = 6.5; % Total allocated dispersion penalty (dBo)
            dBscale = 10;
        case 'Copper_WDP' % Identity channel for copper
            Delays = 0;
            H_chan = 1;
            PAlloc = 14.0;% Total allocated dispersion penalty (dBe)
            dBscale = 20;
        case 'Copper_TWDP' % Cu TWDP stressor
```

```
            ChanResp = [...
                .0 .04849 .09697 .14546 .19394 .24243 .29091 .33940 .38788, ...
                .43637 .48485 .53334 .58182 .63031 .67879 .72728 .77576;
                .0175 .136 .2695 .1649 .0917 .0717 .0498 .0383 .0315, ...
                .027 .0216 .0202 .0174 .0146 .0123 .0094 .0066];
            Delays = ChanResp(1,:);
            PCoefs = ChanResp(2,:)';
            H_chan = exp(ExpArg*Delays)*PCoefs/sum(PCoefs); %With normalization
            PAlloc = 14.0;% Total allocated dispersion penalty (dBe)
            dBscale = 20;
    end
%% End of GetParams function
%% AlignY subFunction
function Y = AlignY(Y0,SqWvPer,OverSampleRate)
    % Aligns the mid crossing of the xMA square waveform to its ideal position.
    Y = Y0-mean(Y0); % AC-couple so crossings are at 0.

    % Look only for the crossing in the middle by ignoring any within ~2 UI from
    % its beginning. Due to possible misalignment of the captured waveform, this
    % is the only crossing that is certain.
    x = find(sign(Y(2*OverSampleRate:end-1))~= ...
        sign(Y(2*OverSampleRate+1:end)),1)+2*OverSampleRate-1;
    % Find a more exact crossing point.
    xinterp = interp1([Y(x),Y(x+1)],[x,x+1],0);

    % Shift to create the aligned square waveform
    Y = circshift(Y0,SqWvPer/2*OverSampleRate-x); % Coarse shift.
    X = [1:length(Y)].'; Y = interp1(X,Y,X+xinterp-x,'spline'); % Fine shift.
%% End of AlignY function
```