SFF Committee

INF-8478i Specification for

OC48 DWDM Pluggable Transceiver

Rev 3.0 May 30 2003

Secretariat: SFF Committee

Abstract: This specification describes the OC48 DWDM Pluggable Transceiver. It was developed by the MSA (Multiple Source Agreement) group in which the following companies participated:

Agilent	NEC
Alcatel Optronics	OKI
Bookham Technology	Sumitomo/Excelight
JDSU	Triquint Optoelectronics
Mitsubishi	

POINTS OF CONTACT:

Dan Rausch
Technical Editor
Avago Technologies
350 West Trimble Rd
San Jose CA 95131

408-435-6689
dan.rausch@avagotech.com

I. Dal Allan
Chairman SFF Committee
14426 Black Walnut Court
Saratoga
CA 95070

408-867-6630
endlcom@acm.org

EXPRESSION OF SUPPORT BY MANUFACTURERS

The following member companies of the SFF Committee voted in favor of this industry specification.

The following member companies of the SFF Committee voted against this industry specification.

The following member companies of the SFF Committee voted to abstain on this industry specification.

SFF COMMITTEE

The SFF Committee is an industry group. The membership of the committee since its formation in August 1990 has included a mix of companies which are leaders across the industry.

When 2 1/2" diameter disk drives were introduced, there was no commonality on external dimensions e.g. physical size, mounting locations, connector type, connector location, between vendors.

The first use of these disk drives was in specific applications such as laptop portable computers and system integrators worked individually with vendors to develop the packaging. The result was wide diversity, and incompatibility.

The problems faced by integrators, device suppliers, and component suppliers led to the formation of the SFF Committee as an industry ad hoc group to address the marketing and engineering considerations of the emerging new technology.

During the development of the form factor definitions, other activities were suggested because participants in the SFF Committee faced more problems than the physical form factors of disk drives. In November 1992, the charter was expanded to address any issues of general interest and concern to the storage industry. The SFF Committee became a forum for resolving industry issues that are either not addressed by the standards process or need an immediate solution.

Those companies which have agreed to support a specification are identified in the first pages of each SFF Specification. Industry consensus is not an essential requirement to publish an SFF Specification because it is recognized that in an emerging product area, there is room for more than one approach. By making the documentation on competing proposals available, an integrator can examine the alternatives available and select the product that is felt to be most suitable.

SFF Committee meetings are held during T10 weeks (see www.t10.org), and Specific Subject Working Groups are held at the convenience of the participants. Material presented at SFF Committee meetings becomes public domain, and there are no restrictions on the open mailing of material presented at committee meetings.

Most of the specifications developed by the SFF Committee have either been incorporated into standards or adopted as standards by EIA (Electronic Industries Association), ANSI (American National Standards Institute) and IEC (International Electrotechnical Commission).

Suggestions for improvement of this specification will be welcome. They should be sent to the SFF Committee, 14426 Black Walnut Ct, Saratoga, CA 95070.

The complete list of SFF Specifications which have been completed or are currently being worked on by the SFF Committee can be found at:

ftp://ftp.seagate.com/sff/SFF-8000.TXT

If you wish to know more about the SFF Committee, the principles which guide the activities can be found at:

ftp://ftp.seagate.com/sff/SFF-8032.TXT

If you are interested in participating or wish to follow the activities of the SFF Committee, the signup for membership and/or documentation can be found at:

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or the following application can be submitted.

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SFF Committee
14426 Black Walnut Ct
Saratoga CA 95070

408-867-6630

endlcom@acm.org

Reference Document for DWDM

PLUGGABLE TRANSCEIVER Modules

This technical document has been created by the DWDM PLUGGABLE TRANSCEIVER MSA group. This document is offered to transceiver users, and suppliers as a basis for a technical agreement. However, it is not a warranted document, each transceiver supplier will have their own datasheet. If the transceiver user wishes to find a warranted document, they should consult the datasheet of the chosen transceiver supplier.

The MSA group reserves the rights at any time to add, amend or withdraw technical data contained in this document.

MSA Group Contacts

Agilent	**Mike Lawton**	mike_lawton@agilent.com
Alcatel Optronics	**Patrice Durand**	patrice.durand@alcatel.fr
Bookham Technology	**Luc Hunziker**	luc.hunziker@bookham.com
JDSU	**Keith Riffee**	keith.riffee@jdsu.com
Mitsubishi	**Junichiro Yamashita**	junichiro.yamashita@edg.mea.com
NEC	**Kanji Shuke**	shuke@ab.jp.nec.com
OKI	**Komei Yusa**	yusa780@oki.co.jp
Sumitomo/Excelight	**Kaz Tanida**	tanida@ppd.sei.co.jp
Triquint Optoelectronics	**Genji Tohmon**	gtohmon@tqs.com

Document Change History

Version	Date	Comments
Release 1	28 May, 2002	First Release
Release 2	09 Sep, 2002	Updates from latest MSA Technical Document meetings.
Release 3	30 May, 2003	Updates from latest MSA Technical Document meetings.

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1 REFERENCE DOCUMENTS

The following documents should be read in conjunction with this specification –

Telcordia GR-253	Synchronous Optical Network (SONET) Transport Systems: Common Generic Criteria
ITU-T G.957	Optical Interfaces For Equipment and Systems Relating To The Synchronous Digital Hierarchy
ITU-T G.692	Optical Interfaces For Multichannel Systems with Optical Amplifiers
GR-468 CORE	Generic Reliability Assurance Requirements for Optoelectronic Devices Used In Telecommunications Equipment
21CFR 1040.10	Laser Safety
IEC 60825-1	Safety Of Laser Products Part 1: Equipment Classification, Requirements and Users Guide
CENELEC EN50082-1	Electromagnetic Compatibility - Generic Immunity Standard Part 1: Residential, Commercial, and Light Industry
CENELEC EN50081-1	Electromagnetic Compatibility - Generic Emissions Standard Part 1: Residential, Commercial, and Light Industry
CENELEC EN50081-1	Electromagnetic Compatibility - Generic Emissions Standard Part 2: Industrial Environment
PHILIPS 9397-750-00954	The I2C Bus Specification
FCC Part 15	Conducted/Radiated EMI

2 GLOSSARY

ITU-T	International Telecommunication Union - Telecommunication
SDH	Synchronous Digital Hierarchy
SONET	Synchronous Optical Network
PRBS	Pseudo Random Binary Sequence
APD	Avalanche Photo-Diode
LVCMOS	Low Voltage Complimentary Metal Oxide Semiconductor
CML	Current Mode Logic
DWDM	Dense Wavelength Division Multiplex
TEC	Thermo-Electric Cooler
SFP	Small Form Pluggable
NRZ	Non-Return to Zero
CDR	Clock and Data Recovery

3 MANDATORY AND OPTIONAL FEATURES

Italics in tables of this document are used to signify optional features. Features shown in tables as **bold text** are absolute minimum requirements for being DWDM PLUGGABLE MSA compatible.

4 OVERVIEW

The OC48 DWDM PLUGGABLE Module is an advanced, highly integrated, long reach ITU & SONET transceiver, which converts optical signals to and from serial electrical signals. The module wavelength is compliant to the ITU DWDM 50/100GHz wavelength grid covering the C-band (L-Band wavelengths available refer to transceiver vendor datasheet). The module features very high functionality and feature integration, accessible via a two-wire serial (I2C) interface. Electrical connection is made through a 70-pin gold plated edge connector, and the optical interface is via receptacle connector(s). The mechanical outline of the module, and rail system design, enable front panel and in-board mountable modules with respect to the host card. The module operates from a single 3.3V supply.

The OC48 DWDM PLUGGABLE Transceiver has been developed to be a highly flexible platform upon which MSA vendors can build a variety of products for many different customer applications. Several examples of module features that can be implemented on this platform include:

- Operating data rates from 155Mb/s to 2.7Gb/s with an upgrade path to provide a 10Gb/s serial transceiver
- Fiber optic link lengths from 40km to 650km
- Wavelengths compliant to the ITU DWDM 50/100GHz grid covering the C band and/or L band
- Temperature or electrical tunability from two ITU channels up to the entire C or L band
- Decision threshold control of the receiver allowing increased sensitivity over amplified links
- An integrated Variable Optical Attenuator (VOA)
- Wide range of optical output power levels
- OC48 transceiver, transmitter-only, and receiver-only operation at LR-1, LR-2, CWDM, and DWDM
- Optional clock and data recovery at one or more data rates
- Receiver bandwidth adjustment to provide higher sensitivity at lower data rates
- Tone injection and detection

5 SIMPLIFIED BLOCK DIAGRAM

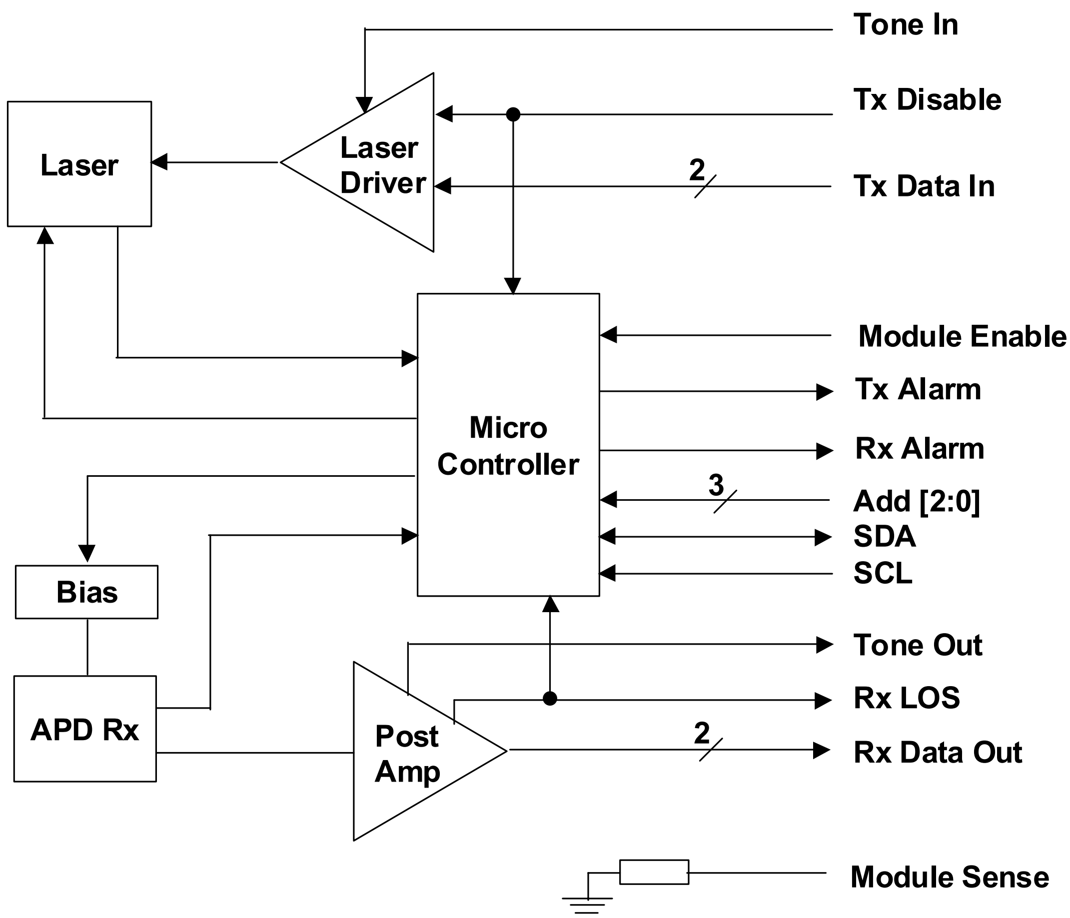


Figure 1 - Module Block Diagram

6 ELECTRICAL INTERFACES

6.1 SIGNAL DESCRIPTION

The electrical interfaces from the module to the host board are through a 70-way SFP type connector carrying all power supplies and signalling data for both transmit and receive paths.

Signal directions and types are defined relative to the module.

Signal Classification		I/O	Type	Description
Group	**Name**			
Data	**Tx Data (+ve)**[4]	**Input**	**CML**	**Tx data bit normal**
	Tx Data (-ve)[4]	**Input**	**CML**	**Tx data bit inverted**
Control	**Tx DISABLE**	**Input**	**LVTTL**[1]	**Laser disable [Internal pull-up]**
	TX ALARM	**Output**	**LVTTL**[2]	**Out of limits detected in Tx**
	TONE IN	*Input*	*Analogue*	*Low frequency tone*
Power	**Vcc (Tx)**	**Input**	**Supply**	**+3.3V supply for transmitter**
	Vcc (TEC)	**Input**	**Supply**	**+3.3V supply for TEC**
	GND (TEC)	**Output**	**Supply**[3]	**Ground for TEC**
	GND (Tx)	**Output**	**Supply**[3]	**Ground for Transmitter**
Clock	*Tx CLK (+ve)*[4]	*Input*	*CML*	*Reference clock normal*
	Tx CLK (-ve)[4]	*Input*	*CML*	*Reference clock inverted*

1. Interfaces to LVCMOS. Active high to disable.
2. Interfaces to LVCMOS. Active high to indicate out of limits detected.
3. Ground to be DC isolated between signal and module housing
4. The Tx Data & Tx CLK signals are AC coupled and have internal 50 Ohm termination.

Table 1 - Transmitter Signal Description

Signal Classification		I/O	Type	Description
Group	**Name**			
Data	**Rx Data (+ve)[4]**	**Out**	**Analogue or CML**	**Rx data bit normal**
	Rx Data (-ve)[4]	**Out**	**Analogue or CML**	**Rx data bit inverted**
Control	**Rx ALARM**	**Out**	**LVTTL[1]**	**Out of limits detected in Rx**
	Rx LOS	**Out**	**LVTTL[2]**	**Receiver received signal below limits**
	Tone Out	*Out*	*Analogue*	*Low frequency tone*
Power	**Vcc (Rx)**	**In**	**Supply**	**+3.3V supply for Receiver**
	Vcc (Rx Bias)	**In**	**Supply**	**+3.3V supply for APD**
	GND (Rx)	**Out**	**Supply[3]**	**Ground for Receiver**
	GND (Rx Bias)	**Out**	**Supply[3]**	**Ground for Receiver**
Clocks	*Rx CLK (+ve)[4]*	*Out*	*CML*	*Rx recovered clock normal (CDR variant only)*
	Rx CLK (-ve)[4]	*Out*	*CML*	*Rx recovered clock inverted (CDR variant only)*

1. Interfaces to LVCMOS. Active high to indicate out of limits detected in Rx
2. Interfaces to LVCMOS. Active high to indicate loss of received signal detected.
3. Ground to be DC isolated between signal and module housing
4. The Rx Data & Rx CLK signals are AC coupled and have internal 50 Ohm termination.

Table 2 - Receiver Signal Description

Signal Classification		I/O	Type	Description
Group	Name			
Power	Vcc (Digital)	In	Supply	+3.3V supply for control circuitry
	GND (Digital)	Out	Supply[1]	Digital Ground
Control	SDA	Input / Output	Open Collector	Serial data [External pull-up]
	SCL	Input	Open Collector	Serial clock [External pull-up]
	SLA-AD0:2	Input	LVTTL[2]	Module address [Internal Pull-up]
	MODULE SENSE	Input	Analogue	1KΩ to GND to indicate module is present
	MODULE ENABLE	Input	LVTTL[2]	Module Control [Internal Pull-down] Moves Module from standby mode, where the Tx and Rx are disabled, and the microcontroller is enabled.

1. Ground to be DC isolated between signal and module housing
2. Interfaces to LVCMOS.

Table 3 - Control Signal Description

6.2 INPUT / OUTPUT OPERATING PARAMETERS

Parameter	Symbol	Min	Max	Unit
DATA				
Operating Rate[1]		0.155	2.7	Gbps
Differential input voltage	Vin_{diff}	400	1000	mVpk-pk
Differential output voltage[2]	$Vout_{diff}$	200/400	1000	mVpk-pk
Differential input impedance	Rin	84	116	Ω
Rx data Output rise time[3]			250	ps
Rx data Output fall time[3]			250	ps
TWO WIRE INTERFACE[4] (SDA / SCL)				
Bus Frequency	f_{max}		100	kHz
MODULATION TONE				
Input Voltage[5]	V_{Tin}	*0*	*2.5*	*Vpk-pk*
Output Voltage	V_{Tout}	*0*	*2.5*	*Vpk-pk*
Bandwidth[6]		*50*	*500*	*kHz*
TX DISABLE				
Input Voltage Low	Vil		0.8	V
Input Voltage High	Vih	2.4		V
Disable time			50	ms
Start up time - controlled[7]			120	s
Disabled power			-40	dBm
TX ALARM				
Output Voltage Low	Vol		0.8	V
Output Voltage High	Voh	2.4		V
Activation Time[8]		500	1000	ms
De-Activation Time[9]		500	1000	ms

RX ALARM				
Output Voltage Low	**Vol**		**0.8**	**V**
Output Voltage High	**Voh**	**2.4**		**V**
Activation Time[8]		**500**	**1000**	**ms**
De-Activation Time[9]		**500**	**1000**	**ms**
RX LOS ALARM				
Output Voltage Low	**Vol**		**0.8**	**V**
Output Voltage High	**Voh**	**2.4**		**V**
Activation Time		**2.3**	**100**	**µs**
De-Activation Time			**100**	**µs**
Activation/Deactivation power		**-45**	**-35**	**dBm**
Hysteresis		**0.5**	**4**	**dB**
MODULE SENSE				
Resistor	**Rsense**	**900**	**1100**	**Ω**
MODULE ENABLE				
Input Voltage Low	**Vil**		**0.8**	**V**
Input Voltage High	**Vih**	**2.4**		**V**
Deassert time			**50**	**ms**
Assert Time[7]			**120**	**S**

1. ITU-T / SONET compliance is at 2.488Gbps.
2. Differential output voltage relates to the output in AGC or limiting mode (200mV analogue / 400mV CML)
3. 20-80% measured.
4. Refer to 'The I2C Bus Specification'.
5. For a constant tone input voltage, modulation depth is determined by the internal gain setting, and will vary between modules.
6. -3dB Bandwidths
7. Maximum time taken for module to ramp-up and stabilise power, extinction ratio & wavelength, from power up / tx enable state over supply/temperature extremes.
8. Activation time includes hold-off period
9. De-Activation time includes hold-on period

Table 4 - Input / Output Electrical Specification

6.3 CONTROL AND MONITORING FUNCTIONS

The module has the following control and monitor functions:

Tx Disable	
0	**Normal operation**
1	**Laser disabled – default state [internal 100K pull up]**
Tx Alarm	
0	**Normal operation**
1	**Out of limits detected in Tx circuit [internal 100K pull up]**
Rx Alarm	
0	**Normal operation**
1	**Out of limits detected in Rx circuit [internal 100K pull up]**
Rx LOS	
0	**Normal operation**
1	**Received signal input below threshold**
Module Enable	
0	**Module Standby Default State [internal 100K pull down]**
1	**Normal Operation**

Table 5 - Control and Monitoring Truth Table

7 WAVELENGTH

The available wavelengths are based on the ITU-T G.692 grid from 1528.77nm to 1563.86nm with 50GHz spacing. For available wavelengths in the L-band refer to transceiver vendor datasheets.

Nominal Centre Wavelength (nm)	Optical Frequency THz	Nominal Centre Wavelength (nm)	Optical Frequency THz
1528.77	196.10	1546.52	193.85
1529.16	196.05	1546.92	193.80
1529.55	196.00	1547.32	193.75
1529.94	195.95	1547.72	193.70
1530.33	195.90	1548.11	193.65
1530.72	195.85	1548.51	193.60
1531.12	195.80	1548.91	193.55
1531.51	195.75	1549.32	193.50
1531.90	195.70	1549.72	193.45

Nominal Centre Wavelength (nm)	Optical Frequency THz	Nominal Centre Wavelength (nm)	Optical Frequency THz
1532.29	195.65	1550.12	193.40
1532.68	195.60	1550.52	193.35
1533.07	195.55	1550.92	193.30
1533.47	195.50	1551.32	193.25
1533.86	195.45	1551.72	193.20
1534.25	195.40	1552.12	193.15
1534.64	195.35	1552.52	193.10
1535.04	195.30	1552.93	193.05
1535.43	195.25	1553.33	193.00
1535.82	195.20	1553.73	192.95
1536.22	195.15	1554.13	192.90
1536.61	195.10	1554.54	192.85
1537.00	195.05	1554.94	192.80
1537.40	195.00	1555.34	192.75
1537.79	194.95	1555.75	192.70
1538.19	194.90	1556.15	192.65
1538.58	194.85	1556.55	192.60
1538.98	194.80	1556.96	192.55
1539.37	194.75	1557.36	192.50
1539.77	194.70	1557.77	192.45
1540.16	194.65	1558.17	192.40
1540.56	194.60	1558.58	192.35
1540.95	194.55	1558.98	192.30
1541.35	194.50	1559.39	192.25
1541.75	194.45	1559.79	192.20
1542.14	194.40	1560.20	192.15
1542.54	194.35	1560.61	192.10
1542.94	194.30	1561.01	192.05
1543.33	194.25	1561.42	192.00
1543.73	194.20	1561.83	191.95
1544.13	194.15	1562.23	191.90
1544.53	194.10	1562.64	191.85
1544.92	194.05	1563.05	191.80
1545.32	194.00	1563.45	191.75
1545.72	193.95	1563.86	191.70
1546.12	193.90		

Note: Non-shaded boxes identify nominal wavelengths on 100G grid.

Note: The listed wavelengths are optional and vendors will list available wavelengths on their datasheet.

Table 6 - Available Wavelengths

8 TWO-WIRE INTERFACE FORMAT

All Two-Wire Interface commands are a mandatory requirement.

8.1 ELECTRICAL INTERFACE

The physical layer of the interface shall comply with the Philips specification as defined in 'The Philips I2C Bus Specification' - see Section 1 of this document.

Points to note include:

a) The I2C mechanical interface will consist of 5 connections within the hot pluggable connector, consisting of the clock (SCL), data (SDA), and 3 address pins.

b) The bus, not the module, will provide the required pull-up resistors as per section 16.1 of The I2C-Bus Specification.

c) The bus shall operate in the 100kHz mode.

d) Address pins are of LVTTL type, positive logic.

e) The module's address shall be sampled once at power up. This address shall not change until the next power up.

f) Address lines have internal 100k pull-up resistors.

g) The module will always take the role of a slave and never a master.

8.2 ADDRESSING

The module uses standard 7-bit addressing. Addressing is controlled by means of hardware settings on the customer board, by use of DIP switches or hard-wired links. The format consists of the first four bits of the address byte set as 0110 and the next three bits of the address byte being used for the hardware setting. The Least Significant Bit (LSB) is used to signify whether a read or write operation is requested. This method will allow up to 8 transceiver modules per 2 wire interface bus.

The format is thus:

Fixed Address				Customer Address			Read/Write
T_3	T_2	T_1	T_0	A_2	A_1	A_0	R/nW

Where :

T_3, T_2, T_1, T_0 : Fixed portion of the address – currently 0110

A_2, A_1, A_0 : Portion of the address configured externally to the module by customer

R/nW: Read/nWrite Bit – '1' signifies Read operation, '0' signifies Write operation

8.3 COMMAND STRUCTURE

All commands are one byte long. Extra data may be sent or received depending on the command. The command byte is a pre-defined hexadecimal number – in the forthcoming tables it is usually titled 'CMD Number'.

8.3.1 Sending Data

To send a command to the module, first a start condition is asserted, followed by the address of the module, with the LSb (the R/nW bit) clear. If the address matches that of the module, the module will thus acknowledge on the next clock pulse, if the module is busy it will respond with a negative acknowledge (as described in Section 8.3.7). If no further data is to be sent, a stop condition must be asserted. If more data is to be sent, the module will acknowledge each byte until the stop condition is asserted.

8.3.2 Receiving Data

To receive data from the module, e.g. temperature, first a command must be sent. After the module has received the command a START is asserted and the module is addressed for read. The master can thus clock out the appropriate number of bytes from the module. If the module is busy it will respond with a negative acknowledge (as described in 8.3.7) The master must acknowledge the module for every byte received, apart from the last byte, which the master must not acknowledge and send a STOP command. It is very important that the master does NOT acknowledge the last byte, failure to do so can result in being unable to assert the stop condition if a low value has been set on the SDA line by the module.

8.3.3 Reading From And Writing To The Memory

The module will offer a minimum of 32 bytes of customer read/write memory. Both the read and write functions will have their own command. An address byte is also included as part of the command structure, to indicate which location within the memory the data is being read from/written to.

8.3.4 Checksum Byte

To calculate the CHK value, the LSb of the address byte must be considered always as zero despite the value of the R/nW bit.

Master to Slave Checksum

The Master to Slave checksum is calculated by XORing all message bytes (except the last one, which is the checksum itself), starting from the Addr|W byte, to the DATAn byte. Note that no data may be sent, in which case only Addr|W and the CMD byte will form the checksum calculation. Prior to verifying the checksum value the Slave should check that the received command is a valid one (an optional command that is not implemented is not a valid command). In the event of an invalid command the slave will answer with an invalid command error and the checksum will not be performed.

Slave to Master Checksum

The Slave to Master Checksum is calculated by XOR-ing all message bytes (except the last one, which is the checksum itself), starting from the Addr|R byte, to the DATAn byte. Note that no data may be returned, in which case only Addr|R and the status byte will form the checksum calculation. (See section 8.3.5.)

8.3.5 Error / Status Byte

After each command is sent, the slave will prepare an answer to indicate the status of the command just received. This status byte will be included within the returned data stream where the command is one that requests data to be read, or to be returned as a single byte stream where the command does not require data to be read.

When the slave finds an error that causes a bit to be changed in the status byte, it should return a TYPE 6 response on receipt of a read enabled address from the master. The master will recognise that there has been an error by the condition of the status byte that it receives in the response and therefore only expect a TYPE 6 format message.

It is the responsibility of the customer to define how to deal with any errors indicated within the status byte – the command could be executed again, or the error simply ignored.

Status Code (Hex)	Description	Notes
00h	**OK**	**Command Executed**
01h	**Unknown Command**	**The command code is not supported.**
02h	**Reserved**	**Reserved for future use.**
03h	**Out of Range**	**At least one parameter of the command is out of range.**
04h	**Reserved**	**Reserved for future use.**
05h	**Check error**	**The command check byte is not consistent with the value indicated by the check byte.**
06h – 08h	**Reserved**	**Reserved for future use.**

09h	**Command not executed**	**The module is not able to execute according to current conditions.**
0Ah – FFh	**Reserved**	**Reserved for future use.**

Table 7 - Error / Status Byte

8.3.5.1 Command Structures

A = acknowledge (SDA low)
Ā = not acknowledge (SDA High)

TYPE 1
If the Master sends a command that requires n bytes of data to be returned:

Master:	START	Addr|W		CMD		CHK		STOP
Slave:			A		A		A	

The Slave will return on receipt of a Read Enabled Address (Addr|R) from the Master:

Master:	START	Addr|R			A		A		Ā	STOP
Slave:			A	STATUS		DATAn		CHK		

TYPE 2
If the Master sends a command that requires n bytes of data to be written to the Slave:

Master:	START	Addr|W		CMD		DATAn		CHK		STOP
Slave:			A		A		A		A	

The Slave will return the Status Byte only on receipt of an Addr|R from the Master:

Master:	START	Addr|R			A		Ā	STOP
Slave:			A	STATUS		CHK		

TYPE 3 {Not in current use. Provisioned for future use}
If the Master sends a command that requires n bytes of data to be written to the Slave and m bytes to be read back from the Slave:

Master:	START	Addr|W		CMD		DATA		CHK		STOP
Slave:			A		A		A		A	

The Slave will return on receipt of an Addr|R from the Master:

Master:	START	Addr|R			A		A		Ā	STOP
Slave:			A	STATUS		DATA		CHK		

TYPE 4
The TYPE 4 command is a specific implementation of a TYPE 2 command.
If the Master sends a command that requires a byte of data to be written to the Memory at Address X:

Master:	START	Addr|W		CMD		ADDR X		DATA		CHK		STOP
Slave:			A		A		A		A		A	

The Slave will return the Status Byte only on receipt of an Addr|R from the Master:

Master:	START	Addr|R			A		Ā	STOP
Slave:			A	STATUS		CHK		

TYPE 5
The TYPE 5 command is a specific implementation of a TYPE 1 command.
If the Master sends a command that requires a byte of data to be returned from the Memory at Address X:

Master:	START	Addr|W		CMD		ADDR X		CHK		STOP
Slave:			A		A		A		A	

The Slave will return the requested byte from Address X after a certain period of time:

Master:	START	Addr|R			A		A		Ā	STOP
Slave:			A	STATUS		DATA		CHK		

TYPE 6
If the Master sends a command only:

Master:	START	Addr|W		CMD		CHK		STOP
Slave:			A		A		A	

The Slave will return the Status Byte only on receipt of an Addr|R from the Master:

Master:	START	Addr|R			A		Ā	STOP
Slave:			A	STATUS		CHK		

8.3.6 Clock Stretching

After being addressed, or after every byte transferring from the host to the module, or before every byte transferring from the module to the host, the module will be permitted to hold the 'SCL' (clock from the master bus) line low whilst the on board processor readies data for either reception or transmission. The time for which the clock is held low (stretched) must not exceed 1ms.

8.3.7 Module Busy

If the module is performing a real-time task, and must not be interrupted, and the master sends an Addr|W (command), the module will send Ā. The master will thus send a STOP bit and then wait (minimum 10ms) before re-sending the message.

Master:	START	Addr|W		STOP
Slave:			Ā	

If the module is performing a real-time task, and must not be interrupted, and the master sends an Addr|R, the module will send Ā. The master will thus send a STOP bit and then wait (minimum 10ms) before re-sending the message.

If the module is preparing data to answer an Addr|W (command), but has not yet completed the task, and the master sends an Addr|R, the module will send Ā. The master will thus send a STOP bit and then wait (minimum 10ms) before re-sending the message.

Master:	START	Addr|R		STOP
Slave:			Ā	

9 COMMAND SET DETAILS

9.1 STATIC DATA

All static data is a mandatory requirement.

The static data stored in memory is listed in the table below. The TYPE 1 command structure is shown in section 8.3.5.1.

Command Name	CMD[1] Number	Parameter	Target	Bytes	Type
IND[2]	01h	Identifiers	Type of transceiver	1	1
ITU[3]	02h	Tuning Range	Number of ITU channels (ie 1 for fixed)	1	1
CON[4]	03h	Connector	Code for optical connector type	1	1
BRN	04h	Bit Rate, Nominal	Nominal bit rate, units of 100Mbps	1	1
LTH[A]	05h	Length	Link length supported for 9/125mm fibre, units of 10km	1	1

VEN[5]	06h	Vendor Name	Module Vendor Name (HEX)	1	1
PPN	07h	Vendor Part Number Leading character first	Product Part No. provided by module vendor (ASCII)	16	1
REV[B]	08h	Vendor Product Release LSB first	Revision level for part (HEX)	2	1
LWA[C]	09h	Wavelength LSB first	Laser Wavelength in tenths pm	4	1
SER	0Ah	Vendor Serial Number Leading character first	Serial number provided by vendor (ASCII)	16	1
DAT[D]	0Bh	Date code LSB first	Vendor's manufacturing date code	4	1
OPT	0Ch	Optional Features	Implemented Optional Features (See Section 9.2)	1	1
Reserved	0Dh - 10h	Reserved	Reserved for future static data	TBD	

1. CMD number is the actual data sent as the 'Command Byte'
2. Type of Transceiver

01h	Fixed, 100GHz spacing, 2.5Gbps	42h	OC-48 LR-1 SONET (1550nm)
02h	Fixed, 50GHz spacing, 2.5Gbps	51h	CWDM
11h	Fixed, 100GHz spacing, 10Gbps	61h	Tx only, fixed, 100Ghzspacing, 2.5Gbps
12h	Fixed, 50GHz spacing, 10Gbps	62h	Tx only, fixed, 50Ghzspacing, 2.5Gbps
21h	Tuneable, 100Ghz Spacing, 2.5Gbps	63h	Tx only, fixed, 100Ghz spacing, 10Gbps
22h	Tuneable, 50Ghz Spacing, 2.5Gbps	64h	Tx only, fixed 50GHz spacing, 10Gbps
31h	Tuneable, 100Ghz Spacing, 10Gbps	65h	Tx only, Tuneable, 100Ghzspacing, 2.5Gbps
32h	Tuneable, 50Ghz Spacing, 10Gbps	66h	Tx only, Tuneable, 50Ghzspacing, 2.5Gbps
41h	OC-48 LR-1 SONET (1310nm)	71h	Rx only

3. Tuning Range

   1 = fixed   n = n channels   (ie 8 = 8 channels)

4. Connector

   1 = Simplex LC   3 = Simplex MU

   2 = Duplex LC   4 = Duplex MU

5. Vendor

01 = Agilent Technologies	02 = Bookham Technology
03 = Triquint Optoelectronics	04 = Alcatel Optronics
05 = Mitsubishi Electric	06 = JDS Uniphase
07 = NEC	08 = OKI
09 = Sumitomo Electric	

A. LTH (Link Length in 10's km)

Format: one byte holding number of 10km units. No decimal encoding.

B. REV (Revision Level)

Format: two bytes representing Major and Minor revision numbers. Both types to use packed BCD, giving revision numbers from 00.00 to 99.99.

Byte order: Minor revision sent first

C. LWA (Wavelength in tenths pm)

Format: Four bytes holding wavelength in packed BCD format. Number left justified so MSB holds wavelength band.

Example: 1541.75

Hex:	15	41	75	00
Decimal:	21	65	117	00

Byte order: LSB (Units and tenths of pm) sent first.

D. DAT (Date of manufacture)

Format: Four bytes holding the Year, Month and Day in packed BCD format.

Example: 31st July 2002

Hex:	31	07	02	20
Decimal:	49	07	02	32

Byte order: Day sent first followed by month, year and century.

Table 8 - Static Data Command Set

9.2 OPTIONAL FEATURES

The OPT command (0Ch) is a TYPE 1 command, and will return the 1-byte status of the Transceiver Optional Features as below. The TYPE 1 command structure is shown in section 8.3.5.1. NOTE: Byte count does not include the command and checksum

The following table lists a proposal structure for the OPT byte. “1” means that the specific feature is implemented, “0” that is not implemented.

7	6	5	4	3	2	1	0
Reserved for future use			Tone input/ output	VOA	VDT	TUN	CDR

Table 9 - Optional Command Structure

9.3 DIAGNOSTIC MONITORING.

9.3.1 Live Data

All Live Data is a mandatory requirement.

The TYPE 1 command structure is shown in section 8.3.5.1.

Command Name	CMD Number	Parameter	Description	Bytes	Type
TEC	11h	Laser Temperature LSB and MSB LSB First	Signed 2’s complement integer temperature. Return in 16 bit value in 1/10ths of a degree (i.e. 345 = 34.5C)	2	1
TMP	12h	Module Temperature LSB and MSB LSB First	Signed 2’s complement integer temperature. Return in 16 bit value in 1/10ths of a degree (i.e. 345 = 34.5C)	2	1
BIA	13h	Laser Bias Current LSB and MSB LSB First	Return the laser bias current in mA. Result is returned as an unsigned 16 bit value in 1/10ths of a mA.	2	1
MOD	14h	Laser Mod Current LSB and MSB	Return the laser mod current in mA. Result is returned as an unsigned 16	2	1

		LSB First	bit value in 1/10ths of a mA.		
POT[1]	15h	TX Power LSB and MSB LSB First	Return measured TX output power in µW. Represented as an un-signed 16 bit integer in µW.	2	1
POR[1]	16h	RX Power LSB and MSB LSB First	Return measured RX input power in µW. Represented as an un-signed 16 bit integer in 1/10's of a µW.	2	1
APV	17h	APD Voltage supply LSB and MSB LSB First	Return measured APD supply voltage. Represented as an unsigned 16 bit integer in 1/10ths of a Volt	2	1
Reserved	18h - 1Ch	Reserved	Reserved for future live data	tbd	

1. The required resolution is not an indicator of the required accuracy

Table 10 - Live Data Command Set

9.3.2 Transceiver Status

The STA command (1Dh) is a TYPE 1 command, and will return the 1-byte status of the Transceiver as below. The TYPE 1 command structure is shown in section 8.3.5.1.

7	6	5	4	3	2	1	0
Laser Status	Alarm Triggered	Warning Triggered	Module Disabled	Vendor Specific Status Bits			

Bit Set = Flag Triggered

Bit Clear = Module OK, no Alarms or Warnings triggered

Table 11 - Status Command Structure

Laser Status is indicated by a 1 = Operating (presence of light), and 0 = Disabled (no light).

'Alarm Triggered' is flagged by any of the alarms in section 9.3.1, and 'Warning Triggered is flagged by any of the un-masked warnings in section 9.3.3.

Module disabled is the inverted logic value of the hardware pin 'Module Enable' and is used to indicate the module status Disabled/Enabled.

The vendor specific status bits will be defined through a vendor specific table.

9.4 ALARMS AND WARNINGS

Tx_ALARM (or Rx_ALARM) hardware pins are to be used as an interrupt if either the alarm or warning flags indicate an event occurred. The pins will also be asserted when Module Enable is de-asserted.

The customer will reset the alarms by sending the reset commands 'RST and/or RSR' – see Section 9.4:-Control Functions.

9.4.1 Alarms (All Alarms are a mandatory requirement)

Alarm flags indicate conditions likely to result (or have resulted) in module failure or out of specification operation and indicate cause for immediate investigation. These events are non-mask-able, and any alarm that occurs will result in TX and/or RX being shut down.

Command Name	CMD	Bit	Name	Description	Action	Type
ALA (1Byte)	1Eh	7	Module Temp High Alarm	Set when module temperature exceeds high alarm level	Shut down TX and RX	1
		6	Module Temp Low Alarm	Set when module temperature is below low alarm level	Shut down TX and RX	1
		5	Wavelength Maximum	Set when wavelength exceeds high alarm level	Shut down TX only	1
		4	Wavelength Minimum	Set when wavelength is below low alarm level	Shut down TX only	1
		3	Tx Power High Alarm	Set when Tx Output power exceeds high alarm level	Shut down TX only	1
		2	Tx Power Low Alarm	Set when Tx Output Power is below low alarm level	Shut down TX only	1
		1	APD Bias Voltage	Set when APD Voltage exceeds high Alarm level	Shut down RX only	1
		0[1]	Module Time Out	Set when the module does not reach full operating status within a set start-up time	Shut down TX only	1

1. Module time out is TX dependant failure during start-up, also asserting the TX Alarm. RX failure during start-up will assert the Rx Alarm only.

The TYPE 1 command structure is shown in section 8.3.5.1.

Table 12 - Alarm Flag Structure

9.4.2 Alarm Trip Points

The activation of an alarm will indicate to the user that a major malfunction or out of tolerance condition has occurred.

This condition will affect traffic through part of the module, could affect other channels or lead to damage to the module.

When an alarm is detected the module will shutdown itself (Tx and/or Rx in function of which alarm was detected) to prevent further damage and to prevent any possible impact to traffic on other channels. If a Module Temp High or Module Temp Low occur the module will be shut down (both Tx and Rx) and to reset the module the customer must send both RST and RSR.

During warm-up, specific alarm activation is disabled, with the exception of Module time-out, Module Temp High and Module Temp Low.

ALA 07	Module Temp High	TMPmax +5% of TMPmax - TMPmin
ALA 06	Module Temp Low	TMPmin -5% of TMPmax - TMPmin
ALA 05	Wavelength High	+ channel spacing/2
ALA 04	Wavelength Low	- channel spacing/2
ALA 03	Tx Power High	POTnom +50%
ALA 02	Tx Power Low	POTnom -50%
ALA 01	APD Voltage High	APVmax +15%
ALA 00	Start Up Time Out	Start-up Time (Controlled) + 10 seconds

Note:- The values in this table are for guidance purposes only. The vendor determines alarm level trip points.

Table 13 - Normalised Alarm Activation Levels

9.4.3 Warnings (All Warnings are a mandatory requirement)

Warning flags generally can be used to indicate end of life conditions (such as for higher than expected bias currents in a constant power control loop). These events will assert the relevant hardware alarm, but are mask-able pending host controller intervention. Masking will de-assert the relevant hardware alarm. If the reason for the warning goes away, the warning should be de-asserted automatically at both hardware and software levels, without the host having to mask the warning. The warning masks are set at 1 (all enabled) by default. The default value will be loaded when a TX or RX reset command occurs.

Command Name	CMD	Bit	Name	Description	Type
WAA	1Fh	7	**LD Current Warning High**	**Set when Ibias or Imod exceeds max warning level**	1
		6	**Module Temp High Warning**	**Set when module temp exceeds max warning level**	1
		5	**Module Temp Low Warning**	**Set when module temp exceeds min warning level**	1
		4	**TEC Current warning maximum**	**Set when TEC Current exceeds max warning level**	1
		3	**Rx Optical Power High Warning**	**Set when Received Power exceeds high warning level**	1
		2	**LOS**	**Loss Of Signal**	1
		1	*LOL*	*Loss Of Lock (CDR Variant Only)*	*1*
		0	**Wavelength Warning**	Set when wavelength drift exceeds vendor specific limit	1

The TYPE 1 command structure is shown in section 8.3.5.1.

Table 14 - Warning Flag Structure

Command Name	CMD	Function	Bytes	Type
MAS	**20h**	**Sets the Masking byte for the warnings. The masking byte will be ANDed with the warning byte to define which warning will trigger Tx_ALARM or Rx_ALARM. Mask corresponds to the bit numbers in command WAA. Use 1 to define warning triggered, 0 to define warning ignored.**	**1**	**2**
MAR	**21h**	**Reads the Masking byte for warnings**	**1**	**1**

TYPE 1 and TYPE 2 command structures are shown in section 8.3.5.1.

Table 15 - Warning Flag Masking byte

9.4.4 Warning Trip Points

The activation of a warning will indicate to the user that the module is approaching an out of range condition on a parameter(s).

Should this out of range actually occur, an Alarm condition may result, traffic may be affected or the module will fail to meet its performance requirements.

A warning condition will not affect the modules ability to meet its performance requirements and can be software masked.

WAA 07	LD Current High	>= BIAmax - 25% or MODset +20%
WAA 06	Module Temp High	>= TMPmax - 5% of TMPmax-TMPmin
WAA 05	Module Temp Low	<= TMPmin +5% of TMPmax-TMPmin
WAA 04	TEC Current High	>= Itecmax -5%
WAA 03	Rx Power High	>= PORmax -5%
WAA 02	Loss Of Signal	Loss Of Signal
WAA 01	*Loss Of Lock (CDR variant only)*	Loss of CDR Lock
WAA 00	Wavelength Warning	>< Normal wavelength Range

Note:- The values in this table are for guidance purposes only. The vendor determines warning level trip points.

Table 16 - Normalised Warnings

9.5 CONTROL FUNCTIONS

These commands perform basic control functions required during set up of the module by the customer. TYPE 1, TYPE 2, and TYPE 6 command structures are shown in section 8.3.5.1.

Command Name	CMD Number	Parameter	Function	Operand	Bytes	Type
CHN[4]	**22h**	**Set Operating State**	**Sets the current operating channel, or disables optical output**	**00h = Transmitter Disabled** **01h = Channel 1**	**1**	**2**
CHR[5]	**23h**	**Read Operating state**	**Reads the current operating channel set by CHN**	**Command Only**	**1**	**1**
DEF[8]	**24h**	**Set Default Power On State**	**Sets the default power on state of the module**	**00h = Transmitter Disabled** **01h = Channel 1**	**1**	**2**
DER[5]	**25h**	**Read Default Power On State**	**Reads the default power on state of the module**	**Command Only**	**1**	**1**
TUN[3]	*26h*	*Set Wavelength Fine Adjustment State*	*Set Fine adjustment of wavelength*	*Signed 2's complement digital number.*	*1*	*2*
TUR[5]	*27h*	*Read Wavelength Fine Adjustment State*	*Reads Fine adjustment of wavelength*	*Command Only*	*1*	*1*
SOP[8]	*28h*	*Store Wavelength Operating Point*	*Store new wavelength operating point*	*Command Only*	*0*	*6*
RST[1]	**29h**	**Resets TX**	**Resets TX**	**Command Only**	**0**	**6**
RSR[2]	**2Ah**	**Resets RX**	**Resets RX**	**Command Only**	**0**	**6**
ROP[5]	*2Bh*	*Read Stored Wavelength Operating Point*	*Reads wavelength operating point*	*Command Only*	*1*	*1*
VTH[4,9]	*2Ch*	*Set Variable Threshold*	*Sets Variable Threshold Level*	*Signed Number*	*2*	*2*

RTH[5]	*2Dh*	*Read Variable Threshold*	*Reads Variable Threshold point*	*Signed Number*	*2*	*1*
STH[6]	*2Eh*	*Store Current Threshold Value*	*Stores Current Threshold Value*	*Command Only*	*0*	*6*
RTHNV[5]	*2Fh*	*Read stored Threshold value*	*Reads stored Threshold value*	*Signed Number*	*2*	*1*
RTHEN[7]	*30h*	*Enable / Disable Variable Threshold*	*Enables / Disables Variable Threshold*	*Unsigned Byte*	*1*	*2*
VOA[4]	*31h*	*Set Variable Optical Attenuation*	*Sets Optical Attenuation adjustment*	*Unsigned Number*	*2*	*2*
ROA[5]	*32h*	*Read Optical Attenuation Adjust*	*Reads Optical Attenuation adjustment*	*Unsigned Number*	*2*	*1*
SOA[8]	*33h*	*Store Current Optical Attenuation value*	*Stores Current Optical Attenuation value*	*Command Only*	*0*	*6*
ROANV[5]	*34h*	*Read Stored Optical Attenuation value*	*Reads Stored Optical Attenuation value*	*Unsigned Number*	*2*	*1*
Reserved	**35h-3Fh**	**Reserved**	**Reserved for future control functions**	**Reserved**	**TBD**	**TBD**
Reserved	**60h-**	**Reserved**	**Reserved for factory calibration**	**Factory Use**	**TBD**	**TBD**

1. Clears hardware Tx Alarm, restores defaults using last wavelength stored via the SOP command, restores warning mask default and restarts transmitter.
2. Clears hardware Rx Alarm, restores defaults, restores warning mask default and restarts receiver.
3. The TUN command allows the wavelength to be increased or decreased. The actual wavelength change will be module and supplier specific.
4. The value is used and stored in volatile memory
5. The value is used and read from volatile memory
6. The value is stored in non-volatile memory. This value is loaded from non-volatile memory on power up or when a RSR command occurs.
7. Value of 0 disables Variable Threshold. Module powers up in nominal threshold (50%) state. The value set through the Threshold Commands has no effect on the crossing voltage until enabled.
8. The value is stored in non-volatile memory. This value is loaded from non-volatile memory on power up or when a RST command occurs
9. A threshold value of zero indicates that the crossing is at the factory default setting. Threshold values less / greater than zero shift the threshold voltage down / up.

Table 17 - Control Functions Structure

9.6 CUSTOMER FUNCTIONS

At least 32 bytes of memory have been reserved for customer requirements.

The customer will be able to write to and read from the reserved area of the non-volatile memory for customer use on a byte by byte basis

Command	CMD Number	Parameter	Data	Size	Type
WRI[1]	40h	Customer Memory Write	Customer can write data to the memory locations reserved for customer use.	1 byte at a time	4
REA[2]	41h	Customer Memory Read	Customer can read data from the memory locations reserved for customer use.	1 byte at a time	5
Reserved	42h - 4Fh	Reserved	Reserved for future customer functions	TBD	TBD

1. A TYPE 4 command structure (see section 8.3.5.1) is utilised in order to allow single byte writes to the reserved area of the memory for customer use.
2. A TYPE 5 command structure (see section 8.3.5.1) is utilised in order to allow single byte reads from the reserved area of the memory for customer use.

Table 18 - Customer Memory Functions

10 TONE INPUT/OUTPUT (TONE INPUT/OUTPUT IS AN OPTIONAL FUNCTION)

The modulation input allows amplitude modulation of the "1"s level in the frequency range of 50 - 500 KHz. This input must be driven from a 50 Ohm source, and is AC coupled internally. Do not exceed the maximum drive level, over driving this input can cause waveform distortion. If unused this input should be connected to 0V to prevent noise pickup. The output is AC coupled and dependant on received power and modulation depth.

11 POWER SUPPLY REQUIREMENTS

The module requires a single supply of +3.3V ± 5%.

Parameter	Min	Nom	Max	Units
Vcc Supply	3.135	3.3	3.465	V
Power Consumption			7	W

1. Maximum continuous current is limited by the connector rating.

Table 19 - Power Supply Requirements

Supply Rail	Max	Units	Conditions
Vcc Supply Noise	50	mVpp	6kHz – 1MHz

Table 20 - Power Supply Noise Requirements

11.1 HOT SWAP AND POWER-ON-RESET

When a hot pluggable Transceiver is inserted the peak in-rush currents to any supply rail shall be limited by the host power supply. The host will maintain a constant maximum current and not foldback. The module will not attempt to start operating or require TEC current until the supply voltage has reached the minimum operating voltage. The module must exit the Power On Reset condition at a voltage in the V_{INIT} range.

Parameter	Symbol	Min	Max	Units
Module Initialisation Voltage	V_{INIT}	2.5	3.0	V

Module user to ensure that the maximum current rating of the connector is not exceeded

Table 21 - Module Initialisation Voltage

When Module Enable is held low, the Tx and Rx elements of the module will be disabled and the Tx and Rx Alarm pins will be asserted. The micro-controller must always be enabled to allow it to be interrogated by the host. The module will not enter the enabled state until Module Enable is taken high.

12 MECHANICAL DESCRIPTION

12.1 PHYSICAL ARRANGEMENT (FRONT PANEL MOUNT)

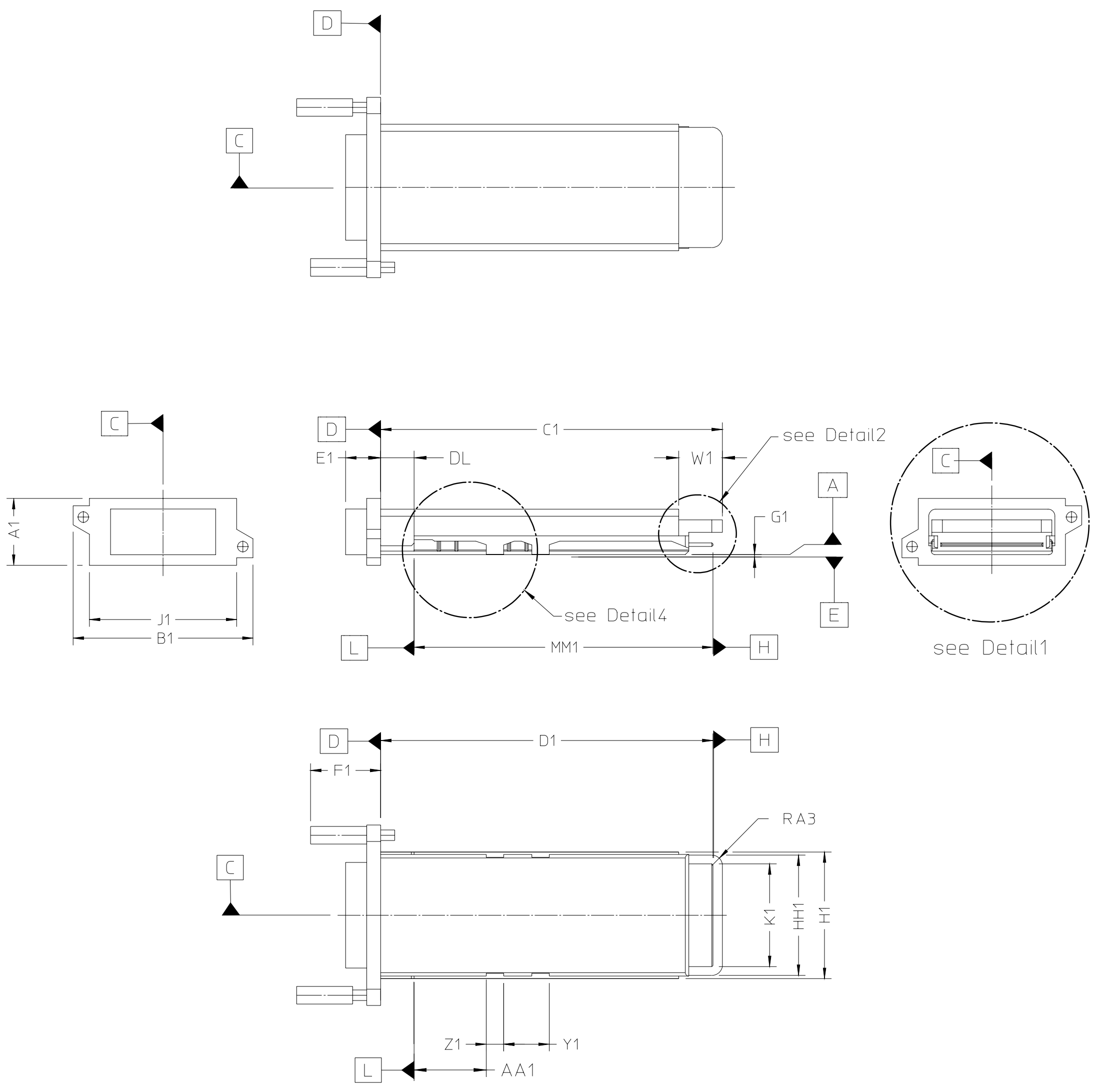


Figure 2 - Mechanical Outline (Faceplate Mount)

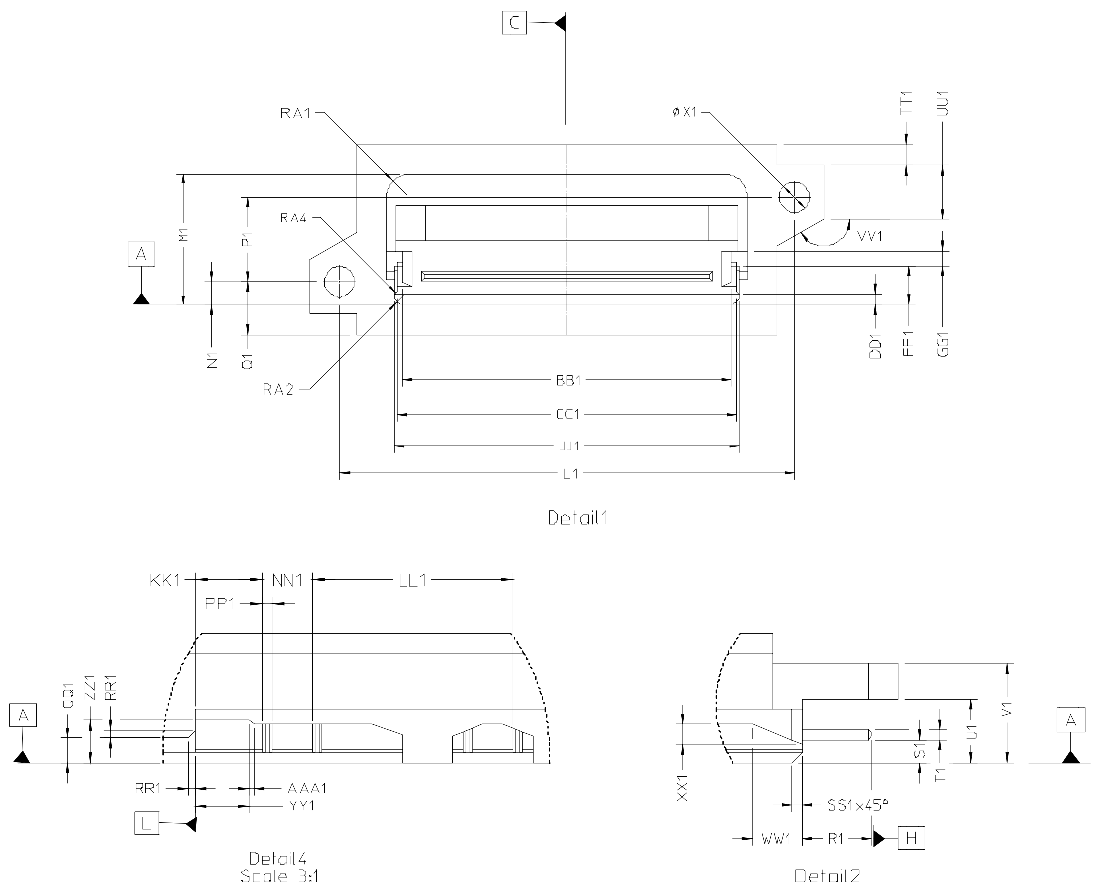


Figure 3 - Mechanical Outline - Details

KEY	VALUE (mm)	TOLERANCE (mm)	COMMENT
A1	19.0	+/- 0.1	Height of bezel overall
B1	51.3	+/- 0.2	Width of bezel overall
C1	97.5	REF	Length of transceiver body from datum D to end of rear shoulder
D1	94.8	+/- 0.3	Datum D to datum H
DL	9.5	+/- 0.3	Datum D to datum L
E1	10.0	Max	Datum D to front of module body, in-board as well as front-panel mount options
F1	20.0	Max	Datum D to end of captive thumb screws
G1	0.5	N/A	Vertical stand-off of transceiver body from host circuit card
H1	36.0	+/- 0.15	Width of transceiver body, overall width of in-board mount transceiver
J1	42.0	+/- 0.2	Width of bezel without side flanges
K1	29.2	Ref.	Width of transceiver circuit card
L1	45.5	+/- 0.2	Distance between holes for captive thumb screw centres in 'X' axis
M1	12.9	+0.0 - 0.3	Height of transceiver body, overall height of in-board mount transceiver
N1	2.25	+/- 0.3	Vertical distance from datum A to bottom hole for captive thumb screw centre
P1	8.4	+/- 0.1	Vertical distance between holes for captive thumb screw centres
Q1	5.3	+/- 0.1	Vertical distance from bottom of bezel to hole for captive screw
R1	6.9	+/- 0.2	Datum H to end of recess for electrical edge connector
S1	2.3	+/- 0.15	Datum A to bottom of transceiver PCB
T1	1.0	Ref.	Transceiver PCB thickness
U1	6.3	Min	Datum A to underside of rear shoulder
V1	9.85	+/- 0.2	Height of rear shoulder from Datum A
W1	12.5	Min	Length of rear shoulder
X1	N/A	N/A	Holes for M3 captive thumb screws
Y1	13.0	+/- 0.2	Pitch of vertical slots for plugging
Z1	5.0	+/- 0.2	Width of vertical slots for plugging
AA1	20.6	+/- 0.2	Datum L to first vertical slot for plugging
BB1	33.0	+/- 0.2	Width of module slot to accommodate rail
CC1	34.0	+/- 0.2	Width of module slot to accommodate location features on rail
DD1	1.0	+/- 0.15	Datum A to base of module slot to accommodate location features on rail
FF1	3.8	+/- 0.15	Datum A to base of module slot to accommodate rail
GG1	1.5	+/- 0.2	Height of module slot to accommodate rail

HH1	34.2	+/- 0.2	Width of PCB rear shoulder
JJ1	34.6	+/- 0.2	Outer width of module slot to accommodate rail
KK1	6.6	+/- 0.2	Datum L to first rail location feature
LL1	20.0	+/- 0.2	Pitch of rail location features
MM1	85.3	+/- 0.2	Datum H to Datum L
NN1	5.0	+/- 0.2	Pitch of rail location features
PP1	1.0	+/- 0.2	Width of rail location features
QQ1	2.5	+/- 0.15	Datum A to bottom of hard stop
RR1	0.75	+/- 0.1	Depth of chamfer on hard stop
SS1	1.0	+/- 0.1	Size of chamfer on bottom corner of module adjacent to electrical connector
TT1	2.1	+/- 0.2	Top of side flange to top of bezel
UU1	5.4	+/- 0.2	Outer height of side flange
VV1	150°	+/- 1°	Angle of chamfer on side flange
WW1	5.0	+/- 0.5	Length of chamfer into slot for rail
XX1	2.0	+/- 0.5	Height of chamfer into slot for rail
YY1	5.25	+/- 0.1	Datum L to chamfer on vertical location feature
ZZ1	4.2	+/- 0.1	Datum A to vertical location feature
AAA1	0.6	+/- 0.1	Depth of chamfer on vertical location feature
RA1	2.0	Min	External radius or chamfer on transceiver lid
RA2	1.0	Min	External radius or chamfer on transceiver base
RA3	3.0	+/- 0.5	External radius on rear shoulder
RA4	0.3	Ref.	Internal radius on module slot to accommodate location features on rail

N.B. For in-board mount option please refer to dimensions E1, H1 and M1.

Table 22 - Definition of Transceiver Module Dimensions

DATUM	DESCRIPTION
A	BOTTOM SURFACE OF TRANSCEIVER BODY
C	CENTRAL VERTICAL PLANE OF TRANSCEIVER BODY
D	BACK SURFACE OF MODULE BEZEL, SAFETY HARD STOP
E	TOP SURFACE OF HOST PCB
H	BACK FACE OF TRANSCEIVER PCB
L	VERTICAL FACE OF MODULE HARD STOP, HARD STOP ON RAIL

Table 23 - Definition of Transceiver Module Datums

12.2 PHYSICAL ARRANGEMENT (IN-BOARD MOUNT)

Module body footprint for in-board mount modules remain the same with the exception to the front flange, which may not exceed dimensions E1, H1, and M1.

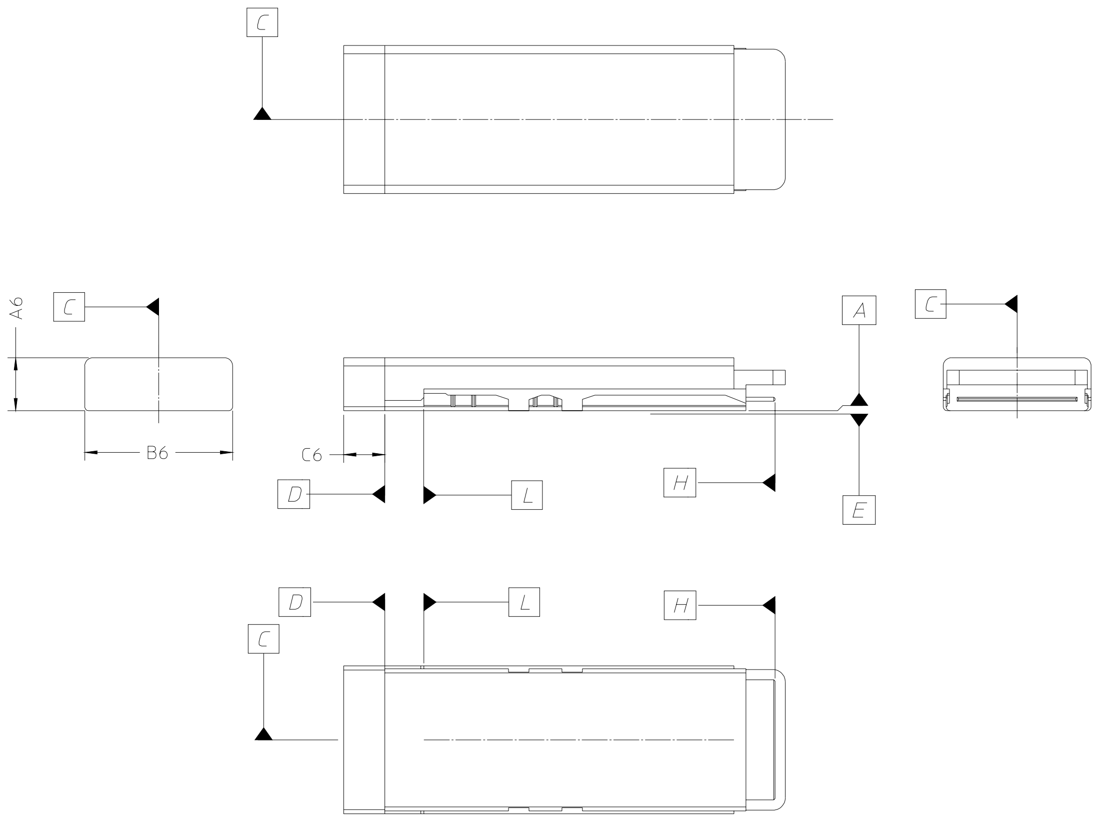
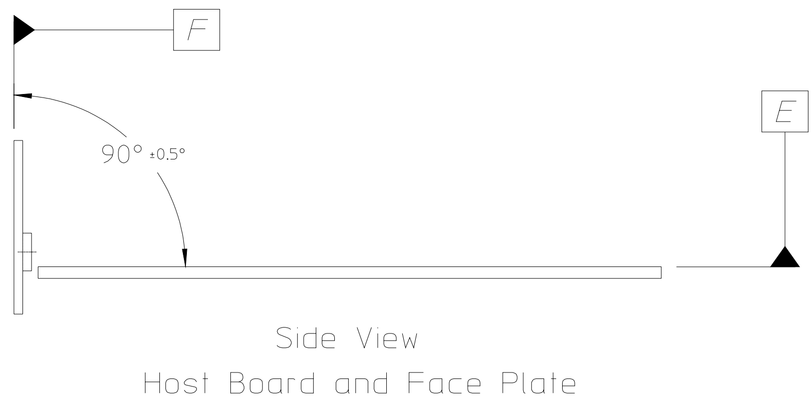


Figure 4 - Mechanical Outline (In-board Mount)

KEY	VALUE (mm)	TOLERANCE (mm)	COMMENT
A6	12.9	Ref.	Height of transceiver body, overall height of in-board mount transceiver
B6	36.0	Ref.	Width of transceiver body, overall width of in-board mount transceiver
C6	10.0	Max.	Datum D to front of module body, in-board as well as front-panel mount options

Table 24 - Definition of In-board Transceiver Module Dimensions

12.3 CUSTOMER FACEPLATE & BOARD PROFILE



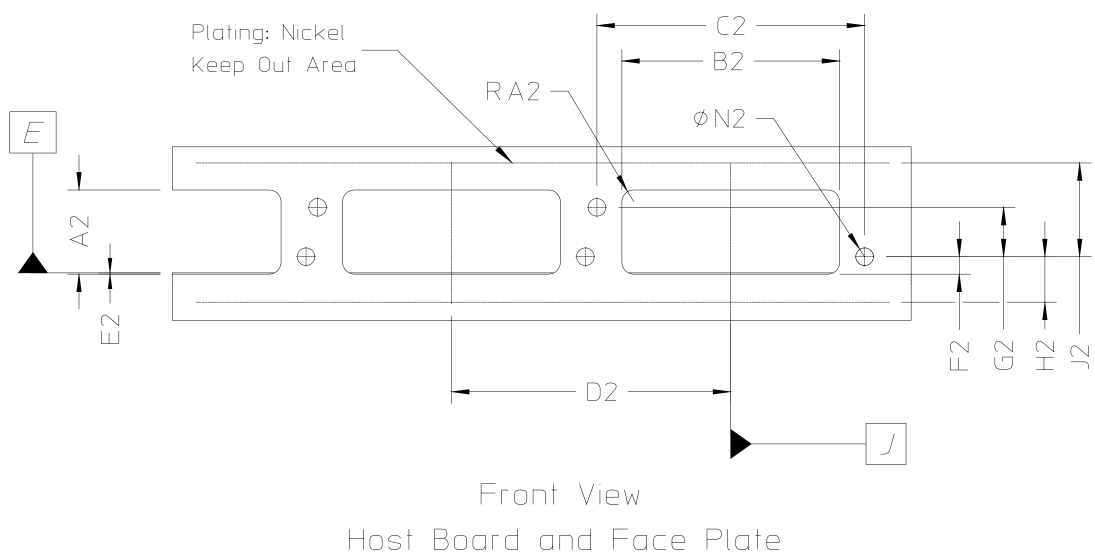


Figure 5 - Side View and Front View of Host PCB and Face Plate

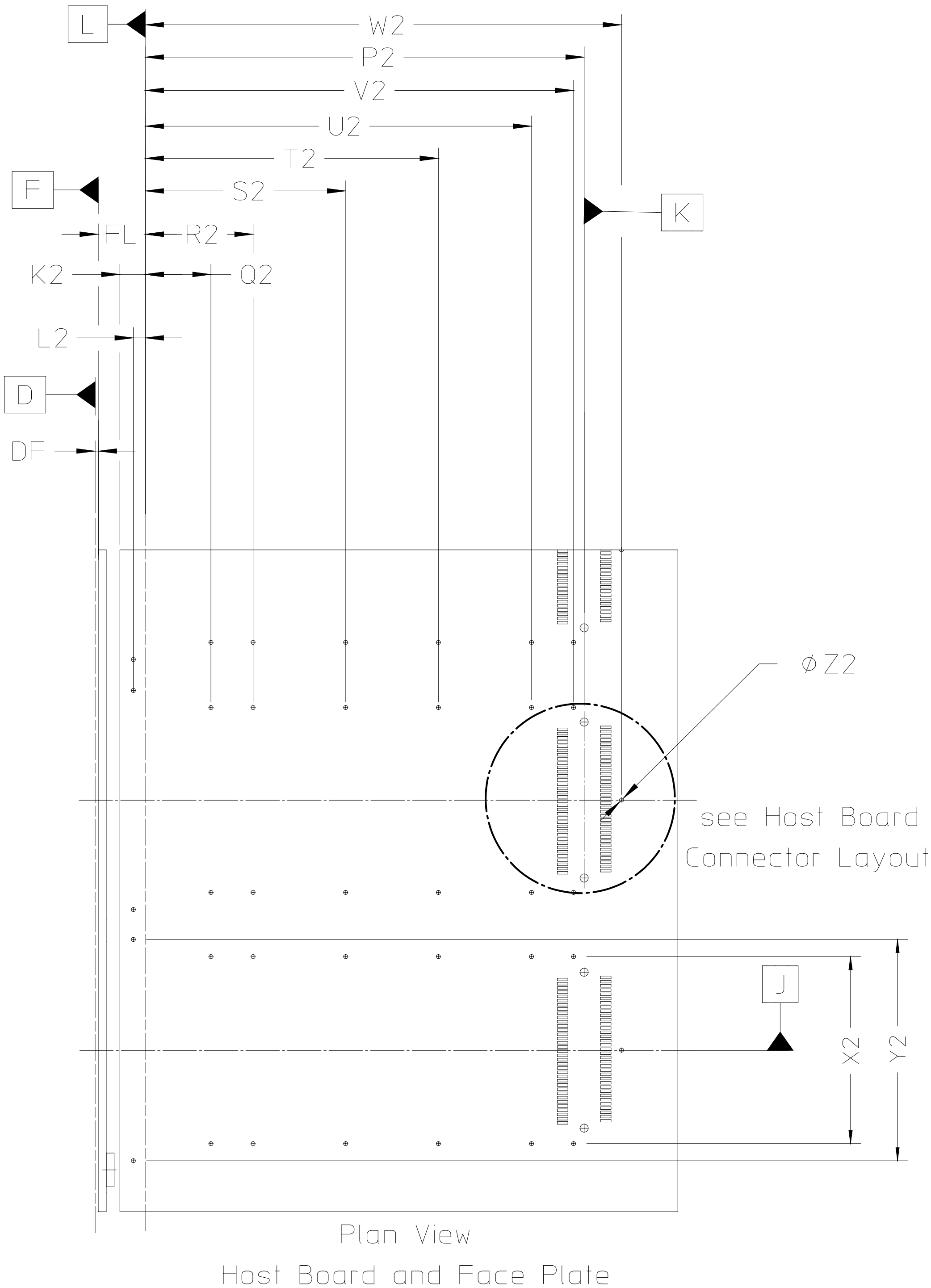


Figure 6 - Faceplate and Host Board for Faceplate Mount Modules

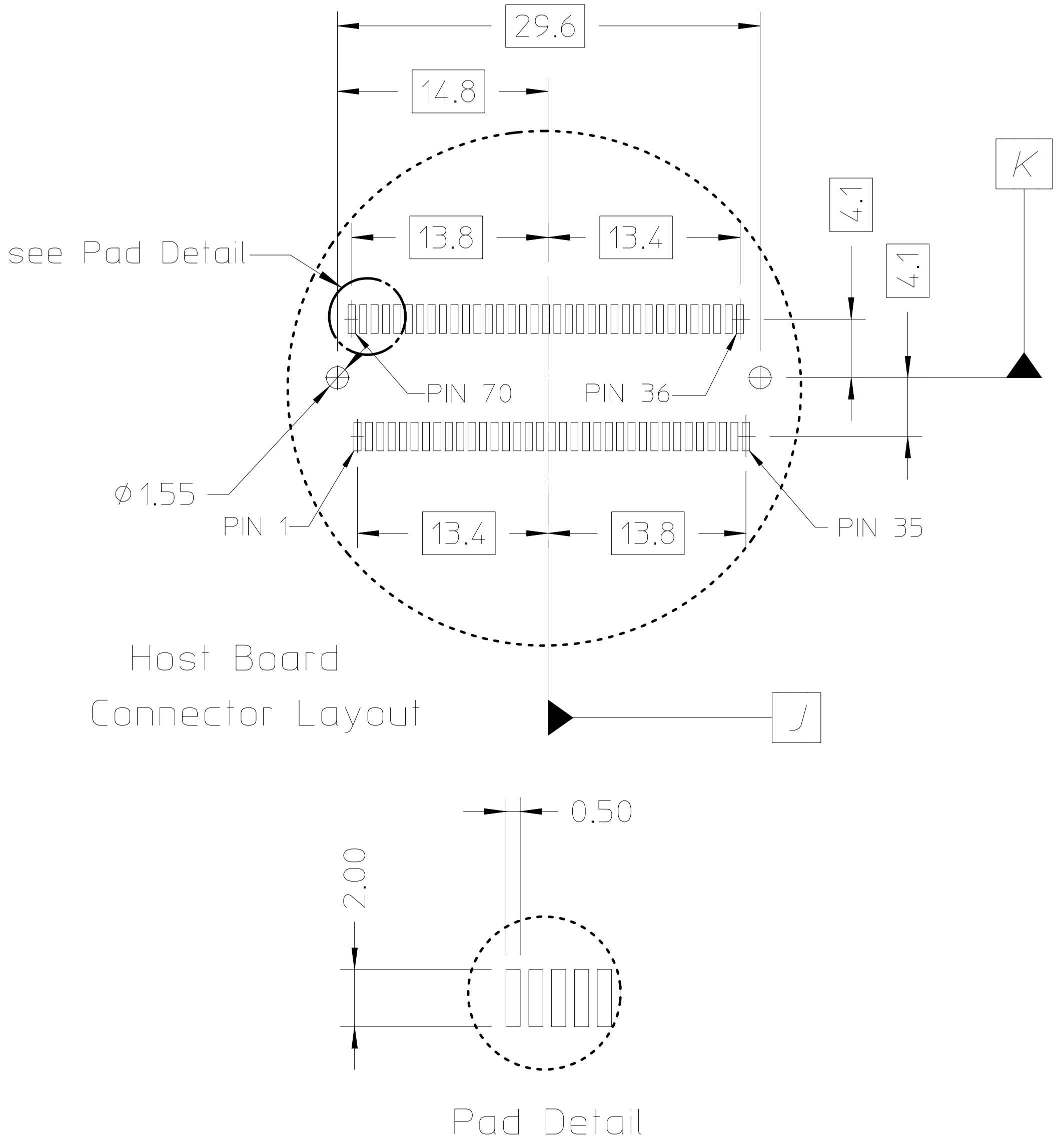


Figure 7 - Host Board Connector Layout

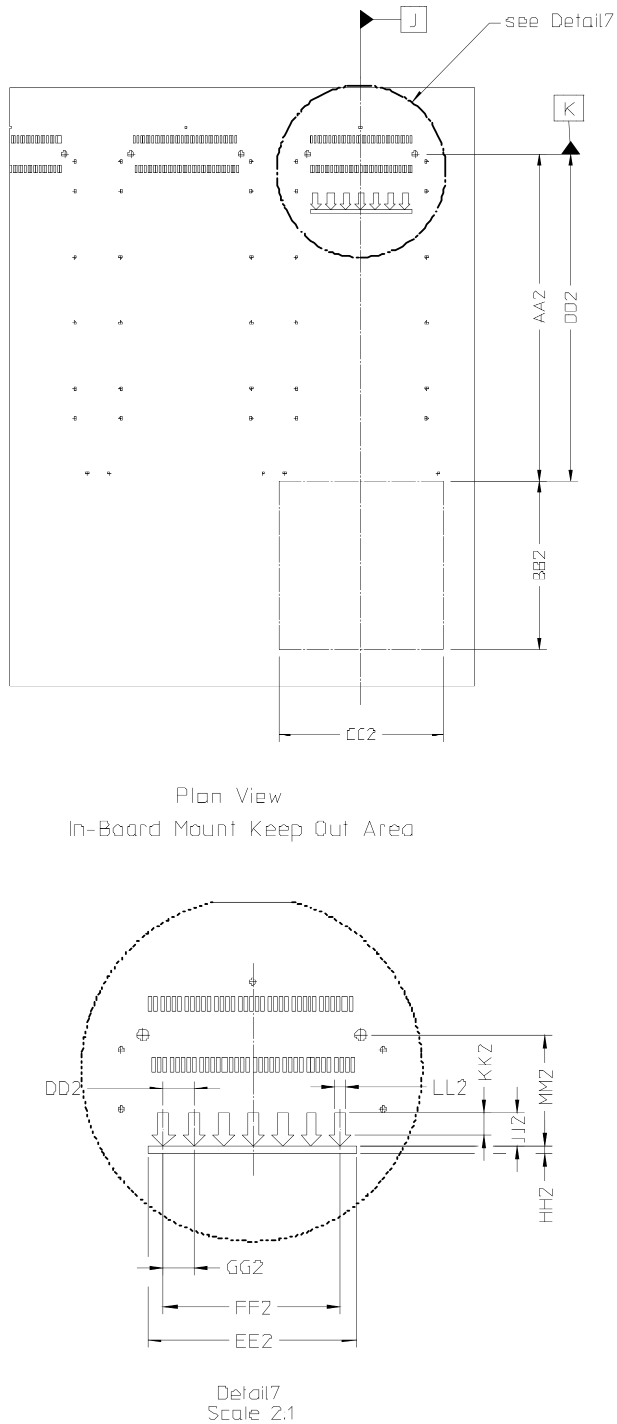


Figure 8 - Host Board Keep Out Areas for In-Board Mount Modules

KEY	VALUE (mm)	TOLERANCE (mm)	COMMENTS
A2	14.3	+/- 0.15	Cut-out in host face plate, 'Y' axis
B2	37.0	+/- 0.15	Cut-out in host face plate, 'X' axis
C2	45.5	+/- 0.2	Distance between mounting holes for captive thumb screws, 'X' axis
D2	47.47	Min	Distance between adjacent transceiver modules
E2	0.2	+/- 0.3	Datum E to bottom of cut-out in host face plate
F2	2.95	+/- 0.15	Lower mounting hole to bottom of cut-out in host face plate
G2	8.4	+/- 0.15	Distance between mounting holes for captive thumb screws, 'Y' axis
H2	6.3	Min	Distance between lower mounting hole and bottom of keep out on host face plate, 'Y' axis
J2	14.7	Min	Distance between lower mounting hole and top of keep out on host face plate, 'Y' axis
K2	4.8	+/- 0.2	Datum L to front edge host PCB edge
L2	2.25	+/- 0.2	Datum L to first plated through holes on host PCB for rail
N2	M3	0.2 Positional	Hole tapped for M3 captive screws
P2	83.4	+/- 0.2	Datum L to Datum K
Q2	12.5	+/- 0.2	Datum L to second plated through holes in host PCB for rail
R2	20.5	+/- 0.2	Datum L to third plated through holes in host PCB for rail
S2	38.1	+/- 0.2	Datum L to fourth plated through holes in host PCB for rail
T2	55.7	+/- 0.2	Datum L to fifth plated through holes in host PCB for rail
U2	73.4	+/- 0.2	Datum L to sixth plated through holes in host PCB for rail
V2	81.4	+/- 0.2	Datum L to seventh plated through holes in host PCB for rail
W2	90.5	+/- 0.2	Datum L to eighth plated through hole in host PCB for rail
X2	35.5	+0, -0.2	Distance between inner mount holes for rail, 'X' axis
Y2	42.0	+0, -0.2	Distance between outer mount holes for rail, 'X' axis
Z2	0.8	+0.1 / -0	Diameter of plated through holes for rail
AA2	87.9	+/- 0.5	Datum K to inner edge of keep out area for in-board mount option
BB2	45.0	+/- 0.5	Depth of keep out area for in-board option
CC2	45.0	+/- 0.5	Width of keep out area for in-board option
EE2	28.2	+/- 0.2	Width of reference stop line of host card PCB for in-board mount
FF2	24.0	+/- 0.2	6 pitches of GG2
GG2	4.0	+/- 0.2	Individual pitch between arrow
HH2	0.9	+/- 0.2	Length of reference stop line of host card PCB for in-board mount
JJ2	4.6	+/- 0.2	Overall length of arrow
KK2	3.0	+/- 0.2	Length of arrow

LL2	1.5	+/- 0.2	Width of arrow
MM2	15	+/- 0.2	Location position of reference stop line of host card PCB for in-board mount
RA2	2.0	Max	Internal radii for cut-out in host face plate

Table 25 - Definition of Host Card / Face Plate Dimensions

DATUM	DESCRIPTION
E	Top surface of host PCB
F	Front surface of host face plate
J	Centre vertical plane of rail system
L	Vertical face of module hard-stop, hard-stop on rail.
K	Centre of 70 way edge connector mounting holes

Table 26 - Definition of Host Card / Face Plate Datums

12.4 MODULE ELECTRICAL CONNECTOR

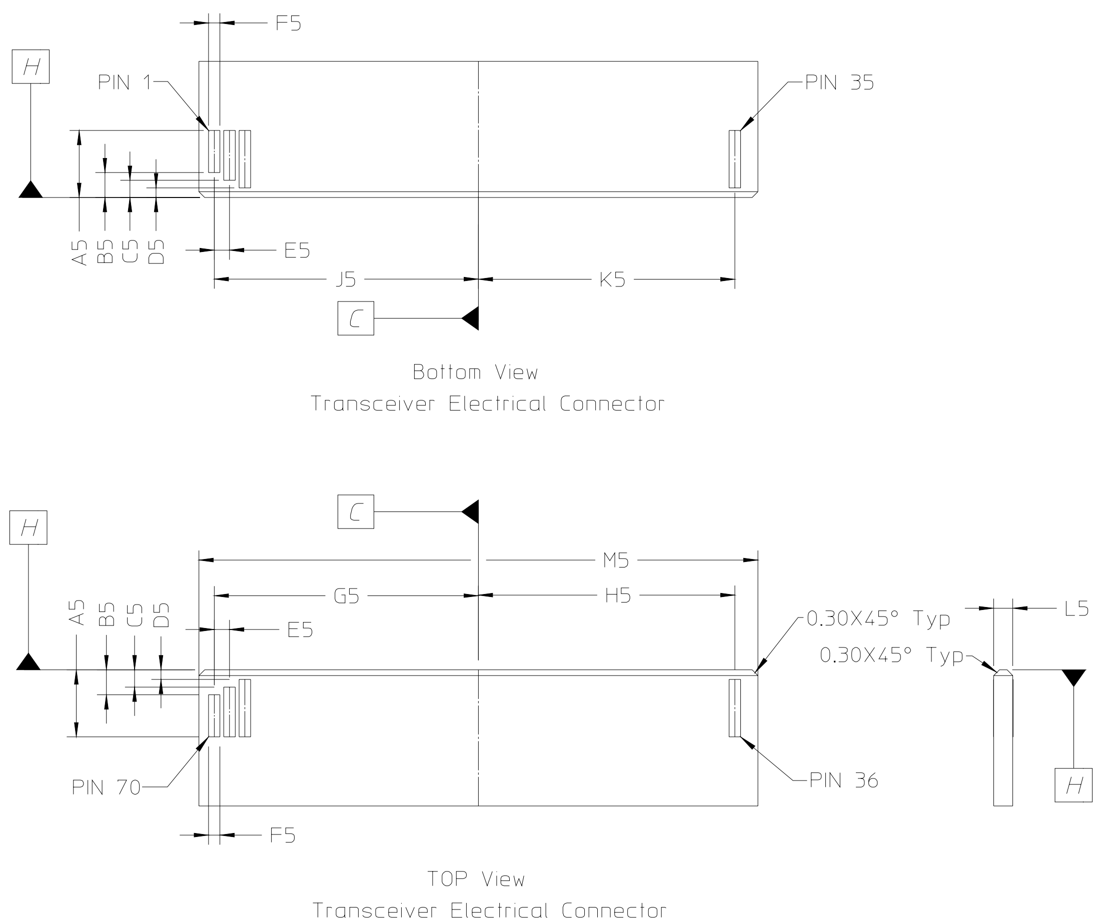


Figure 9 - Module Electrical Connector Pad Definition

KEY	VALUE (mm)	TOLERANCE (mm)	COMMENTS
A5	3.5	Min Typ	Datum H to rear of connector pins
B5	1.3	+/-0.05	Datum H to typical signal connector pin
C5	0.9	+/-0.05	Datum H to typical power connector pin
D5	0.5	+/-0.05	Datum H to typical ground connector pin
E5	0.8	+/-0.05	Distance between connector pins
F5	0.6	+0.05	Width of connector pins

G5	13.8	Ref.	Datum C to PIN 70
H5	13.4	Ref.	Datum C to PIN 36
J5	13.4	Ref.	Datum C to PIN 1
K5	13.8	Ref.	Datum C to PIN 35
L5	1.0	+/-0.1	Transceiver PCB thickness over pins
M5	29.2	+/-0.1	Width of transceiver circuit card

Table 27 - Module Electrical Connector Dimensions

DATUM	DESCRIPTION 70 WAY ELECTRICAL CONNECTOR
C	Centre vertical plane of transceiver body.
H	Back face of transceiver PCB.

Table 28 - Definition of Electrical Connector Datums

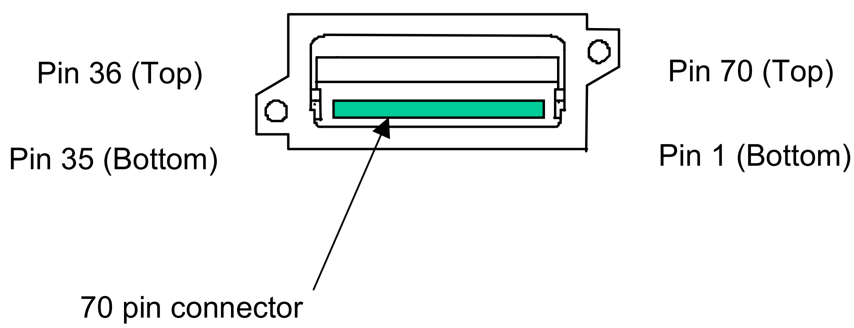


Figure 10 - Rear View of Module Showing Relative Pin Positions

12.5 PCB MOUNT RAIL SYSTEM

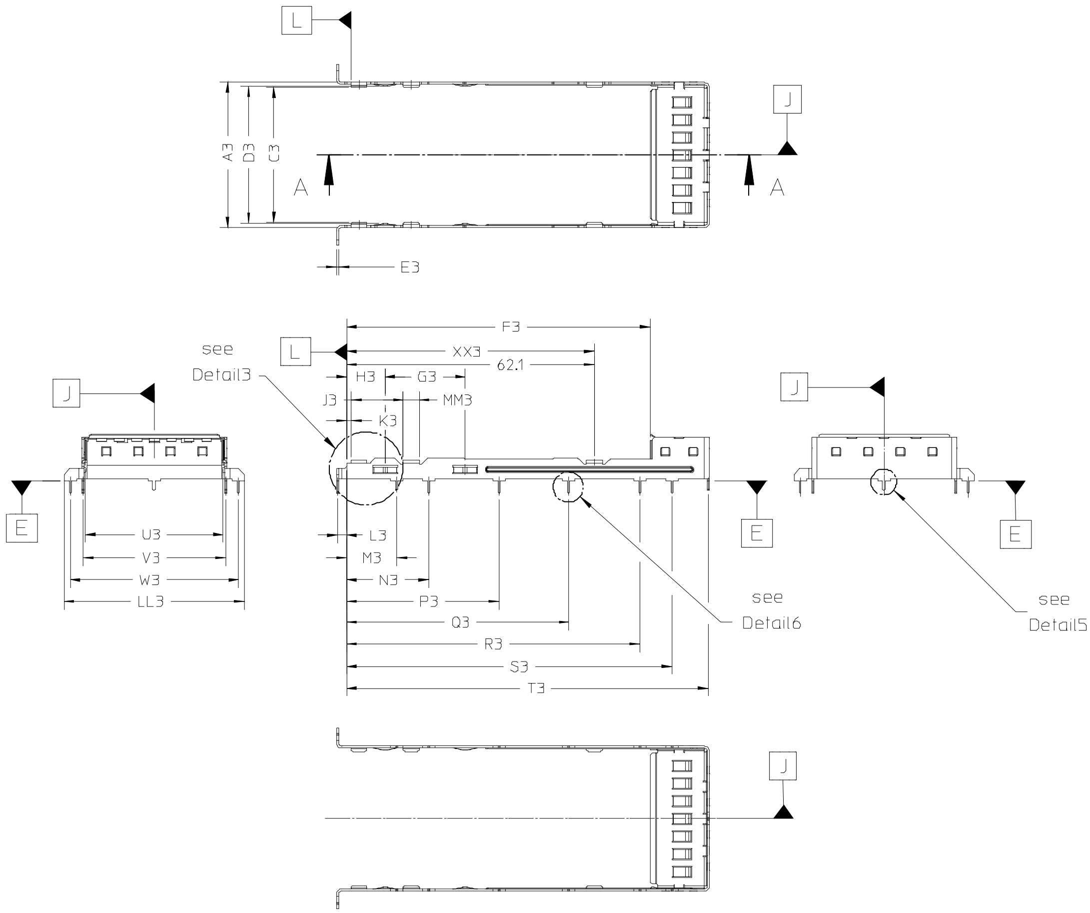


Figure 11 - Host Rail System Outline Drawing

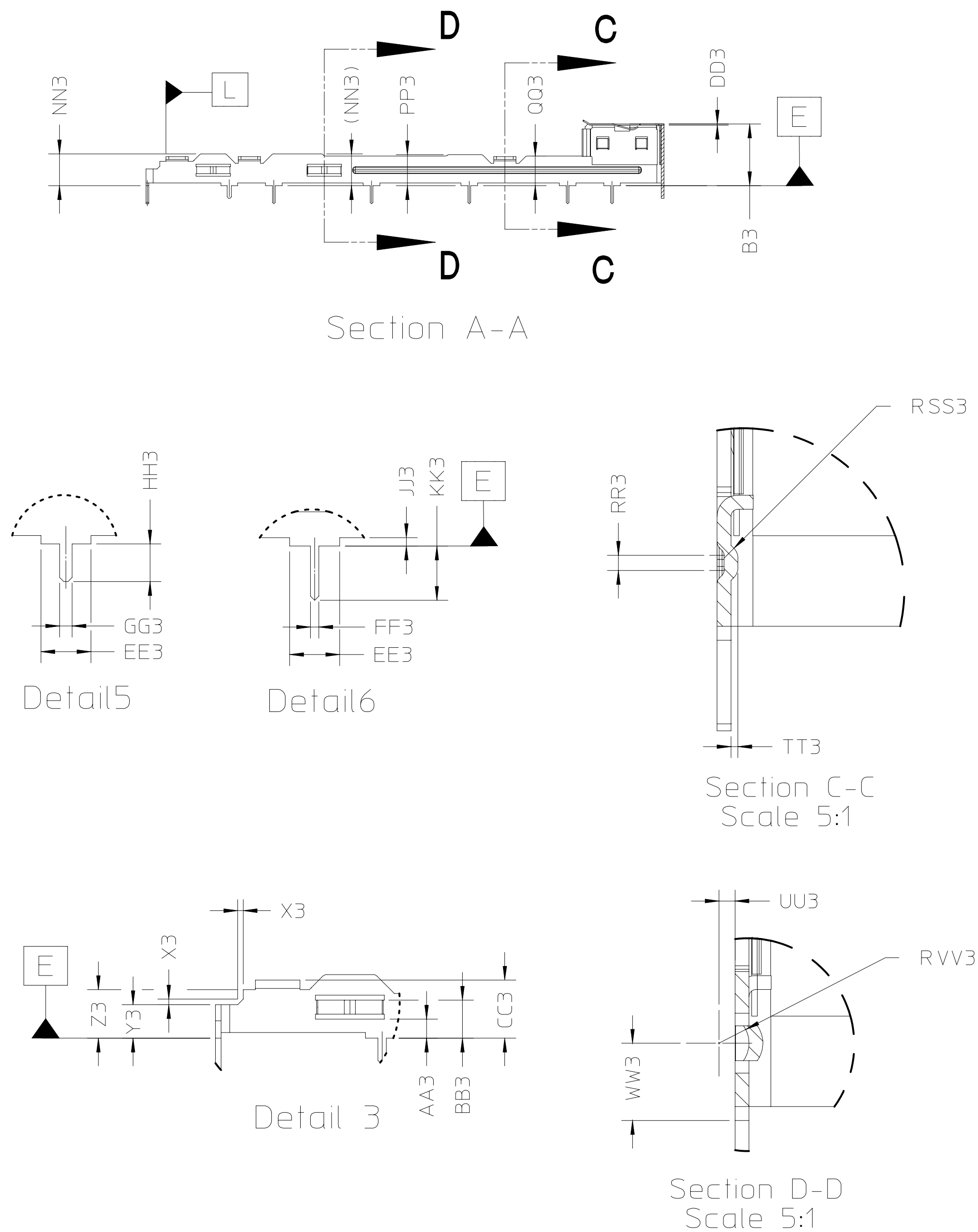


Figure 12 - Host Rail System Details

KEY	VALUE (mm)	TOLERANCE (mm)	COMMENTS
A3	36.0	+0 / -0.2	Overall width of body of rail system.
B3	11.05	+/-0.2	Datum E to top of rail system
C3	33.4	+/-0.2	Internal width of rail system at guide features
D3	34.0	+0.3 / -0	Internal width of rail system at location features
E3	0.5	+/-0.01	Material thickness of body of rail system
F3	76.0	+/-0.2	Datum L to beginning of EMI shield to accommodate transceiver rear shoulder
G3	20.0	+/-0.15	Pitch of location features
H3	9.6	+/-0.15	Datum L to centre of first location feature
J3	13.0	+/-0.15	Pitch of guide features
K3	1.1	+/-0.1	Datum L to first guide feature
L3	2.25	+/-0.2	Datum L to first solder pin
M3	12.5	+/-0.2	Datum L to second solder pin
N3	20.5	+/-0.2	Datum L to third solder pin
P3	38.1	+/-0.2	Datum L to fourth solder pin
Q3	55.7	+/-0.2	Datum L to fifth solder pin
R3	73.4	+/-0.2	Datum L to sixth solder pin
S3	81.4	+/-0.2	Datum L to seventh solder pin
T3	90.5	+/-0.2	Datum L to eighth solder pin
U3	34.4	REF	Internal width of rail system at EMI shield
V3	35.5	+0 / -0.2	Distance between centres of inner solder pins, 'X' Axis
W3	42.0	+0 / -0.2	Distance between centres of outer solder pins, 'X' Axis
X3	0.5 Max	+0 / -0.05	Height and length of chamfer at base of hard stop
Y3	3.0	+/-0.05	Datum E to base of hard stop
Z3	4.35	+/-0.1	Datum E to top of hard stop
AA3	1.7	+/-0.1	Datum E to base of location features
BB3	3.4	+/-0.1	Datum E to top of location features
CC3	5.2	+/-0.1	Datum E to top of guide features
DD3	0.2	+/-.01	Material thickness of EMI shield
EE3	3.0	+/-0.2	Width of board stand-off at solder pins
FF3	0.5	+/-0.05	Width of first mate solder pins
GG3	0.75	+0 / -0.1	Width of second mate solder pins
HH3	2.25	+/- 0.1	Height of second mate solder pins
JJ3	0.5	+/- 0.2	Height of board stand-off at solder pins
KK3	3.25	+/-0.1	Height of first mate solder pins
LL3	45.0	+/-0.2	Overall width of rail system
MM3	4.0	+/-0.1	Width of guide features
NN3	5.7	+/- 0.1	Local vertical height of hard stop to module
PP3	5.55	+/- 0.1	Local vertical height of hard stop to module

QQ3	4.8	+/-0.1	Local vertical height of hard stop to module
RR3	0.5	+/- 0.1	Flat section of strengthening feature
RSS3	0.5	+/- 0.1	Radius of strengthening feature
TT3	0.25	MAX	Max allowable protrusion for strengthening feature
UU3	0.6	+/- 0.1	Horizontal position for center of radius of formed feature
RVV3	1.0	+/- 0.1	Radius of formed rail feature
WW3	2.8	+/- 0.1	Vertical position of formed rail feature
XX3	62.1	+/- 0.15	Position of location feature

Table 29 - Definition of Rail System Dimensions

12.6 CONNECTOR DESCRIPTION

Customer connector is the TycoAMP 70 position Right angle Connector Assembly (0.8mm pitch), part number 1367337-1 (or similar).

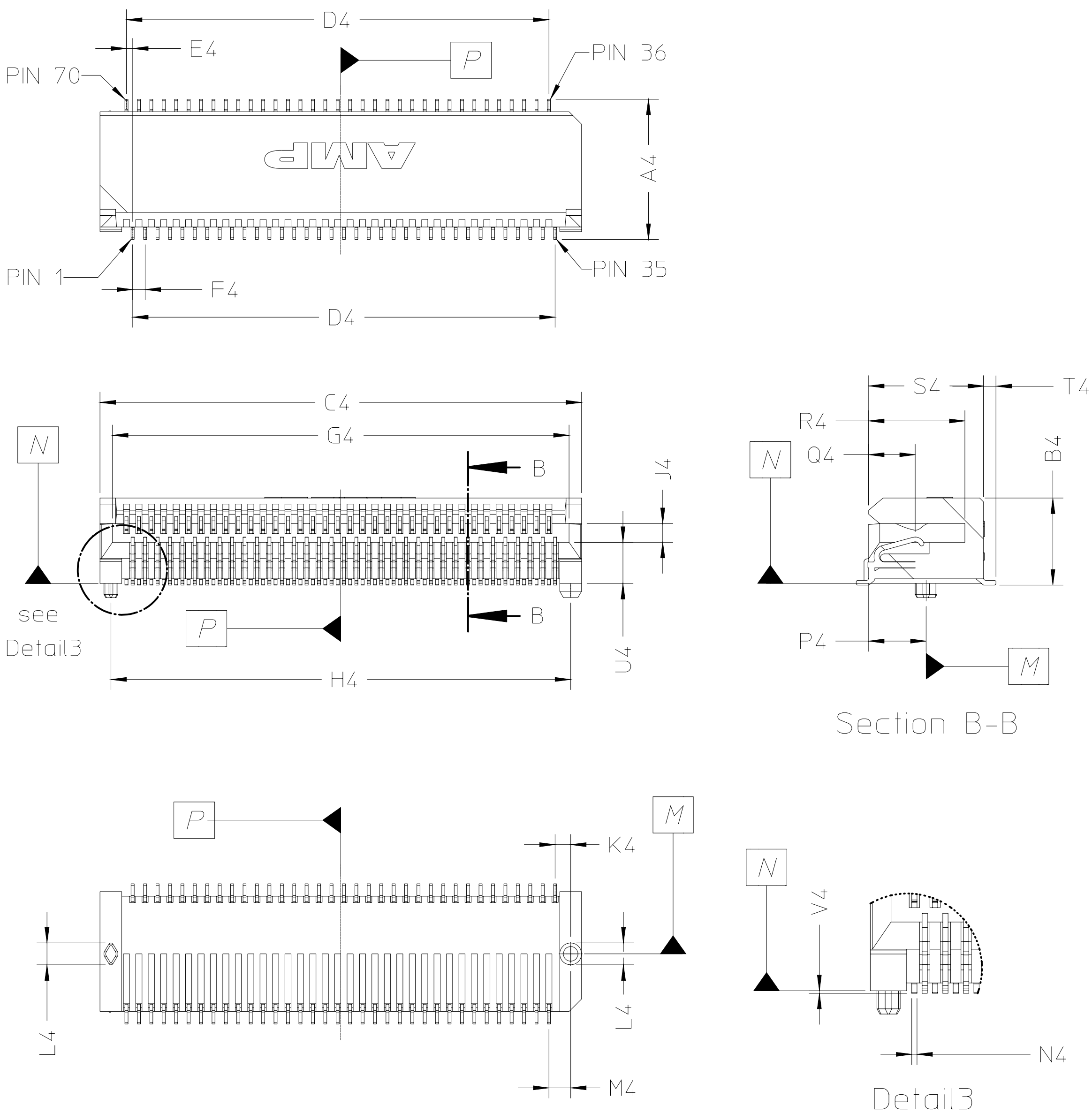


Table 30 - 70-way Electrical Connector Layout

KEY	VALUE (mm)	TOLERANCE (mm)	COMMENTS
A4	9.2	Max	Connector length
B4	5.9	Max	Connector height
C4	31.2	Max	Connector width
D4	27.2	Ref.	Contact array width
E4	0.4	Typ.	Offset of second row of contacts from first
F4	0.8	Typ.	Pitch of contacts
G4	29.4	+/-0.08	Connector card slot width
H4	29.6	TP	Distance between guide pins
J4	1.35	Max	Connector Card Slot Height
K4	1.0		Round guide pin to PIN 35
L4	1.4		Width of guide pins
M4	1.4		Round guide pin to PIN 36
N4	0.2		Width of contacts
P4	3.7		Datum M to mouth of connector card slot
Q4	3.0	Max	Depth of contact point from mouth of connector card slot
R4	6.0	Min	Depth of card slot from mouth of connector card slot
S4	7.4		Back of connector from mouth of connector card slot
T4	0.8		Length of solder leads past housing, front and rear
U4	2.6	Min	Datum N to bottom of card slot
V4	0.1	+0.1-0.13	Datum N to bottom of contacts

Table 31 - 70-way Electrical Connector Dimensions

DATUM	DESCRIPTION
M	Centre vertical plane of guide pins
N	Bottom of connector stand off surfaces
P	Centre vertical plane of connector

Table 32 - 70-way Electrical Connector Datums

13 ENVIRONMENTAL CONDITIONS

Environmental Conditions are a mandatory requirement.

13.1 THERMAL REQUIREMENTS

This section sets the boundary conditions for thermal dissipation and cooling, to ensure inter-operability of transceivers from different suppliers.

13.2 COOLING

A single transceiver should be capable of normal operation under the following worst-case conditions:

55^{o}C maximum ambient air temperature

1.0 metre/second minimum air flow

Possible directions of airflow are as shown in the Figure below.

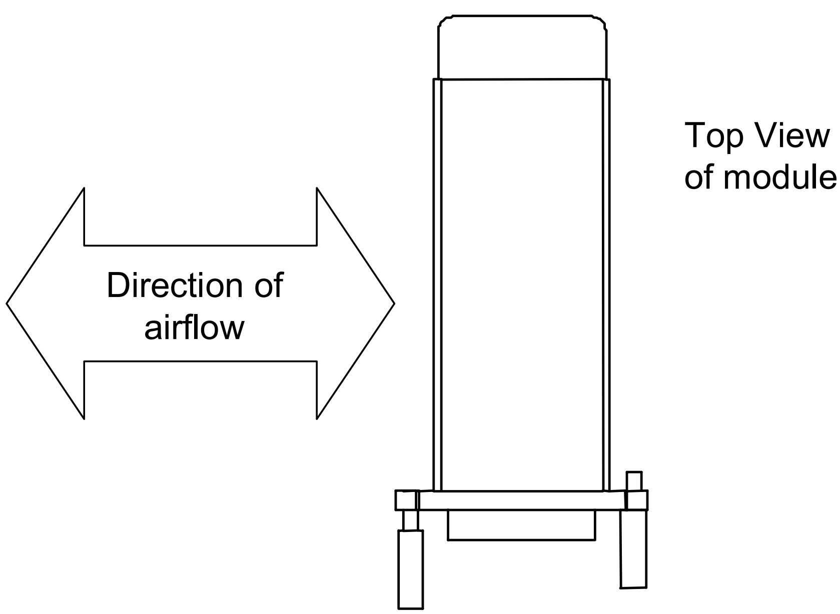


Figure 13 - Airflow Direction

14 PIN ASSIGNMENT

Top Row			Bottom Row		
Mating sequence	Pin	Description	Description	Pin	Mating Sequence
1	70	Gnd (Tx)	Vcc (TEC)	1	2
1	69	Gnd (Tx)	Vcc (TEC)	2	2
3	68	*TxClk (-ve)*	Vcc (TEC)	3	2
3	67	*TxClk (+ve)*	Gnd (TEC)	4	1
1	66	Gnd (Tx)	Gnd (TEC)	5	1
3	65	Reserved	Gnd (TEC)	6	1
3	64	Reserved	Vcc (Tx)	7	2
1	63	Gnd (Tx)	Vcc (Tx)	8	2
3	62	Reserved	Gnd (Digital)	9	1
3	61	Reserved	SDA	10	3
1	60	Gnd (Tx)	SCL	11	3
3	59	Reserved	Module Enable	12	3
3	58	Reserved	Vcc (Digital)	13	2
1	57	Gnd (Tx)	Gnd (Digital)	14	1
3	56	Tx Data (-ve)	Tx Disable	15	3
3	55	Tx Data (+ve)	Tx Alarm	16	3
1	54	Gnd (Tx)	Tone Input	17	3
1	53	Gnd (Tx)	Tone Output	18	3
1	52	Gnd (Rx)	Rx Alarm	19	3
3	51	Reserved	Rx LOS	20	3
3	50	Reserved	SLA-AD2	21	3
1	49	Gnd (Rx)	SLA-AD1	22	3
3	48	Reserved	SLA-AD0	23	3
3	47	Reserved	Vendor Reserved	24	3
1	46	Gnd (Rx)	Vendor Reserved	25	3
3	45	Reserved	Vendor Reserved	26	3
3	44	Reserved	Vendor Reserved	27	3
1	43	Gnd (Rx)	Vendor Reserved	28	3
3	42	Rx Data (-ve)	Module Sense	29	3
3	41	Rx Data (+ve)	Vcc (Rx)	30	2
1	40	Gnd (Rx)	Vcc (Rx)	31	2
3	39	*Rx Clk (-ve)*	Vcc (Rx Bias)	32	2
3	38	*Rx Clk (+ve)*	Gnd (Rx Bias)	33	1
1	37	Gnd (Rx)	Gnd (Rx Bias)	34	1
1	36	Gnd (Rx)	Gnd (Rx)	35	1

Notes:-

1) "Reserved" Pins are reserved by the MSA for future function. These are " No user Connect"
(ie. should not be connected to ground)
2) "Vendor Reserved" Pins are reserved vendor specific function. For connection, refer to vendor datasheet.

3) All ground connections should have the same potential

Module Status Outputs	Management Input/Output
Module Control Inputs	Positive Supply Voltage
Clock/Data Input/Output	Negative Supply Voltage
Vendor Specific Functions	Reserved Functionality (MSA)