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A Packaged 60 GHz Low-Power Transceiver with Integrated Antennas for Short-Range Communications

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Abstract — This paper describes a 60-GHz transceiver with integrated antennas for short range and low power wireless communications fabricated in a CMOS 65nm SOI technology. The transceiver uses an on-off-keying UWB pulse modulation and is packaged in a standard QFN48L pre-molded cavity package with removable lid. The transceiver performances at 60-GHz was evaluated using the full wave 3D electromagnetic and the circuit co-simulation.

Index Terms — Millimeter-wave antennas, integrated antennas, 60 GHz, packaging, system-on-chip, system-in-package.

I. INTRODUCTION

Future consumer mobile platforms will need high data rate wireless connections for data exchange and video streaming. 60-GHz band has been intensively explored for such purpose [1-3, 5]. A first approach consists in using classical coherent architecture with frequency modulated signals (QPSK, 16-QAM) and high spectral efficiency. However, such systems exhibit a low energy efficiency resulting in high power consumption that makes them unsuitable for autonomous mobile devices like smart phones [1, 2]. A trade-off between spectral efficiency and transmission range combined to simplified architecture can respond to challenges such as multi-Gbps data rate and sub 100-mW power consumption. This work describes a transceiver on a 65-nm CMOS-SOI technology achieving low power wireless (sub 50pJ/bit) at 2-Gbps transmission for short range (7-cm).

II. MM-WAVE INTEGRATED UWB TRANSCEIVER

The transceiver uses an on-off-keying (OOK) modulation scheme with pulsed signals in the 57–62 GHz frequency band. The transmitter (*Tx*) consists in a pulse generator, a power amplifier and an integrated antenna (Fig. 1a). It is similar to the Tx in [4] and it is used as a V-band continuous wave signal generator (free running oscillator) for the antenna characterization (Section III). The receiver (*Rx*) includes an integrated antenna, a low-noise amplifier (LNA), a super-regenerator oscillator (SRO) and an envelope detector (Fig. 1b). Additional analogue and digital circuits are

integrated for synchronization and digitization. Both *Tx* and *Rx* antennas are identical and presented in Section III. The circuit is implemented in a standard 65-nm CMOS-SOI (Silicon-on-Insulator) technology with high-resistivity silicon substrate (STMicroelectronics).

The transceiver chip size is $3.1 \times 1.9 \times 0.3 \text{ mm}^3$ and this transceiver is mounted in a QFN pre-molded cavity package (Fig. 2) soldered on a test board with connections to power supplies and input/output signals.

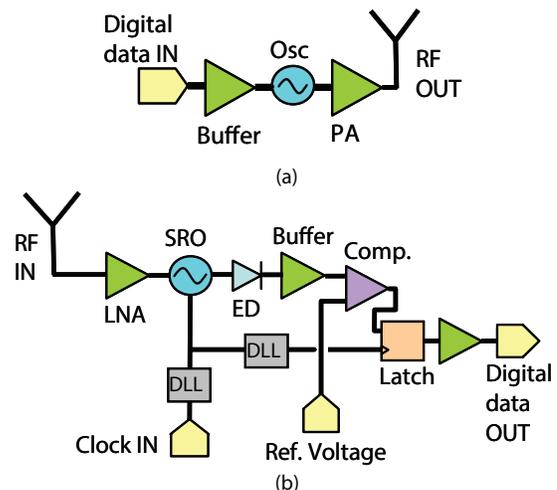


Fig. 1. Block level architecture (*Tx* chain (a), *Rx* chain (b)).

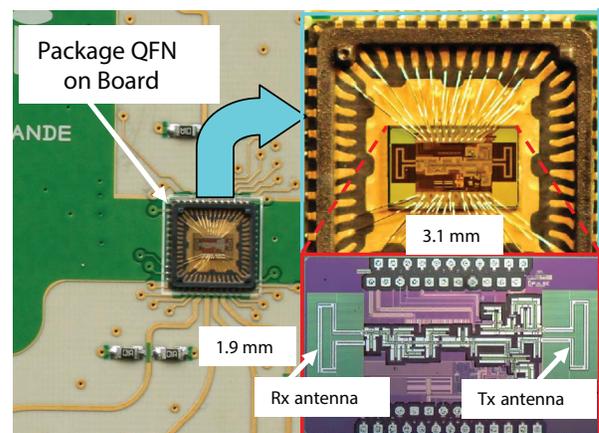


Fig. 2. Packaged circuit on the test board (lid removed).

III. INTEGRATED ANTENNAS AND PACKAGING

The QFN48L package size is $7 \times 7 \times 1.75 \text{ mm}^3$, the walls and lid of the package are made of Liquid Crystal Polymer (LCP) with a dielectric permittivity $\epsilon_r = 3.225$ and a loss tangent $\tan\delta = 0.007$. The lead-frame of the package (leads, die pad) is made of copper with a thickness of 0.2 mm. The chip is bonded in the package with 25- μm aluminum wires.

The electromagnetic (EM) model of the transceiver chip takes into account (i) a ground plane ($1.9 \times 1.9 \text{ mm}^2$ including the I/O pads), (ii) the main t-lines (coplanar waveguide lines), (iii) a metal ring (width 9 μm) at the periphery of the chip, and (iv) the actual geometry of the antenna feed (Fig. 3a). The ground plane is a stack of the six metal layers (M1–M6, 4.22 μm). The folded dipole antenna ($750 \times 200 \mu\text{m}^2$) and the t-lines are realized on metal layer 6 (M6, 2.99 μm). The two halves of the ground plane are connected by underpasses on metal layer 1 (M1, 0.18 μm) at the feed point of each antenna, as well as each t-line corner. A 3D EM model of the packaged chip, including the 43 bond-wires, was designed and simulated in Agilent-EMPro (Fig 3).

The simulated impedance of the antenna shows a resonance at 56.9 GHz with an impedance of 46.5 Ω and a reflection coefficient lower than -6 dB across the 55.6–58.2 GHz band (Fig. 4a). The E-plane radiation pattern at 60 GHz exhibits a simulated maximum realized gain of 2.7/1.6 dBi at $\theta = \pm 90^\circ$ and the gain in the broadside direction is about -7.4 dBi (Fig. 4b). In the H-plane, the simulated maximum realized gain is -3.1 dBi at 56° (Fig. 4c). These values are confirmed by the measured radiation patterns.

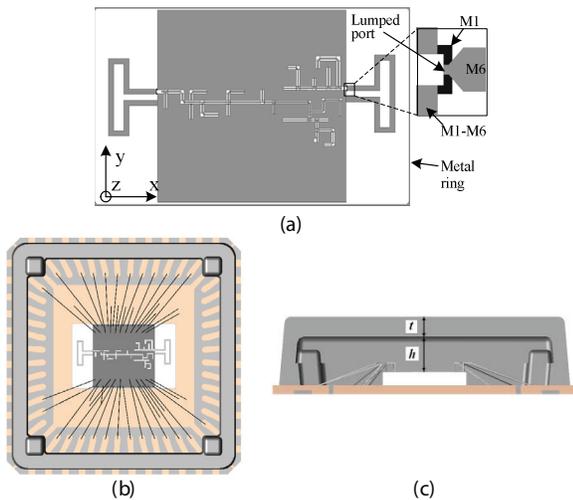


Fig. 3. EM model of the transceiver circuit and integrated folded dipole antenna (a). 3D EM model of the packaged transceiver: top view without lid (b), and cross-section with lid (c) ($t = 0.45 \text{ mm}$, $h = 0.8 \text{ mm}$).

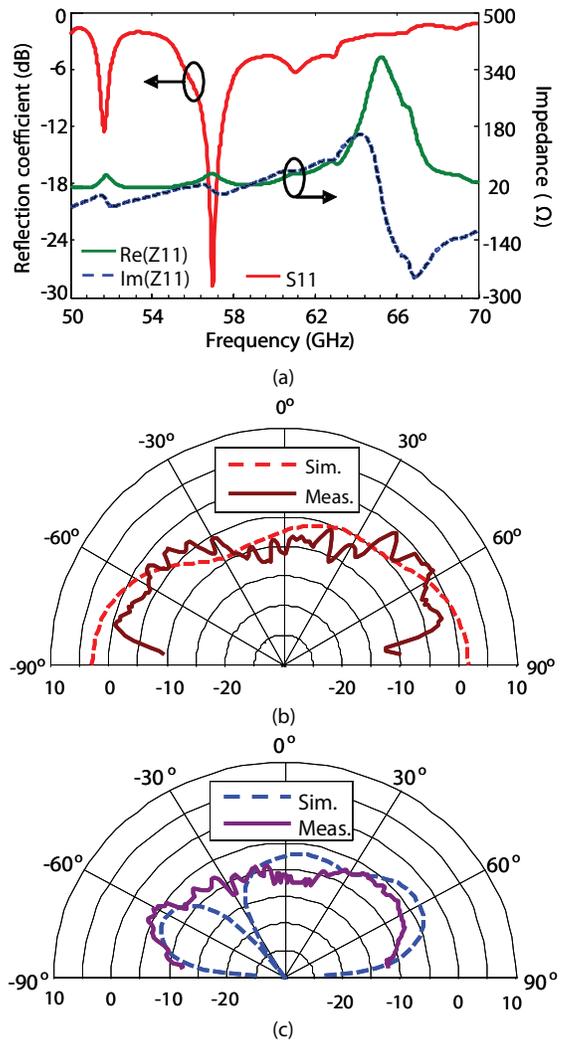


Fig. 4. Performances of the packaged integrated transceiver with lid; simulated return loss and impedance (a), simulated and measured gain radiation patterns at 60 GHz in E-plane (b) and H-plane (c).

IV. TRANSCEIVER-ANTENNA CO-SIMULATION

With on-chip integrated antennas, a real co-design between the receiver/transmitter circuits and the antennas is necessary for a global optimization of the system's performances. The simulations were performed using Agilent ADS and EMPro Finite-Element Method engine at the transceiver level. The co-design approach provides a key advantage over classical methods based on S-Parameter files to model the actual ground current paths and therefore have an accurate description of the current distribution inside the chip. This is specifically important in low power applications where a miscalculation of the ground can limit the voltage swing and lead to limited output power and transmission range. As ADS and EMPro are sharing the

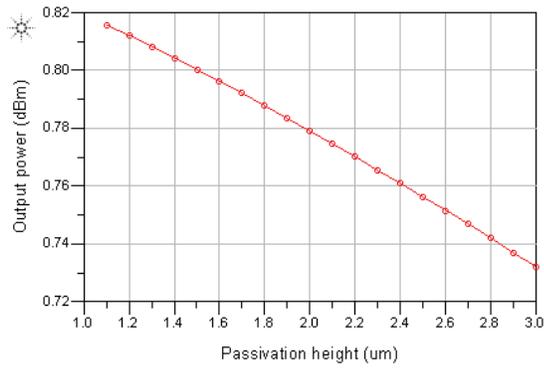


Fig. 5. Influence of process parameters (passivation) on the output power of the transmitter.

same database, a dynamic co-design has also been studied, including for instance the impact of some technology parameters (passivation or substrate thickness) (Fig. 5) or design parameters on the system's performances. For instance, the antenna's impedance, which is difficult to optimize due to the modeling complexity in a CMOS back-end, has a significant impact on the amplifier's gain (Fig. 6a,b) or even a moderate impact on the VCO's oscillation frequency.

V. CONCLUSION

A 60-GHz low-power packaged transceiver with integrated antennas was designed and demonstrated as a low-cost solution for high data rate, low power, and short-range wireless data exchange chipsets. The design relied significantly on a co-design approach of the circuits and integrated antennas to derive the global system performances.

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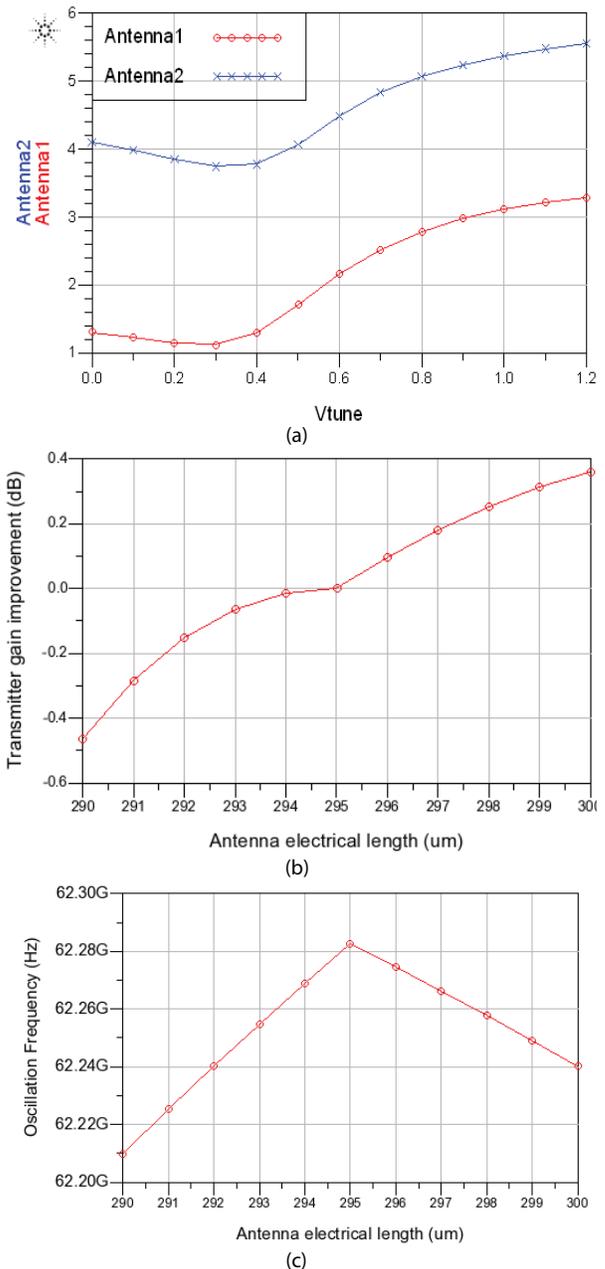


Fig. 6. Influence of design parameters on the transmitter performances; amplifier gain for two different antennas (Antenna 1 is the antenna presented in section III, Antenna 2 is a novel antenna not presented here with a better impedance matching) (a), relative gain of the amplifier (b) and VCO oscillation frequency (c) as a function of the antenna half-length.