



# AMD Socket S1 with M690T Chipset Reference Schematic

## NOTES:

- 1) This schematic supports the AMD Socket S1 CPU devices.
- 2) These are "Reference Schematics" and as such they have not been verified by an actual board build.
- 3) This reference schematic supports AMD M960T revision A12 or later. If A12 or later revision is not used, please see your customer support representative for the necessary application notes for workarounds.
- 4) This reference schematic supports SB600 revision A21 or later. If A21 or later revision is not used, please see your customer support representative for the necessary application notes for workarounds.
- 5) Unless otherwise specified, resistors have 5% tolerance.
- 6) Unless otherwise specified, capacitors have 20% tolerance.

Page	Index	Page	Index
1	Cover Page	17	SB600 PCIe, PCI, LPC, Straps, & CPU Control
2	Revision History	18	SB600 ACPI, GPIO, USB, and Audio Interfaces
3	Block Diagram	19	SB SATA, IDE, SPI, and HW Management Interfaces
4	Clock Structure	20	SB600 Power
5	Power Configuration (1)	21	CRT Connector
6	Power Configuration (2)	22	Broadcom Ethernet Controller
7	Reset & Voltage Sequence	23	Realtek Audio Codec
8	Socket S1 HT Interface	24	LPC BIOS
9	Socket S1 DDR2 Memory Interface	25	USB Power and Connectors
10	Socket S1 Control & Debug	26	Power Main System, SB600 PCIe, & Other
11	Socket S1 Power & Ground	27	Standby Power & Powergood
12	SODIMM DDR2	28	Power for CPU Core
13	M690T HT, PCI, PCIe™, PCIe Graphics Port	29	Power for DDR2 Memory and Interface
14	M690T PLL and Video Interface	30	Power M690T Core, PCIe Interface
15	M690T Power and Side Port Memory Interface	31	Unused Interfaces
16	Clock Generator		

## IMPORTANT NOTICE:

1. THIS DOCUMENT MAY NOT REFLECT THE MOST RECENT CHANGES IN BOARD DEVELOPMENT AND DEBUG. ANY DEVELOPER INTENDING TO USE THIS SCHEMATIC AS A REFERENCE SHOULD CONTACT THEIR LOCAL FIELD APPLICATIONS ENGINEER, REGIONAL SALES OFFICE, OR PROGRAM MANAGER FOR SCHEMATIC UPDATES, DESIGN RECOMMENDATIONS AND PCB LAYOUT GUIDELINES. AMD ALSO RECOMMENDS A DESIGN REVIEW OF BOTH THE SCHEMATIC DIAGRAM AND PCB LAYOUT BEFORE CONSIDERING PRODUCTION.
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## DESIGN CONSIDERATIONS

**DESIGN NOTE:**  
Example text for informational design notes.

**DESIGN NOTE:**  
Example text for cautionary design notes.

**DESIGN NOTE:**  
Example text for critical design notes.

**LAYOUT NOTE:**  
Example text for critical layout guidelines.

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PID	42504	Rev	0.5
Size	Custom	Date:	Tuesday, March 13, 2007
Sheet	1	of	31

Cover Page

**REVISION HISTORY:**

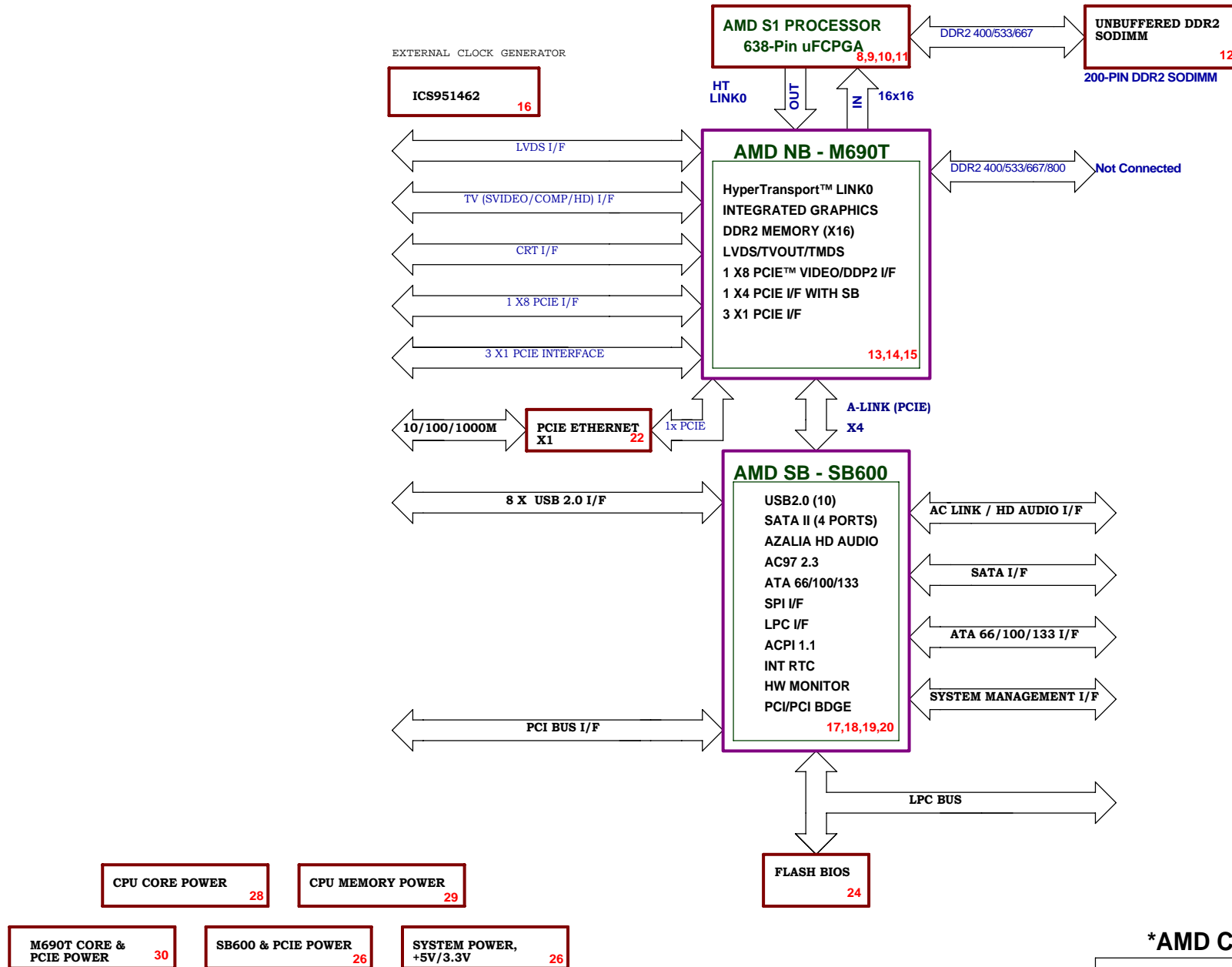
<b>REV</b>	<b>DATE</b>	<b>NOTES</b>
0.5	03/07/2007	Preliminary release

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PID <b>42504</b>		Rev <b>0.5</b>	
Size Custom	Date: Tuesday, March 13, 2007	Sheet <b>2</b>	of <b>31</b>

**Revision History**

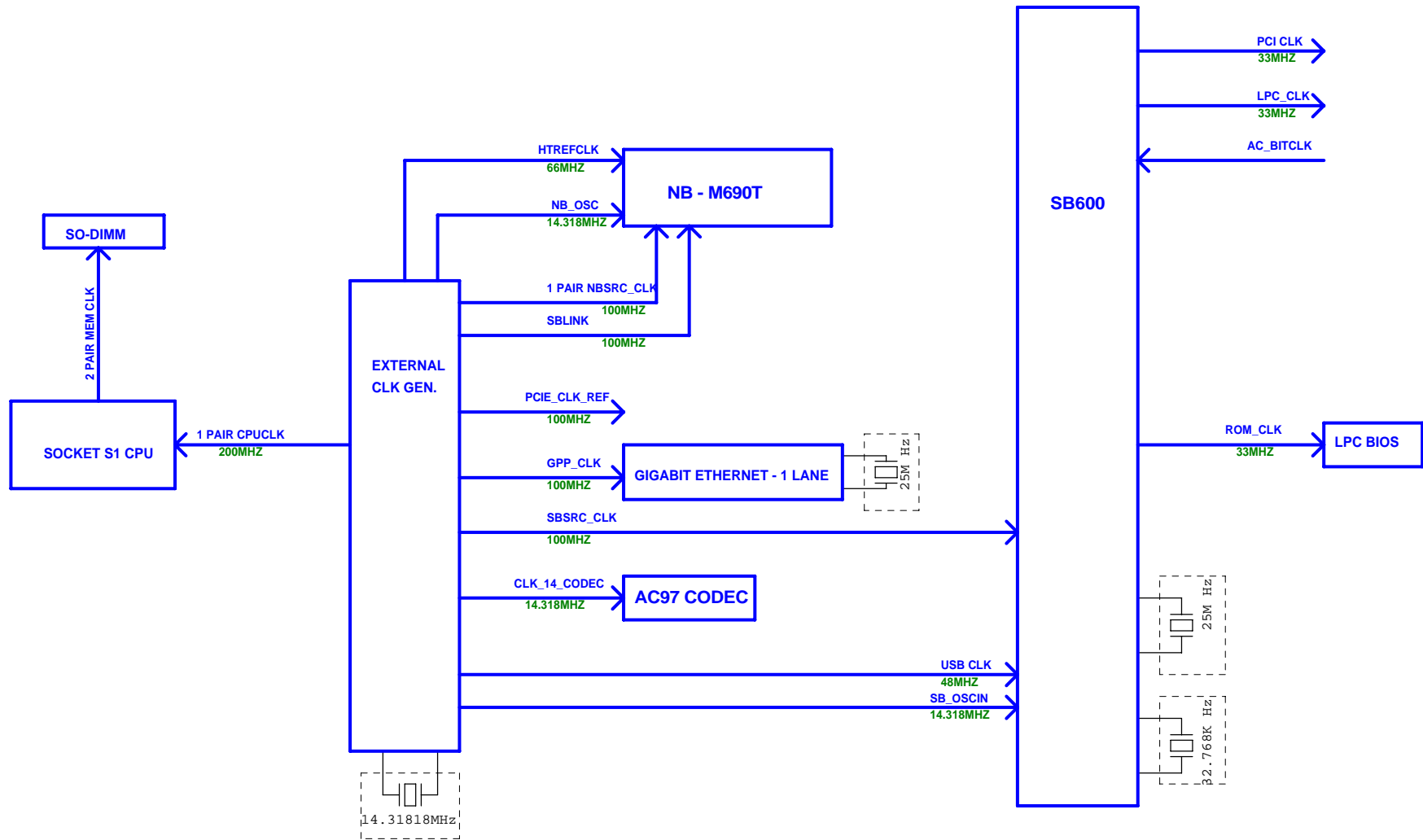
# REFERENCE DESIGN FOR SOCKET S1 / M690T / SB600



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PID	42504	Rev	0.5
Size	Custom	Date:	Tuesday, March 13, 2007
Sheet	3	of	31

Block Diagram



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Size Custom	Date: Tuesday, March 13, 2007	Sheet <b>4</b>	of <b>31</b>


**Clock Structure**

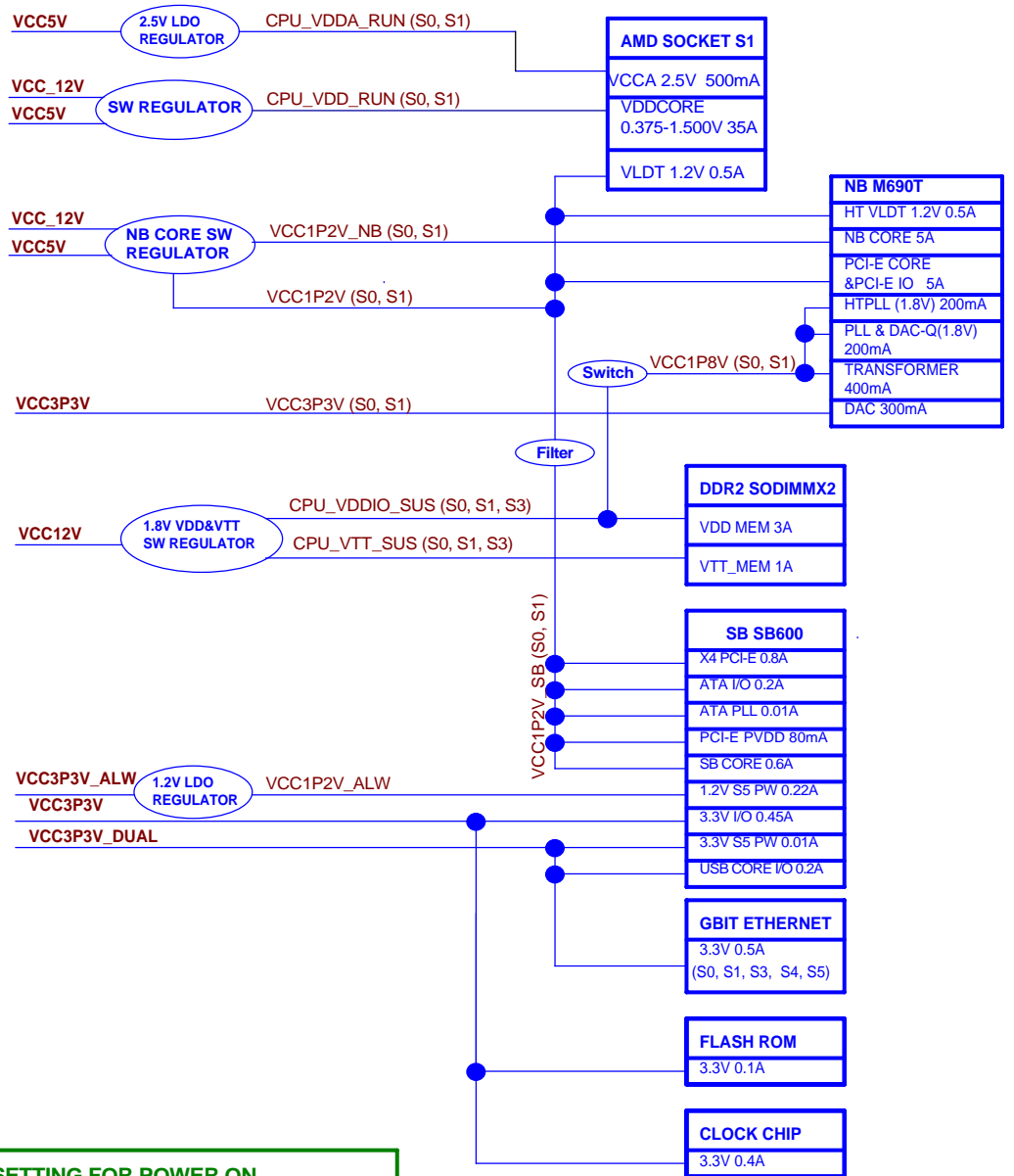
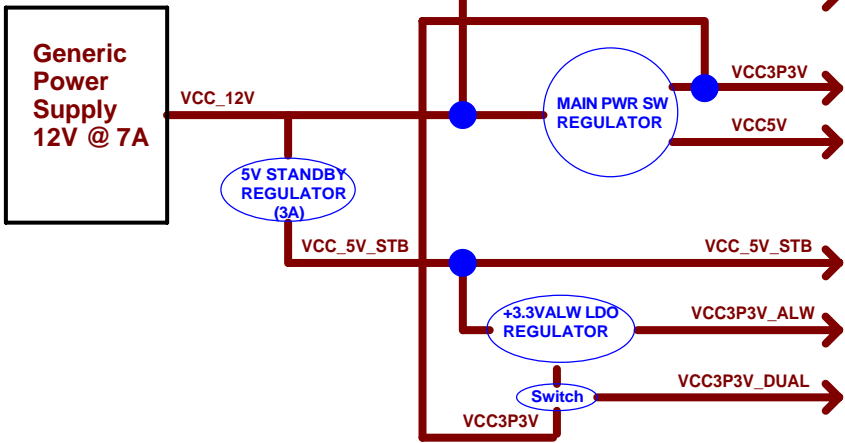
	POWER RAIL		S0	S1	S3	S4	S5
	SOURCE NET	V (NET NAME)					
INPUT VOLTAGE	VCC_12V	+12V	ON	ON	OFF	OFF	OFF
SYSTEM POWER	VCC3P3V_ALW	+3.3V	ON	ON	ON	ON	ON
	VCC1P2V_ALW	+1.2V	ON	ON	ON	ON	ON
	VCC3P3V_DUAL	+3.3V	ON	ON	ON	ON	ON
	VCC5V	+5V	ON	ON	OFF	OFF	OFF
	VCC3P3V	+3.3V	ON	ON	OFF	OFF	OFF
CPU	CPU_VDD_RUN	VID[5:0]	ON	ON	OFF	OFF	OFF
	VCC1P2V	+1.2V	ON	ON	OFF	OFF	OFF
	CPU_VDDA_RUN	+2.5V	ON	ON	OFF	OFF	OFF
CPU & MEMORY	CPU_VDDIO_SUS	+1.8V	ON	ON	ON	OFF	OFF
	CPU_M_VREF_SUS	+0.9V	ON	ON	ON	OFF	OFF
	MEM_M_VREF_SUS	+0.9V	ON	ON	ON	OFF	OFF
	CPU_VTT_SUS	+0.9V	ON	ON	ON	OFF	OFF
RS690T	VCC1P2V_NB	+1.2V (VDDC)	ON	ON	OFF	OFF	OFF
	VCC1P2V	+1.2V (VDDA_12)	ON	ON	OFF	OFF	OFF
	VCC1P2V	+1.2V (VDD_HT)	ON	ON	OFF	OFF	OFF
	VCC1P2V	+1.2V (VDDPLL)	ON	ON	OFF	OFF	OFF
	VCC1P2V	+1.2V (PLLVD12)	ON	ON	OFF	OFF	OFF

	POWER RAIL		S0	S1	S3	S4	S5	
	SOURCE NET	V (NET NAME)						
RS690T	VCC1P8V	+1.8V (PLLVD18)	ON	ON	OFF	OFF	OFF	
	VCC1P8V	+1.8V (LVDDR18,LPVDD)	ON	ON	OFF	OFF	OFF	
	VCC1P8V	+1.8V (VDD_18)	ON	ON	OFF	OFF	OFF	
	VCC1P8V	+1.8V (HTPVDD)	ON	ON	OFF	OFF	OFF	
	VCC1P8V	+1.8V (AVDDI)	ON	ON	OFF	OFF	OFF	
	VCC1P8V	+1.8V (AVDDQ)	ON	ON	OFF	OFF	OFF	
	VCC3P3V	+3.3V (VDDR3,LVDDR33)	ON	ON	OFF	OFF	OFF	
	VCC3P3V	+3.3V (AVDD)	ON	ON	OFF	OFF	OFF	
	SB600	VCC1P2V_SB	+1.2V (VDD)	ON	ON	OFF	OFF	OFF
		VCC1P2V_SB	+1.2V(PCIE_PVDD)	ON	ON	OFF	OFF	OFF
VCC1P2V_SB		+1.2V(PCIE_VDDR)	ON	ON	OFF	OFF	OFF	
VCC1P2V_SB		+1.2V(PLLVD_SATA)	ON	ON	OFF	OFF	OFF	
VCC1P2V_SB		+1.2V(AVDD_SATA)	ON	ON	OFF	OFF	OFF	
VCC1P2V_SB		+1.2V (AVDDCK_1.2V)	ON	ON	OFF	OFF	OFF	
VCC1P2V_ALW		+1.2V (S5_1.2V)	ON	ON	ON	ON	ON	
VCC1P2V_ALW		+1.2V(USN_PHY_1.2V)	ON	ON	ON	ON	ON	
VCC3P3V_DUAL		+3.3V (AVDDC)	ON	ON	ON	ON	ON	
VCC3P3V		+3.3V(XTLVDD_SATA)	ON	ON	OFF	OFF	OFF	
VCC3P3V		+3.3V (VDDQ)	ON	ON	OFF	OFF	OFF	
VCC3P3V		+3.3V (AVDD)	ON	ON	OFF	OFF	OFF	
VCC3.3V_ALW		+3.3V (S5_3.3V)	ON	ON	ON	ON	ON	
VCC3P3V_DUAL		+3.3V (AVDDTX_RX)	ON	ON	ON	ON	ON	
VCC3P3V		+3.3V (AVDDCK_3.3V)	ON	ON	OFF	OFF	OFF	
VCC1P8V		+1.8V (CPU_PWR)	ON	ON	OFF	OFF	OFF	
VCC5V		+5V (V5_VREF)	ON	ON	OFF	OFF	OFF	

POWER ON SEQUENCING REQUIREMENT BY PARTS
<p><b>CPU</b>  PIN(BALL): VDDIO &amp; VTT &amp; VDDA -&gt; VDD -&gt; VLDT  NET NAME: CPU_VDDIO_SUS &amp; CPU_VTT_SUS &amp; CPU_VDDA_RUN -&gt; CPU_VDD_RUN -&gt; VCC1P2V</p>
<p><b>RS690T</b>  PIN(BALL): 3.3V (VDDR3, LVDDR33, AVDD) -&gt; 1.8V DISPLAY AND PLL(PLLVD18, IOPLLVD18, LVDDR18D, LPVDD, AVDDI, AVDDQ, HTPVDD, VDD_18) -&gt; 1.8V MEMORY(VDD_MEM) -&gt; 1.2V PLL (PLLVD12, IOPLLVD12) -&gt; 1.2V VDD  NET NAME: VCC3P3V (VDDR3, LVDDR33, AVDD) -&gt; VCC1P8V (PLLVD18D, IOPLLVD18, LVDDR18D, LPVDD, AVDDI, AVDDQ, HTPVDD, VDD_18) -&gt; MEM_VDDQ (VDD_MEM) -&gt; VCC1P2V (PLLVD12, IOPLLVD12) -&gt; VCC1P2V_NB  THERE ARE NO SPECIFIC REQUIREMENTS FOR THE FOLLOWING 1.2V RAILS: VDD_HT, VDDA_12, AND VDD_PLL</p>
<p><b>SB600</b>  THERE ARE NO SPECIFIC POWER SEQUENCING REQUIREMENTS OTHER THAN 5V VREF AND VDDQ. VDDQ(3.3V) MUST NOT EXCEED V5_VREF BY MORE THAN 0.6V AT ANY TIME DURING RAMP UP, STEADY STATE, OR RAMP DOWN.  NET NAME: VCC5V, VCC3P3V -&gt; VCC1P2V_SB</p>

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PID	42504	Rev	0.5
Size	Custom	Date:	Tuesday, March 13, 2007
Sheet	5	of	31



PCI DEVICES IRQ TABLE				
DEVICE	IDSEL#	REQ/GNT#	PCI INT	CLOCK
M690T VGA	N/A	N/A	A	
SB600	AD31(INT)	N/A	N/A	
ATA	AD31	N/A	A	INT
AC97/HD	AD31	N/A	B	INT
USB	AD30	N/A	D	INT

SMBUS TABLE		
SOURCE	BALL(PIN) NAME	LINKED DEVICES
M690T	DACSCL/DACSDA	CRT
	I2C_CLK/I2C_DATA	LVDS
SB600	SCL0/SDA0	SO-DIMM / CLK_GEN / THERM_SENSOR
	SCL1/SDA1	GBIT ETHERNET

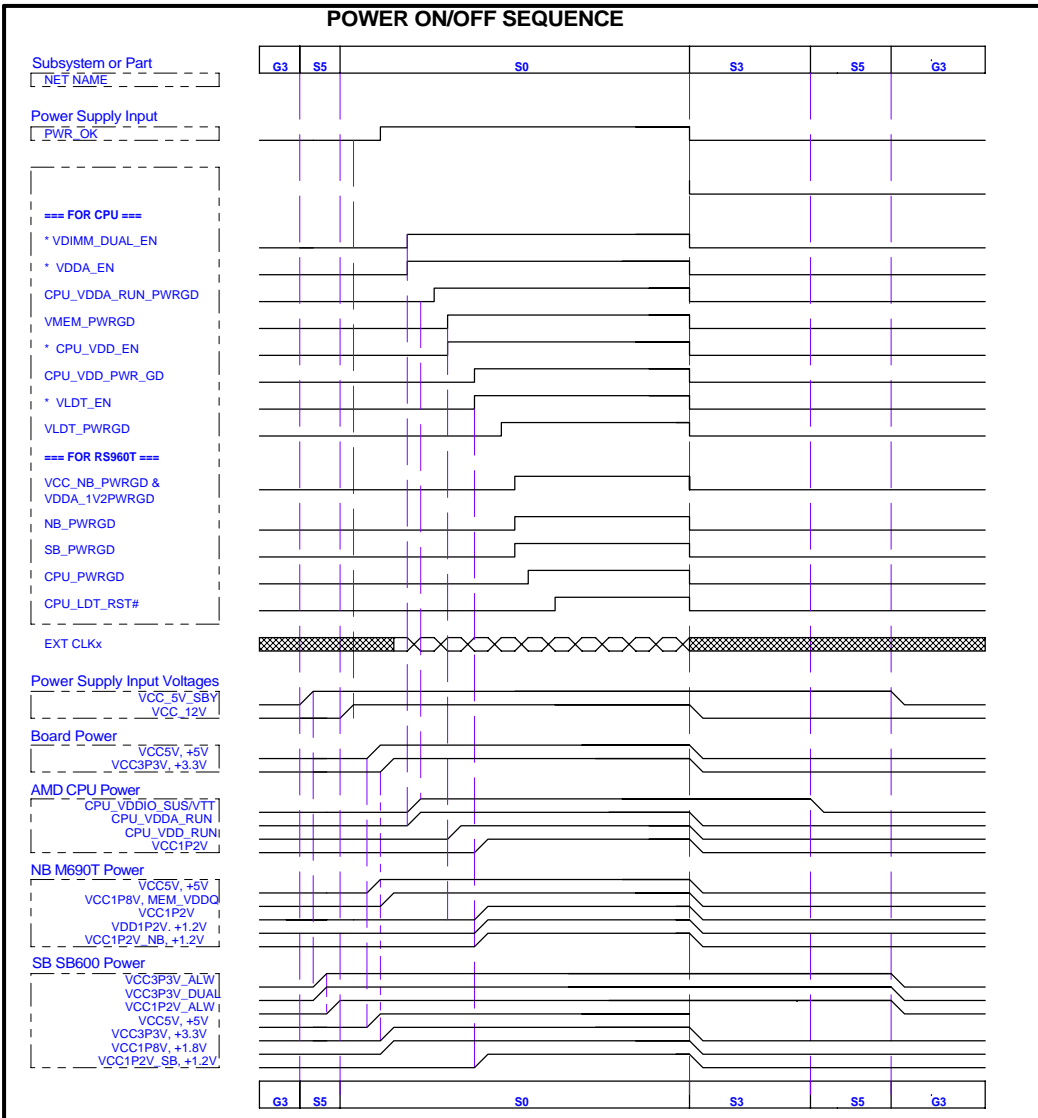
DEFAULT JUMPER SETTING FOR POWER ON		
JUMPER	DEF.	FUNCTION
JU5	1-2	CMOS NORMAL MODE OR CLEAR CMOS
JU7	1-2	SPI BIOS PROGRAMMING SELECTION

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PID: 42504 | Rev: 0.5  
Size: Custom | Date: Tuesday, March 13, 2007 | Sheet: 6 of 31

### POWER ON/OFF SEQUENCE

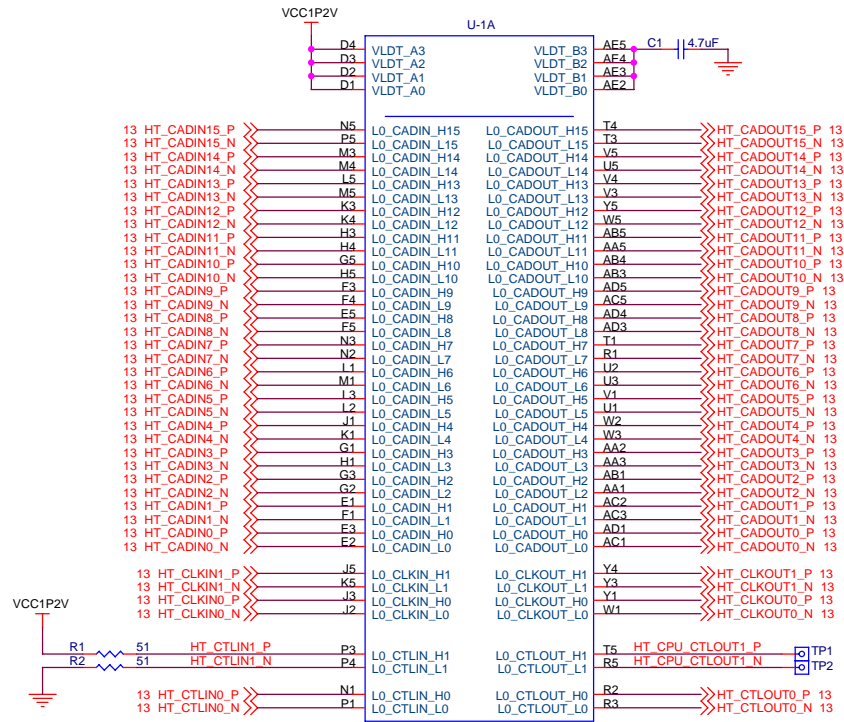


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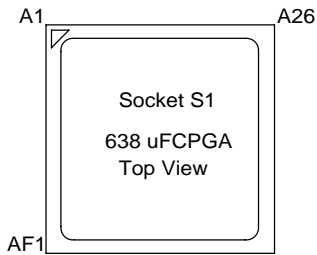
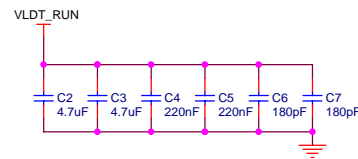
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Size <b>Custom</b>	Sheet <b>7</b> of <b>31</b>		

**Reset and Voltage Sequence**

DESIGN NOTE: VLDT\_Ax or VLDT\_Bx can be connected to VCC1P2V. Layout considerations should decide which group is connected to VCC1P2V. If VLDT\_Ax pins are connected to VCC1P2V then VLDT\_Bx pins should be connected to a single 4.7uF CAP. Conversely, if VLDT\_Bx pins are connected to VCC1P2V then VLDT\_Ax pins should be connected to a single 4.7uF CAP.



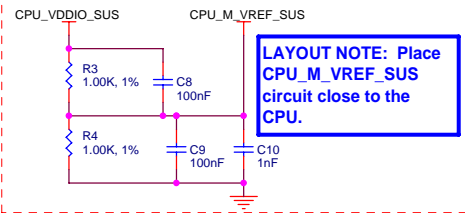
Socket S1 Processor



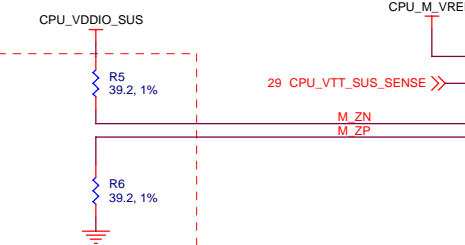
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PID <b>42504</b>	Rev <b>0.5</b>		
Size Custom	Date: <b>Tuesday, March 13, 2007</b>	Sheet <b>8</b>	of <b>31</b>





**LAYOUT NOTE:** Place CPU\_M\_VREF\_SUS circuit close to the CPU.

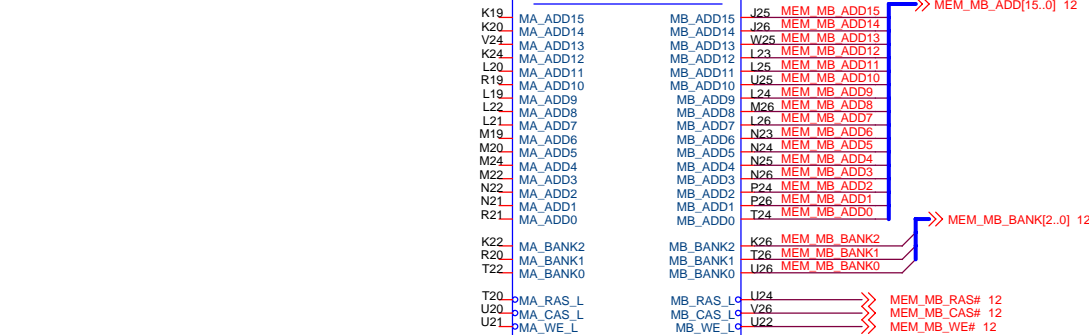


**LAYOUT NOTE:** Keep trace to resistors less than 1.5" from CPU pin.

29 CPU\_VTT\_SUS\_SENSE >>>

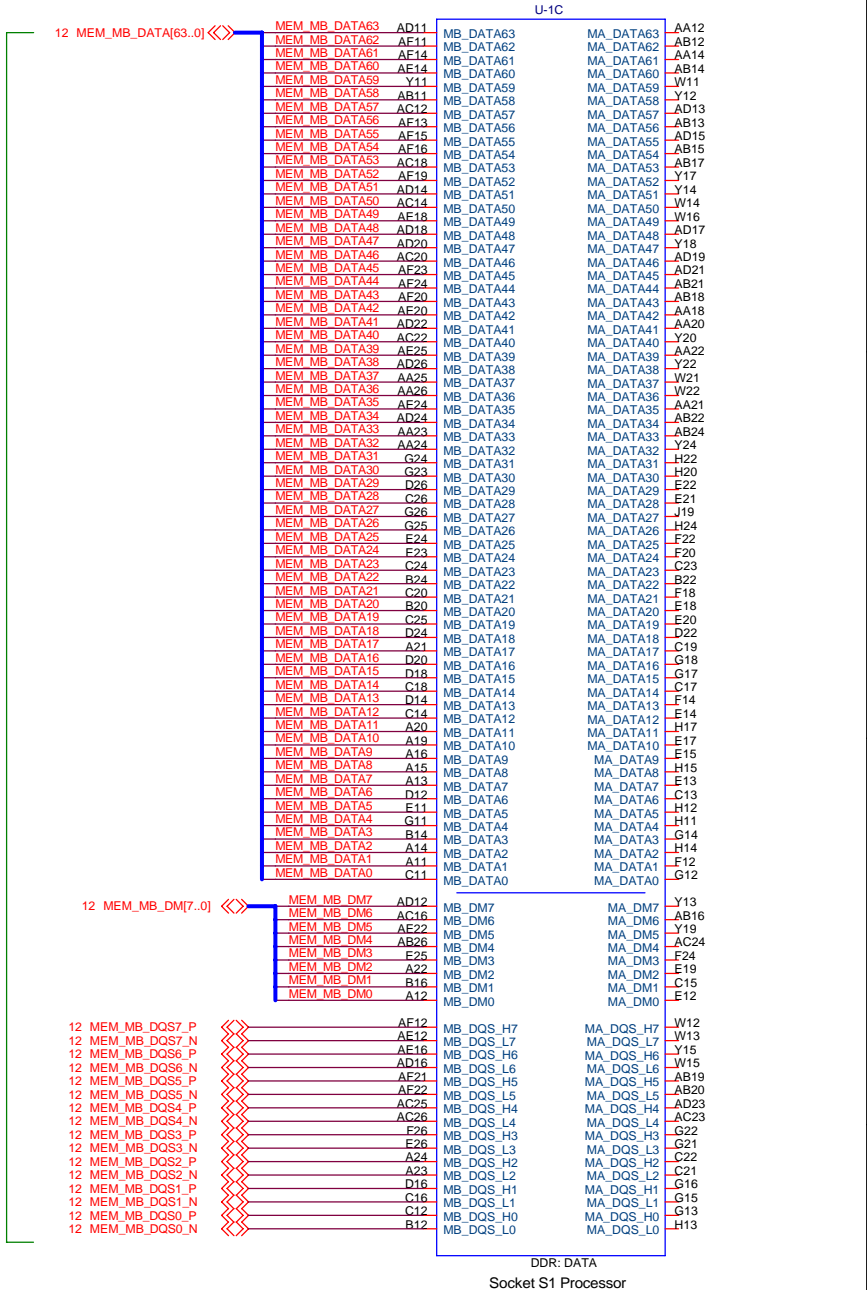
12 MEM\_MB\_CS1# <<<  
12 MEM\_MB\_CS0# <<<

12 MEM\_MB\_CKE1 <<<  
12 MEM\_MB\_CKE0 <<<



DDR II CMD/CTRL/CLK Socket S1 Processor

**DESIGN NOTE:** Reverse type SODIMM connector should be used to ease the layout with channel B signals on the component side of PCB.



DDR: DATA Socket S1 Processor

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**DESIGN NOTE: Thermal monitoring using internal hardware cannot be used at this time. Must use thermal diode and external hardware.**

**LAYOUT NOTE: Keep trace to resistors less than 1.5" from CPU pin.**

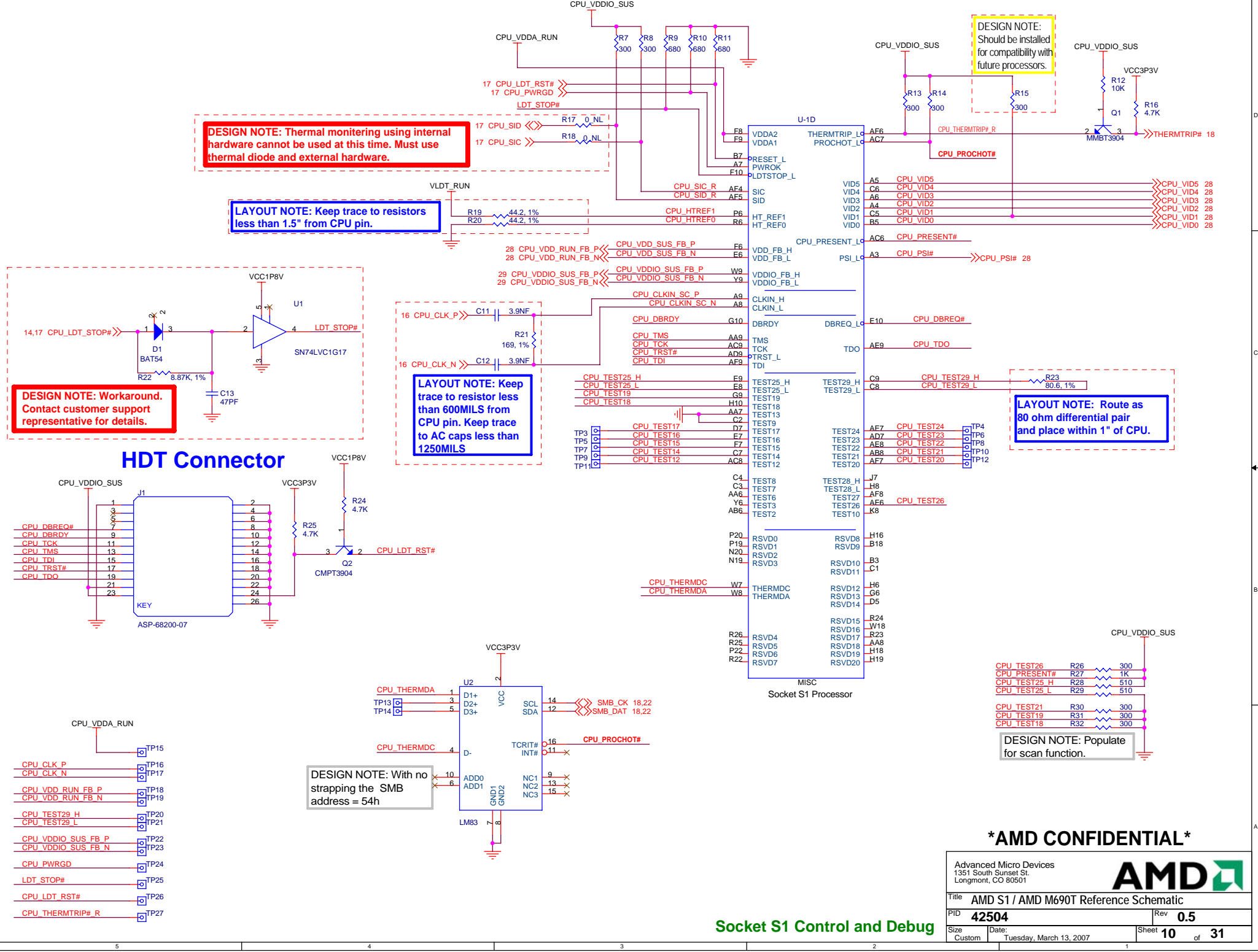
**DESIGN NOTE:** Should be installed for compatibility with future processors.

**DESIGN NOTE: Workaround.** Contact customer support representative for details.

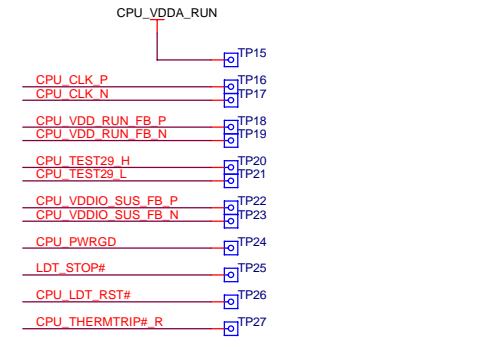
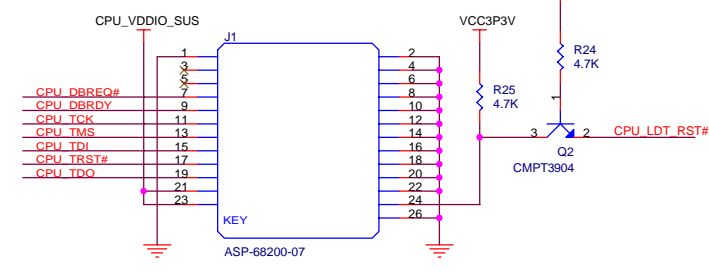
**LAYOUT NOTE: Keep trace to resistor less than 600MILS from CPU pin. Keep trace to AC caps less than 1250MILS**

**LAYOUT NOTE: Route as 80 ohm differential pair and place within 1" of CPU.**

**DESIGN NOTE: With no strapping the SMB address = 54h**



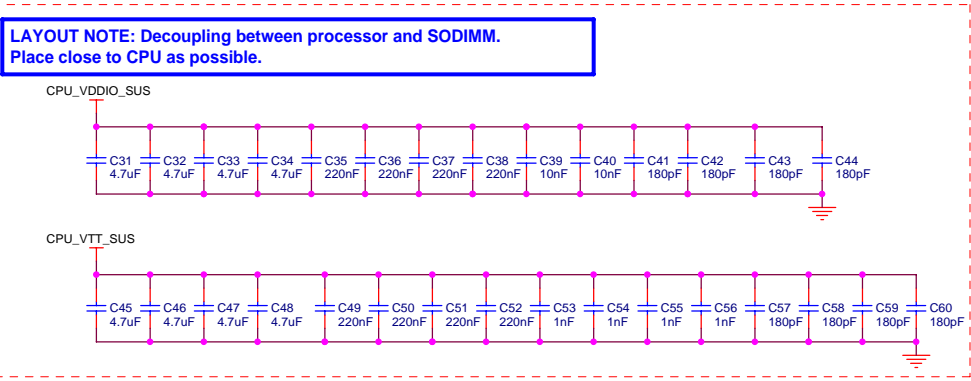
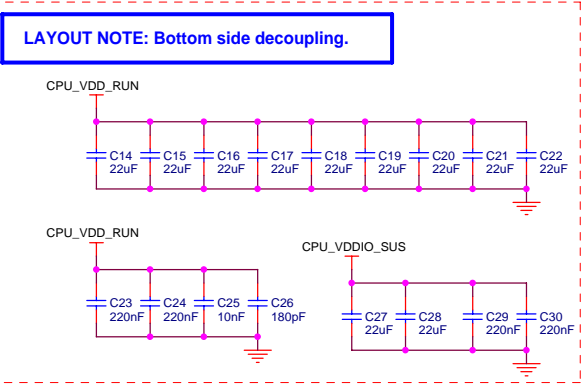
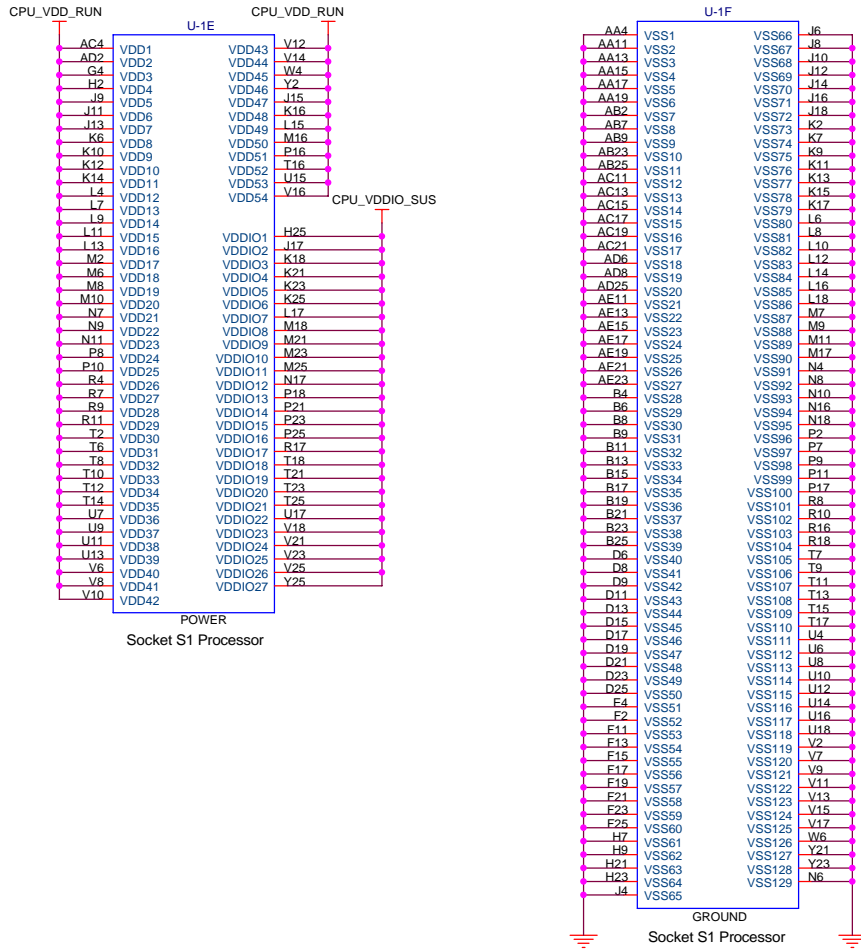
**HDT Connector**



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 PID: 42504 Rev: 0.5  
 Size: Custom Date: Tuesday, March 13, 2007 Sheet: 10 of 31

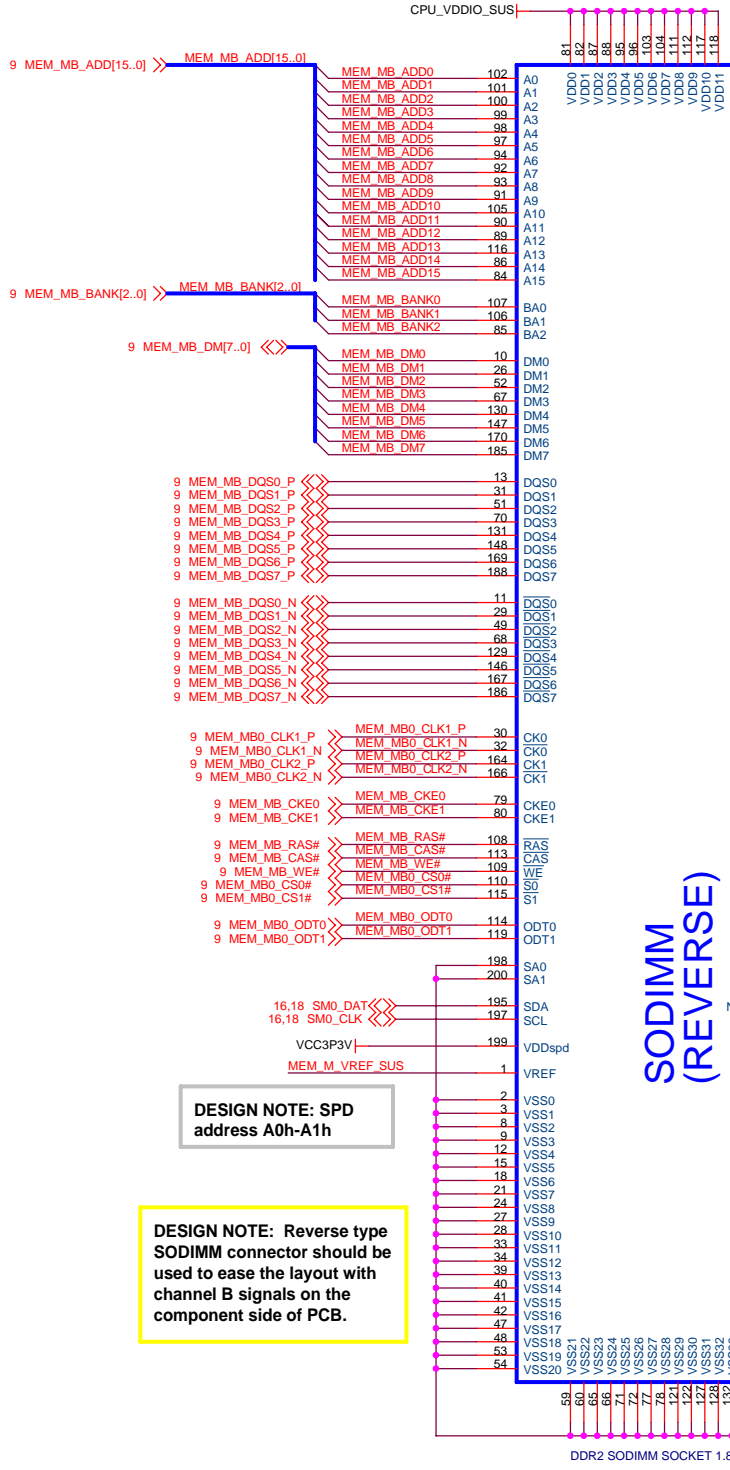


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Title	AMD S1 / AMD M690T Reference Schematic
PID	<b>42504</b>
Rev	<b>0.5</b>
Size	Custom
Date	Tuesday, March 13, 2007
Sheet	<b>11</b> of <b>31</b>

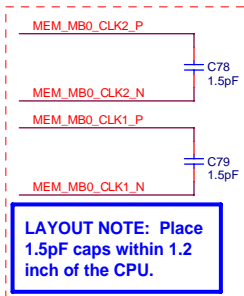
**Socket S1 Power and Ground**



**SODIMM (REVERSE)**

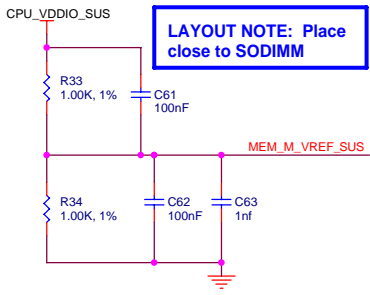
**DESIGN NOTE: SPD address A0h-A1h**

**DESIGN NOTE: Reverse type SODIMM connector should be used to ease the layout with channel B signals on the component side of PCB.**



**LAYOUT NOTE: Place 1.5pF caps within 1.2 inch of the CPU.**

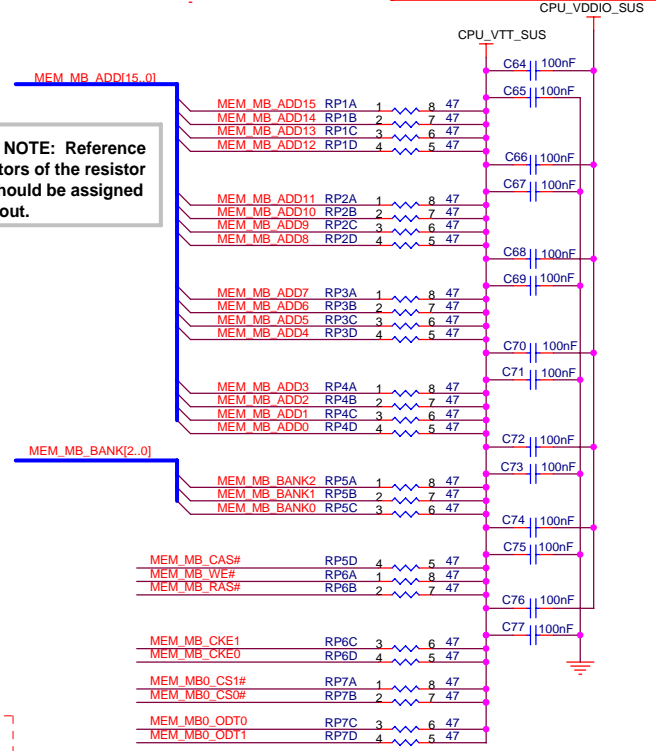
**MEM\_VREF\_SUS**



**LAYOUT NOTE: Place close to SODIMM**

**DESIGN NOTE: CPU\_VTT\_SUS should be decoupled to CPU\_VDDIO\_SUS and ground with one 0.1uF cap in a 0603 X7R package for each Rpack.**

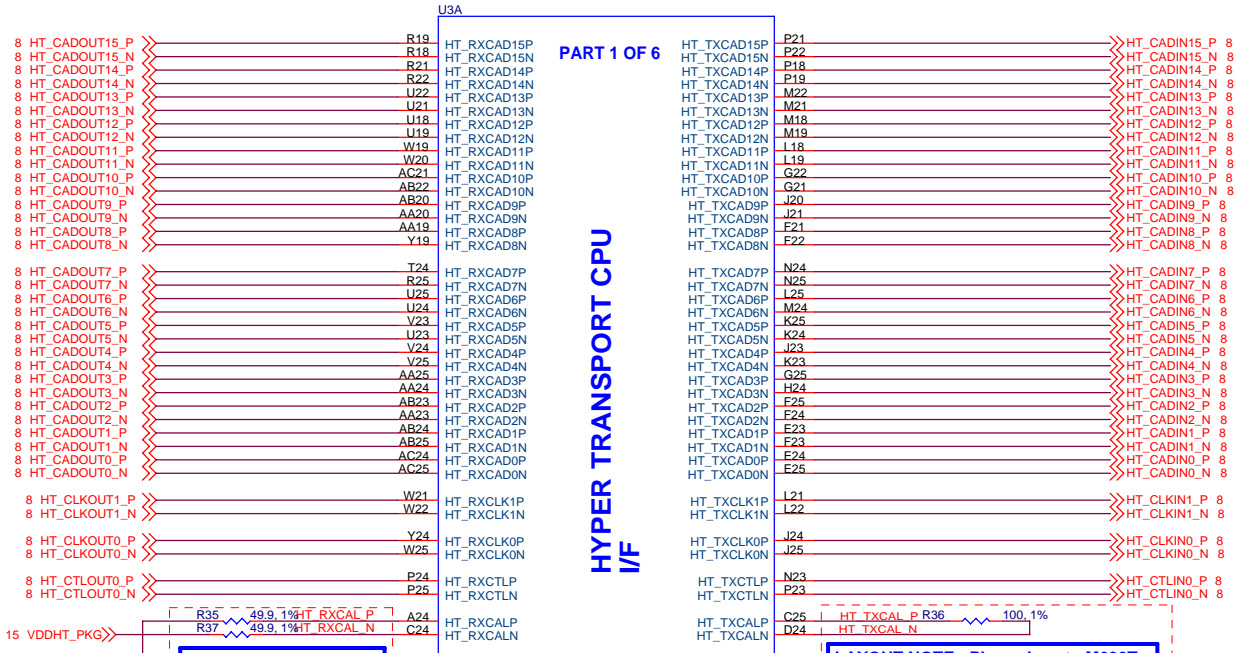
**DESIGN NOTE: Reference designators of the resistor packs should be assigned after layout.**



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**SODIMM DDR2**



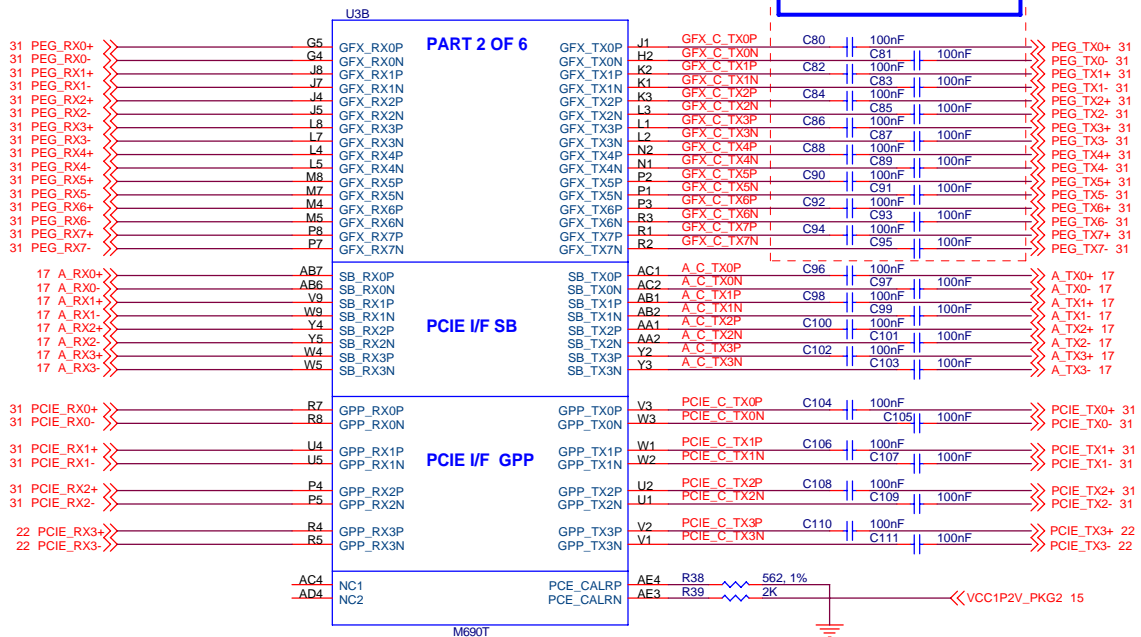
PART 1 OF 6

HYPER TRANSPORT CPU I/F

LAYOUT NOTE: Place close to M690T.

LAYOUT NOTE: Place close to M690T.

LAYOUT NOTE: If signals are passing through a connector, place caps close to connector. If not, then place close to M690T.



PART 2 OF 6

PCIe I/F SB

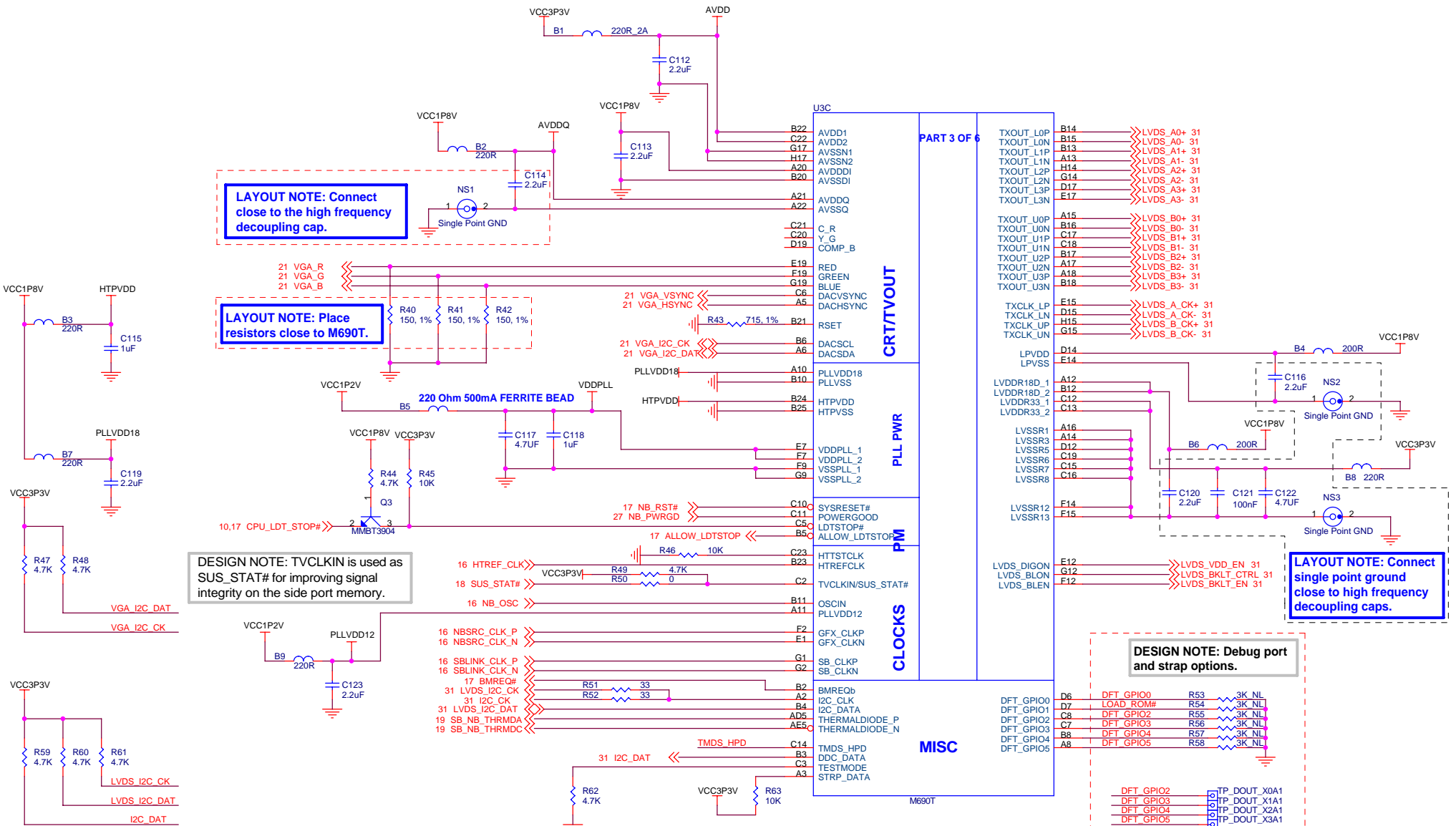
PCIe I/F GPP

AMD M690T HyperTransport™, PCIe™, and PCIe Graphics

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 PID: 42504 Rev: 0.5  
 Size: Custom Date: Tuesday, March 13, 2007 Sheet: 13 of 31

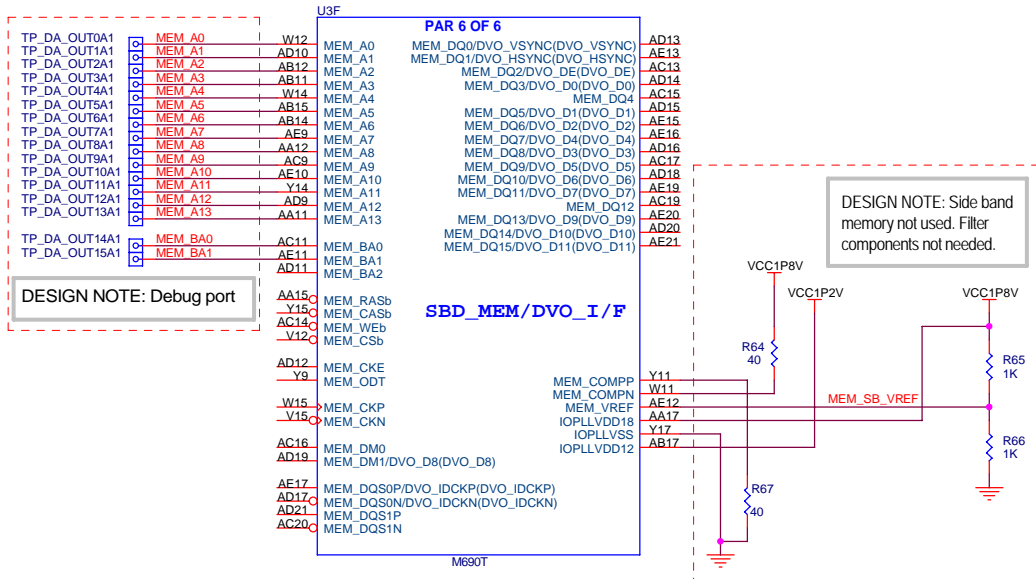
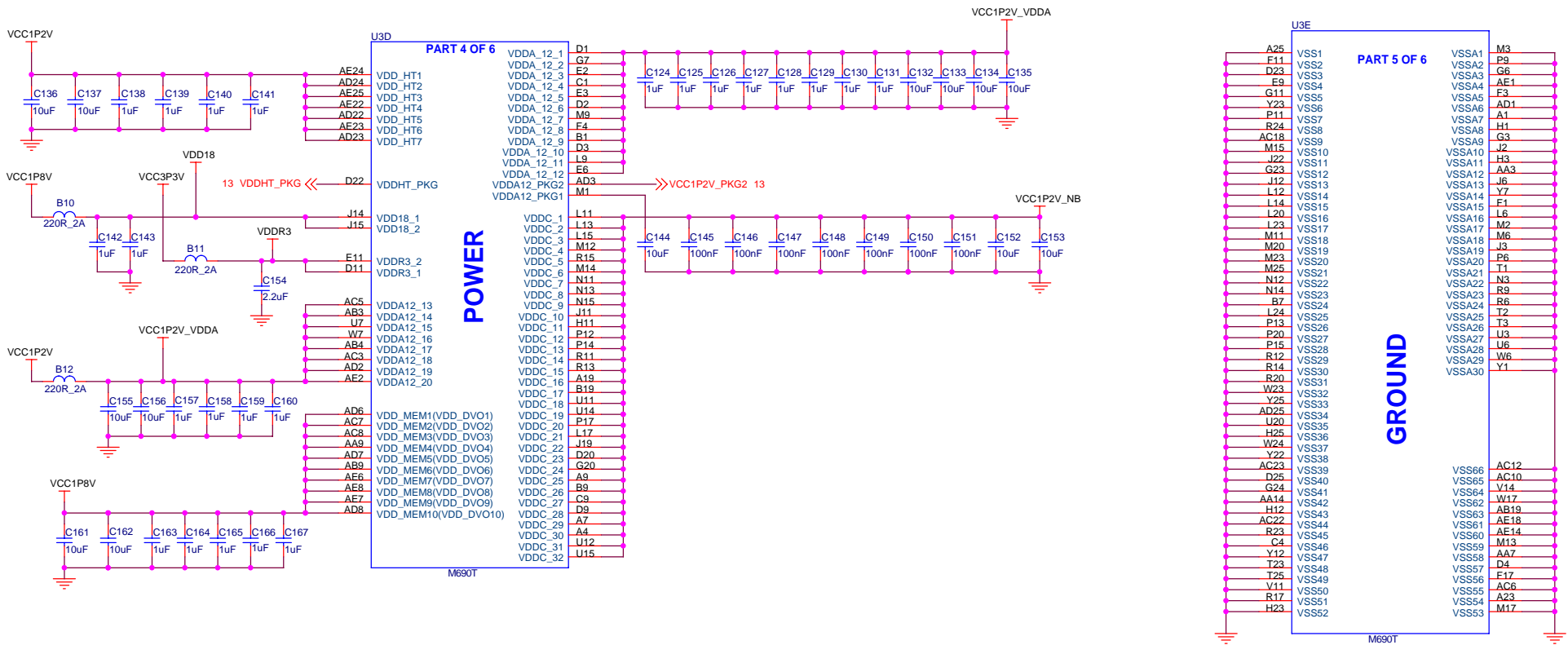


M690T Strapping Table				
	DFT_GPIO1	DFT_GPIO0	DFT_GPIO[4:2]	DFT_GPIO5
<b>PULL HIGH</b> (internally pulled high)	Use Hardware values <b>REQUIRED SET</b>	Memory side port not available <b>REQUIRED SET</b>	These pin straps are used to configure PCIe General Purpose Port (GPP) mode: 111: Register defined configuration, register default setting to Config E 101: Config A - 4-0-0-0-0 101: Config B - 4-4 100: Config C - 4-2-2 011: Config D - 4-2-1-1 010: Config E - 4-1-1-1	Enable debug bus via the memory IO pads, if available in the package. Use default values. <b>REQUIRED SET</b>
<b>PULL LOW</b>		Memory side port available	All other setting are register defined configuration, register default setting to Config E	Use the memory data bus to output the debug bus

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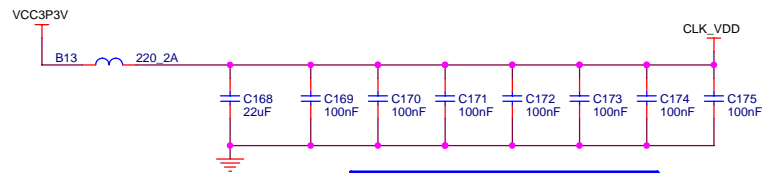
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 PID: **42504** Rev: **0.5**  
 Size: Custom Date: Tuesday, March 13, 2007 Sheet: **14** of **31**



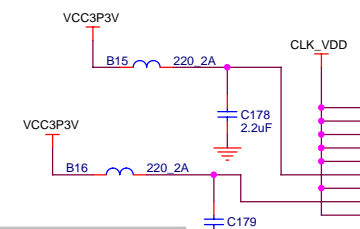
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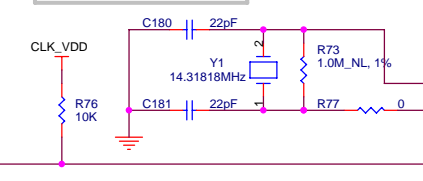
Title		AMD S1 / AMD M690T Reference Schematic	
PID	42504	Rev	0.5
Size	Custom	Date:	Tuesday, March 13, 2007
Sheet	15	of	31



**LAYOUT NOTE:** Place decoupling caps close to the power pins.



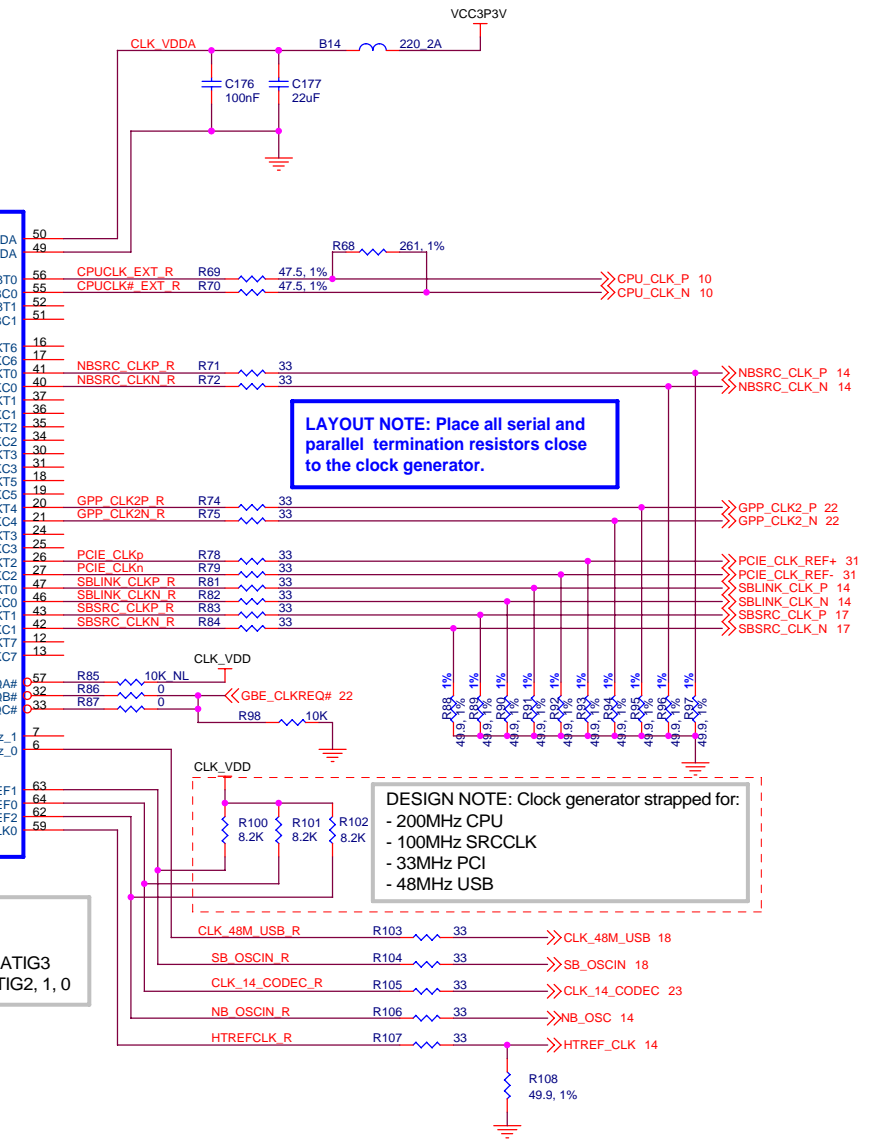
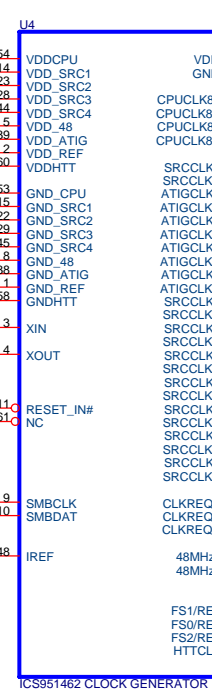
**DESIGN NOTE:** Parallel Resonance Crystal.



**DESIGN NOTE:** Spread spectrum is controlled by software using the SM Bus interface. See the datasheet for details.

**DESIGN NOTE:**  
 $I_{oh} = 5 * I_{ref} (2.32mA)$   
 $V_{oh} = 0.71V @ 60 \text{ ohm}$

**DESIGN NOTE:**  
 CLKREQA# CONTROL SRC7, 6, 5  
 CLKREQB# CONTROL SRC4, 3, 2, ATIG3  
 CLKREQC# CONTROL SRC1, 0, ATIG2, 1, 0



**LAYOUT NOTE:** Place all serial and parallel termination resistors close to the clock generator.

**DESIGN NOTE:** Clock generator strapped for:  
 - 200MHz CPU  
 - 100MHz SRCCLK  
 - 33MHz PCI  
 - 48MHz USB

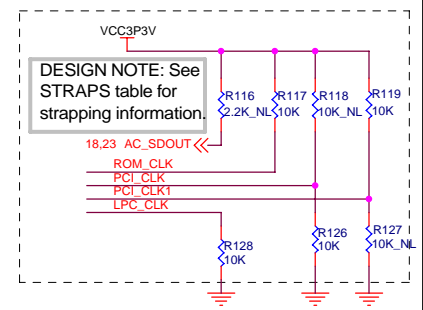
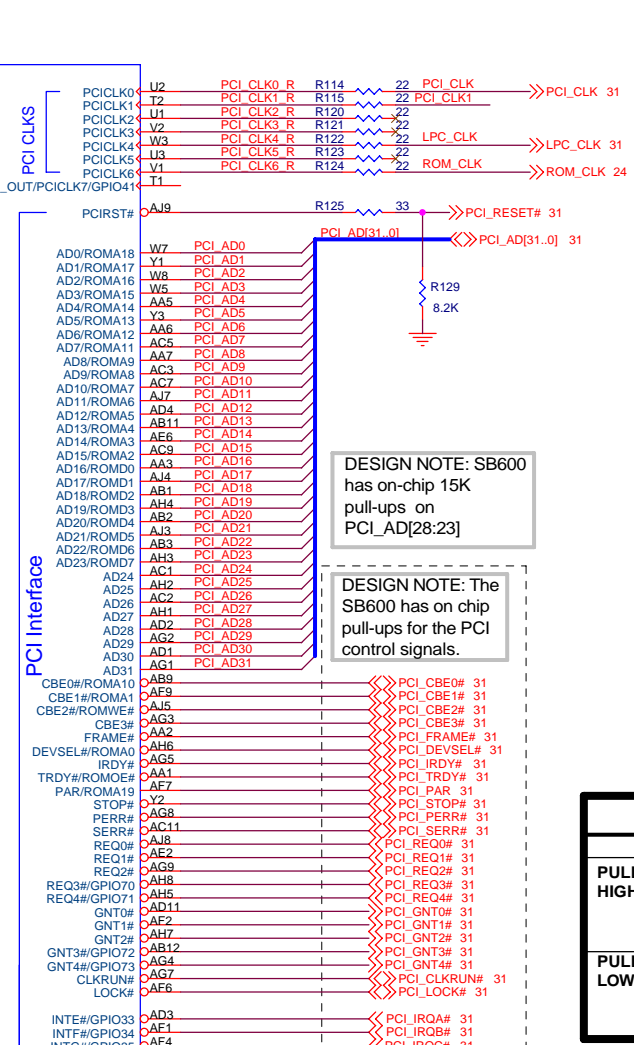
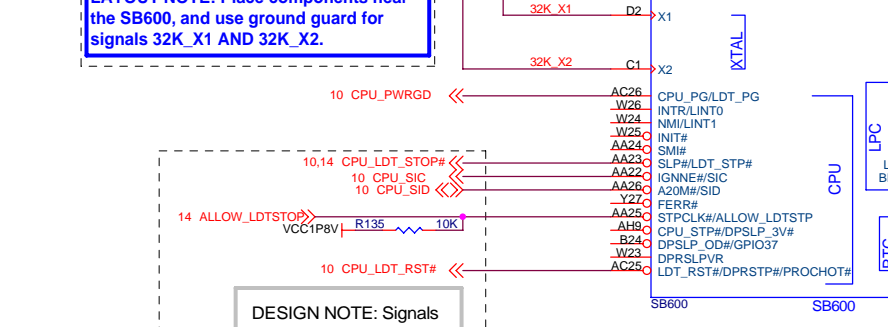
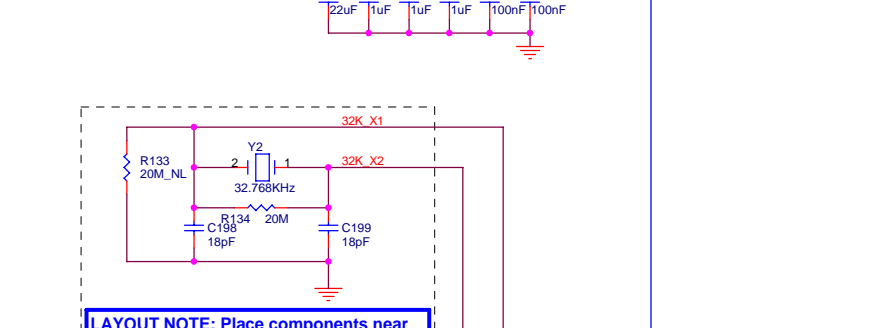
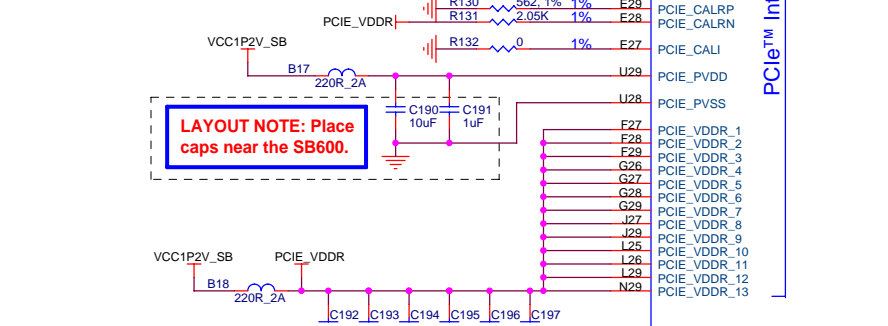
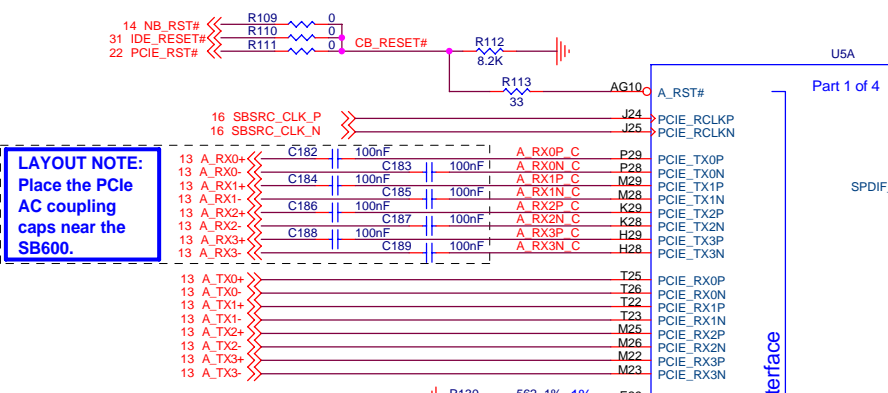
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Title	AMD S1 / AMD M690T Reference Schematic
PID	42504
Rev	0.5
Size	Custom
Date:	Tuesday, March 13, 2007
Sheet	16 of 31

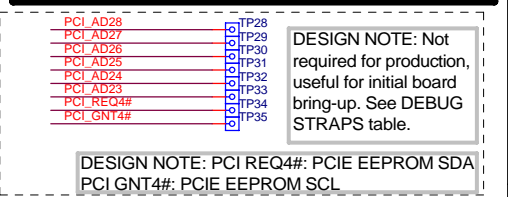
**Clock Generator**



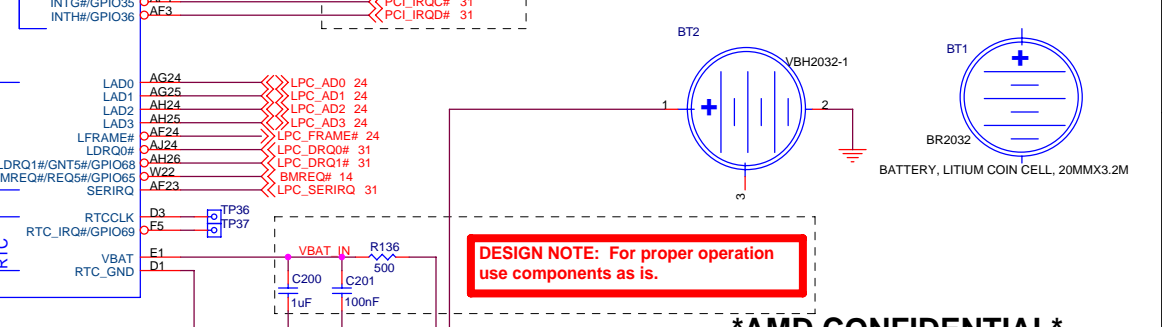


	AC_SDOU	LPC_CLK (PCI_CLK4)	ROM_CLK (PCI_CLK6)	PCI_CLK (PCI_CLK1)
<b>PULL HIGH</b>	USE DEBUG STRAPS	USE INT. PLL48.	CPU IF= AMD REQUIRED SET	ROM TYPE: * H, H = PCI ROM H, L = SPI ROM
<b>PULL LOW</b>	IGNORE DEBUG STRAPS REQUIRED SET	USE EXT. 48MHZ REQUIRED SET	CPU IF= OTHER	L, H = LPC ROM REQUIRED SET L, L = FWH ROM

\* PCI ROM is not supported for SB600 Rev A21 or later.



	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
<b>PULL HIGH</b>	USE LONG RESET REQUIRED SET	USE PCI PLL REQUIRED SET	USE ACPI BCLK REQUIRED SET	USE IDE PLL REQUIRED SET	USE DEFAULT PCIE STRAPS REQUIRED SET	BOOTFAIL TIMER DISABLED REQUIRED SET
<b>PULL LOW</b>	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOTFAIL TIMER ENABLED



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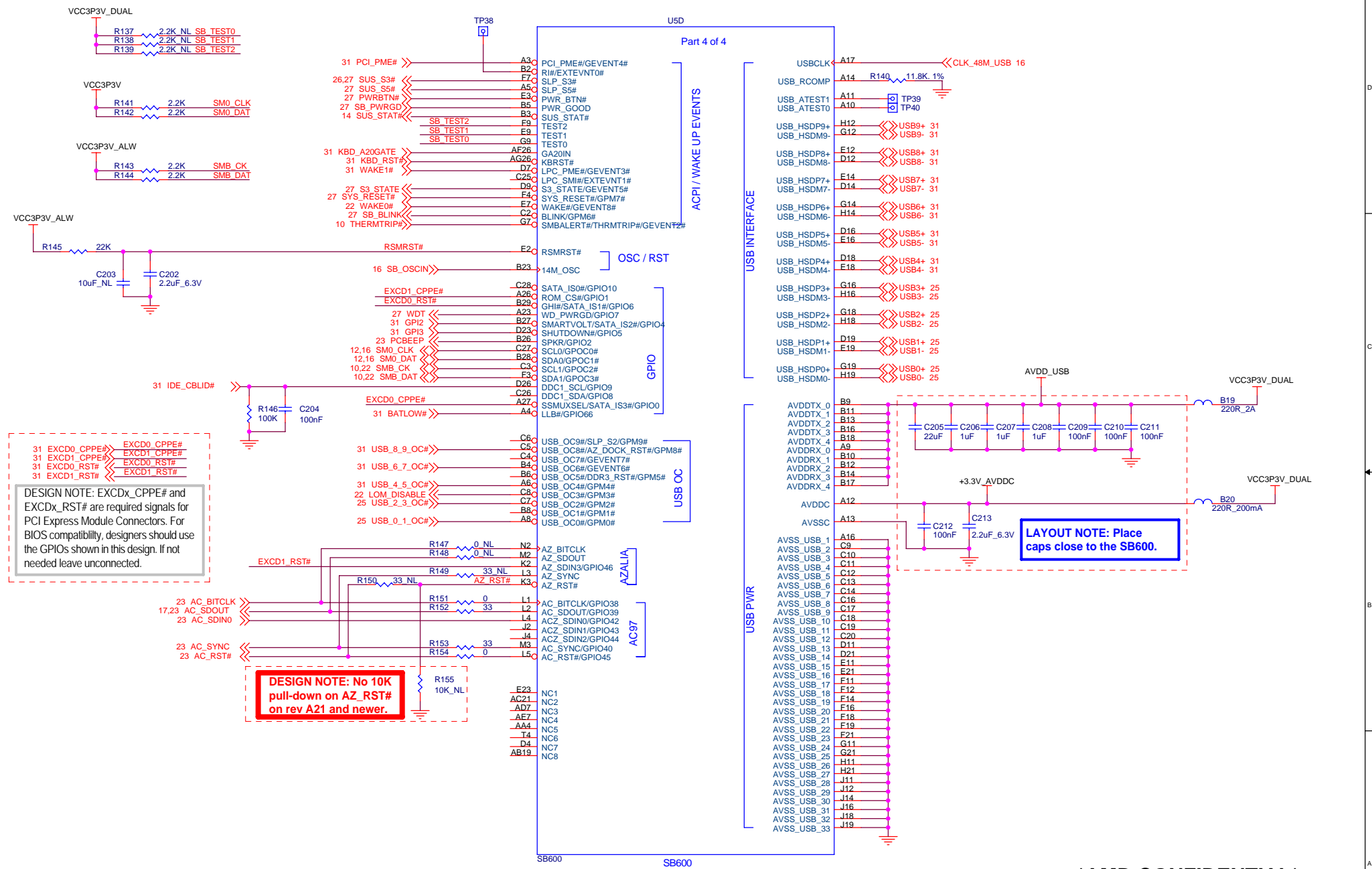
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**AMD**

Title: AMD S1 / AMD M690T Reference Schematic  
PID: 42504  
Rev: 0.5

Size: Custom Date: Tuesday, March 13, 2007 Sheet: 17 of 31

**SB600 PCIe™, PCI, LPC, straps, and CPU control**



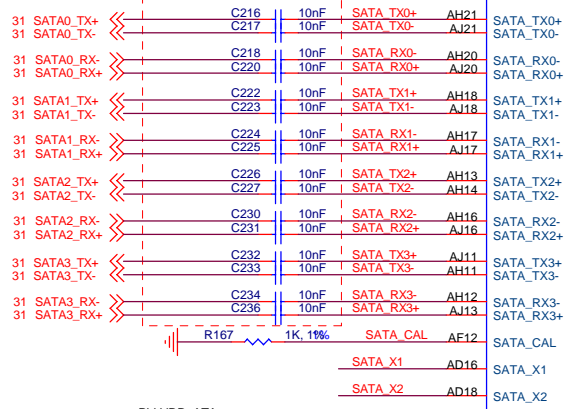
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Title: AMD S1 / AMD M690T Reference Schematic  
PID: 42504 Rev: 0.5  
Size: Custom Date: Tuesday, March 13, 2007 Sheet: 18 of 31

**SB600 ACPI, GPIO, USB, and Audio Interfaces**

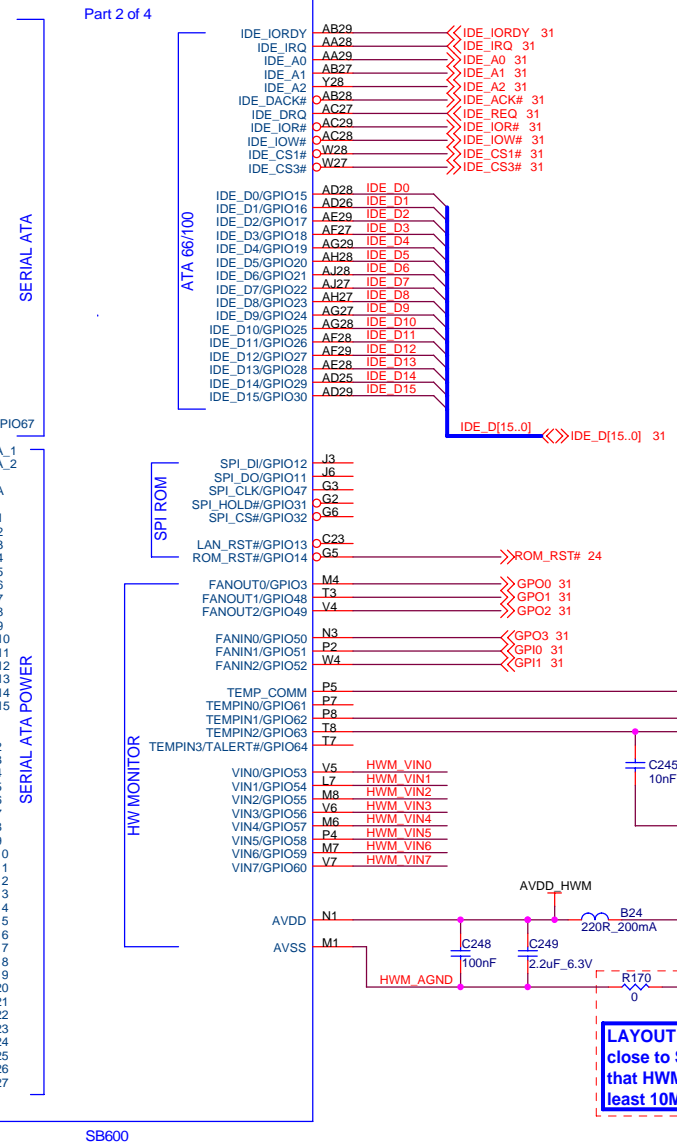
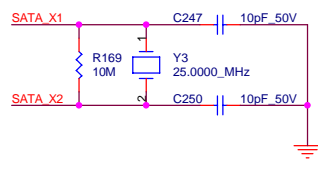
**LAYOUT NOTE: Place SATA AC coupling caps near the SB600.**



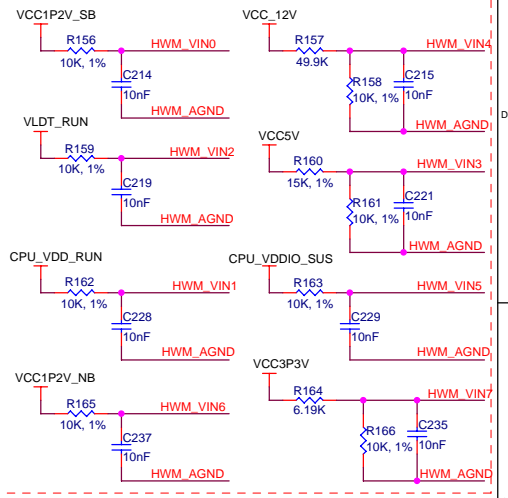
**LAYOUT NOTE: Place cap near the SB600 ball.**

**LAYOUT NOTE: Place cap near the SB600 ball.**

**DESIGN NOTE: AVDD\_SATA voltage requirements are different on revisions prior to rev A21. See your field service representative for details.**



**DESIGN NOTE: Hardware monitoring pins HWM\_VIN[7:0] are not validated and not recommended at this time.**



**DESIGN NOTE: TEMPIN[2:0] pins are not validated and not recommended for use.**

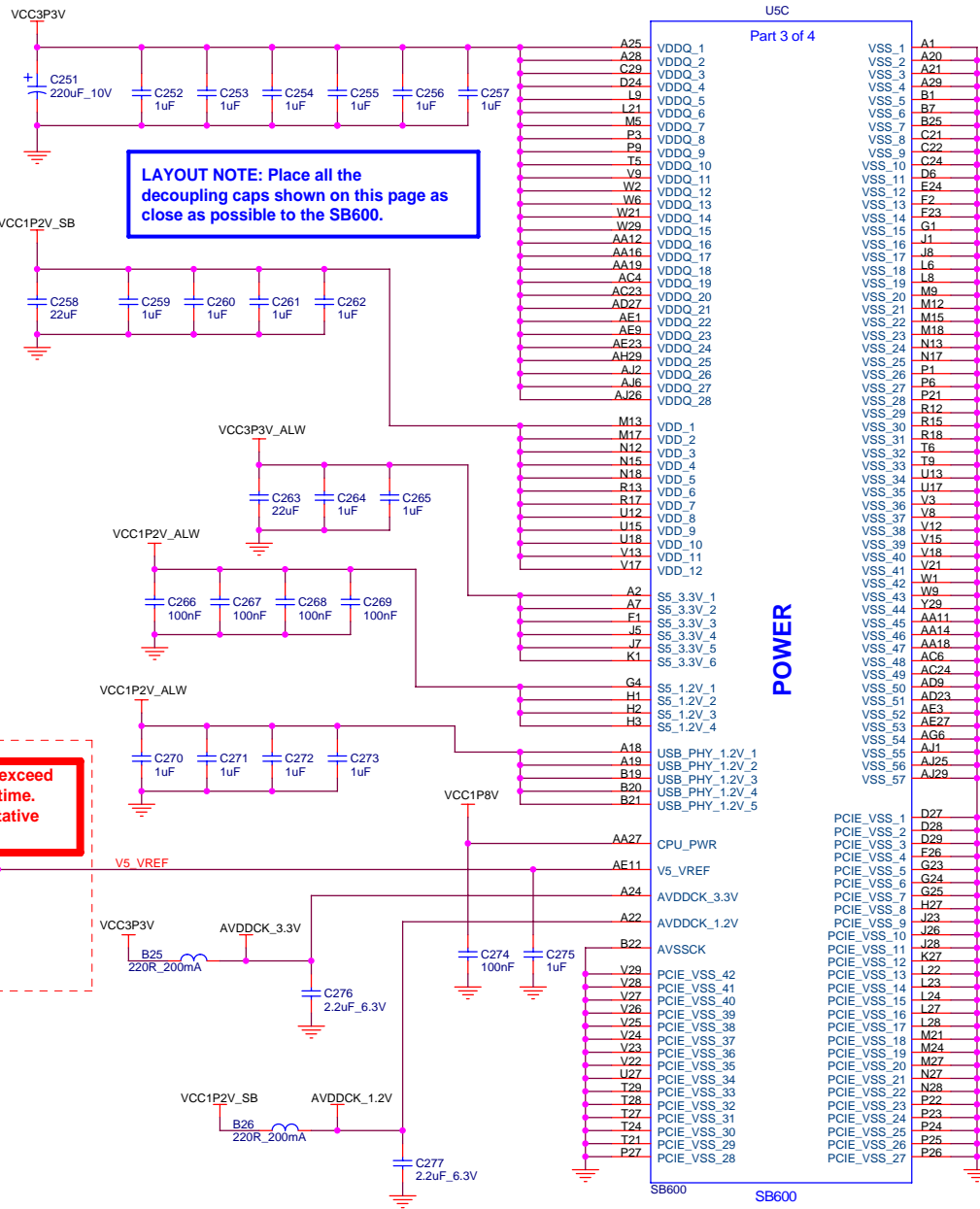
**LAYOUT NOTE: Place resistor close to SB600 and make sure that HWM\_AGNND TRACE is at least 10MIL wide.**

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Title: AMD S1 / AMD M690T Reference Schematic  
PID: 42504  
Rev: 0.5  
Date: Tuesday, March 13, 2007  
Sheet: 19 of 31

**SB600 SATA, IDE, SPI, and Hardware Management Interfaces**



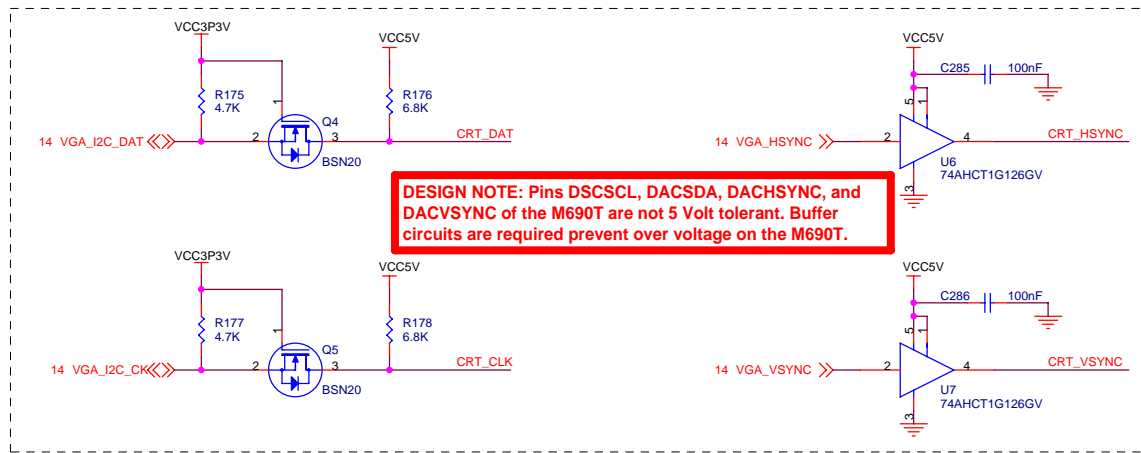
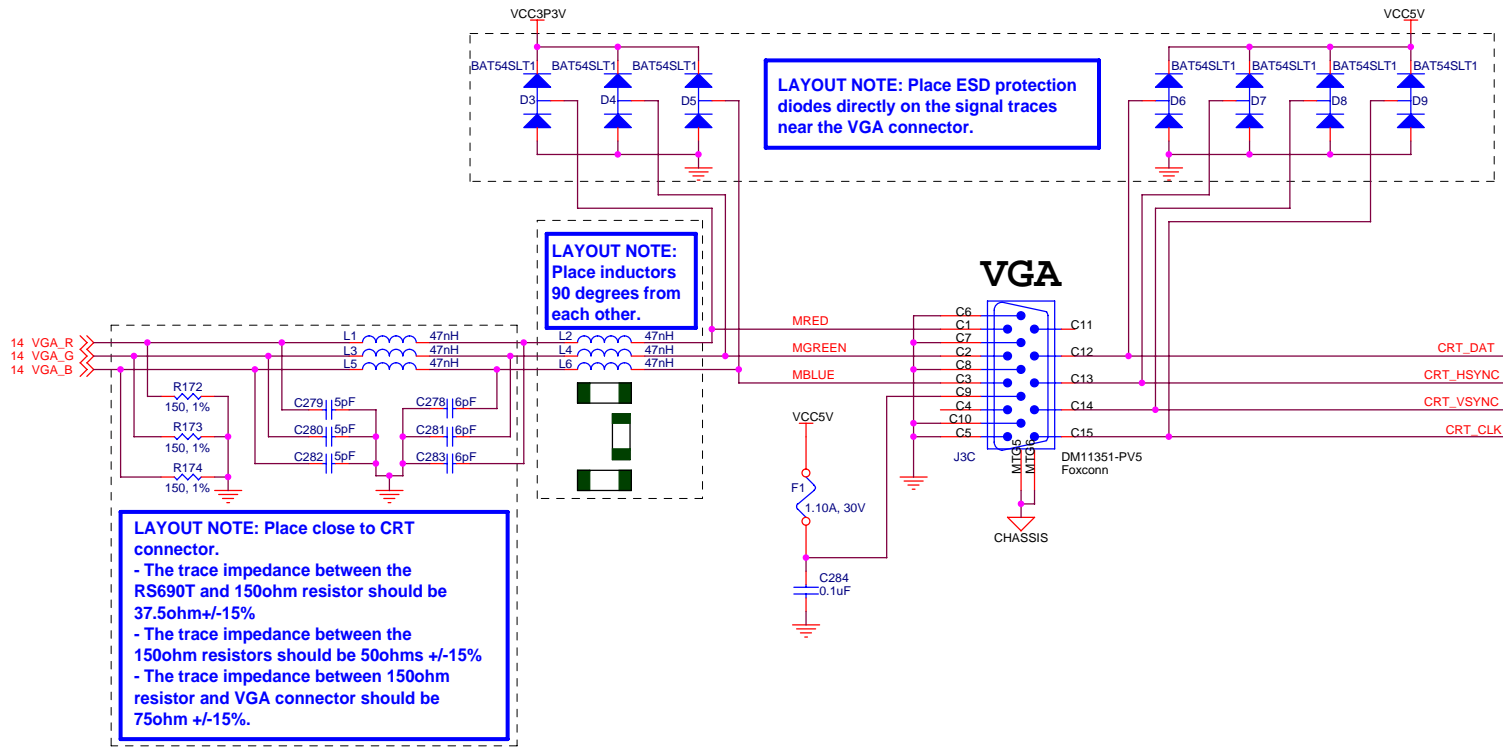
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Title: **AMD S1 / AMD M690T Reference Schematic**  
 PID: **42504** Rev: **0.5**  
 Size: Custom Date: Tuesday, March 13, 2007 Sheet: **20** of **31**

**SB600 Power**



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Advanced Micro Devices 1351 South Sunset St. Longmont, CO 80501		<b>AMD</b>	
Title	AMD S1 / AMD M690T Reference Schematic		
PID	<b>42504</b>	Rev	<b>0.5</b>
Size	Custom	Date:	Tuesday, March 13, 2007
Sheet	<b>21</b>	of	<b>31</b>

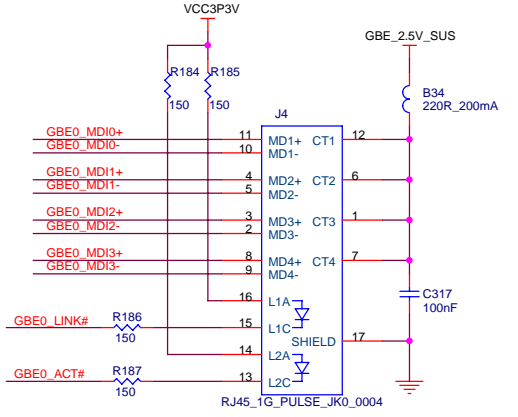
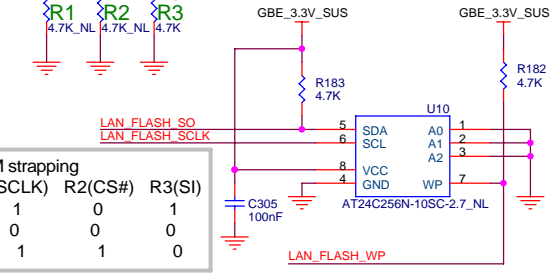
**CRT Connector**

DESIGN NOTE: Contact Broadcom for implementation details on the BCM5787.



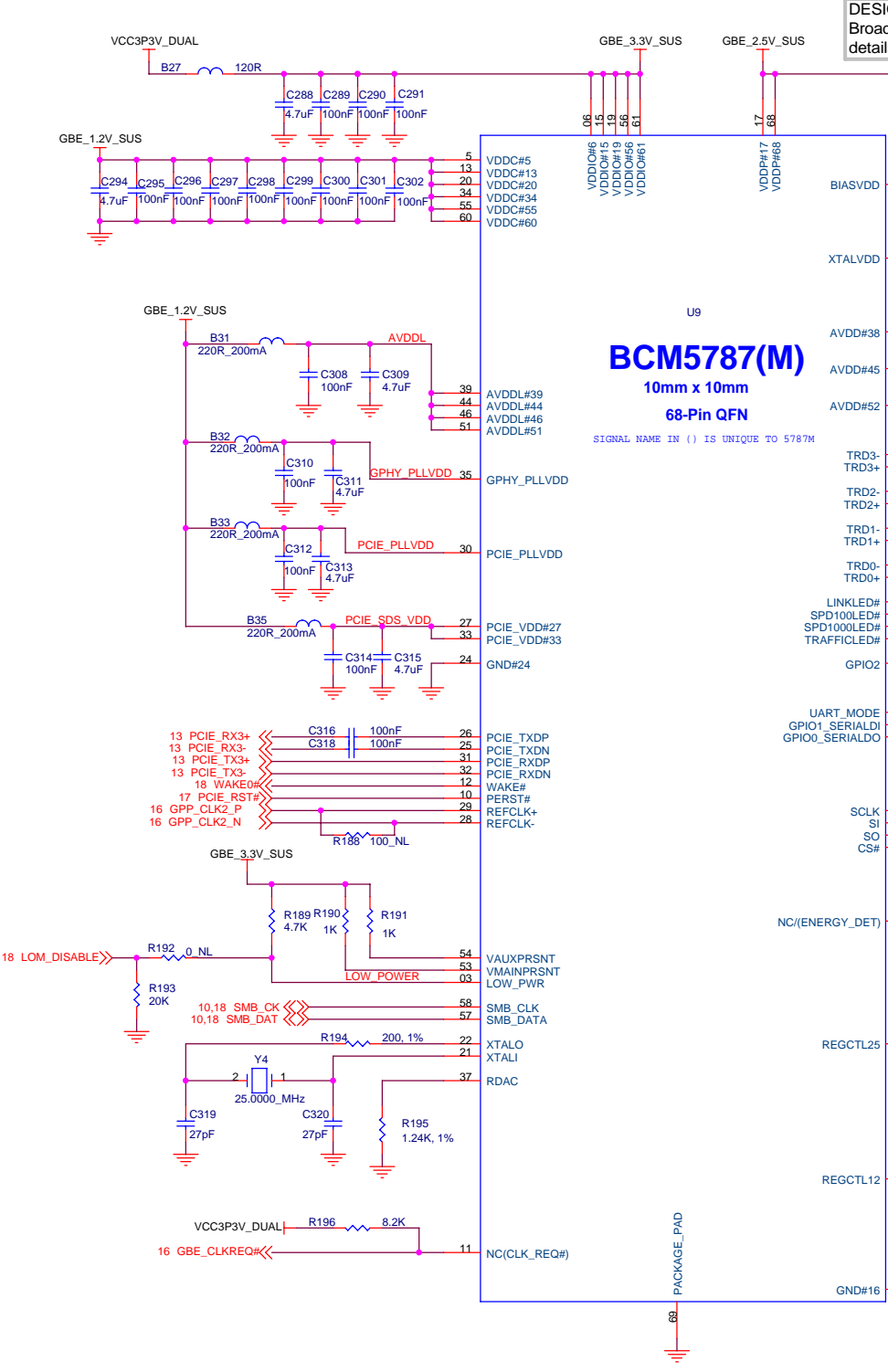
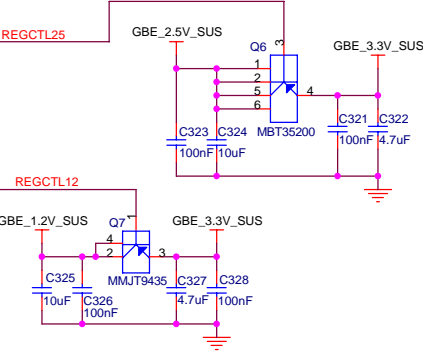
DESIGN NOTE: NVRAM strapping

	R1(SCLK)	R2(CS#)	R3(SI)
EEPROM 24C64/256	1	0	1
MICROCHIP	0	0	0
ATMEL AT45DB011B	1	1	0



DESIGN NOTE: Verify with Ethernet controller supplier for best choice of connector and connectivity.

DESIGN NOTE: Contact Broadcom for implementation details on pin ENERGY\_DET.



**BCM5787(M)**  
10mm x 10mm  
68-Pin QFN

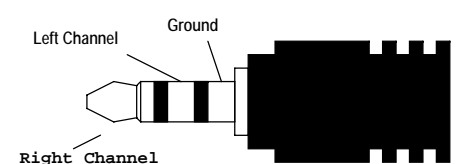
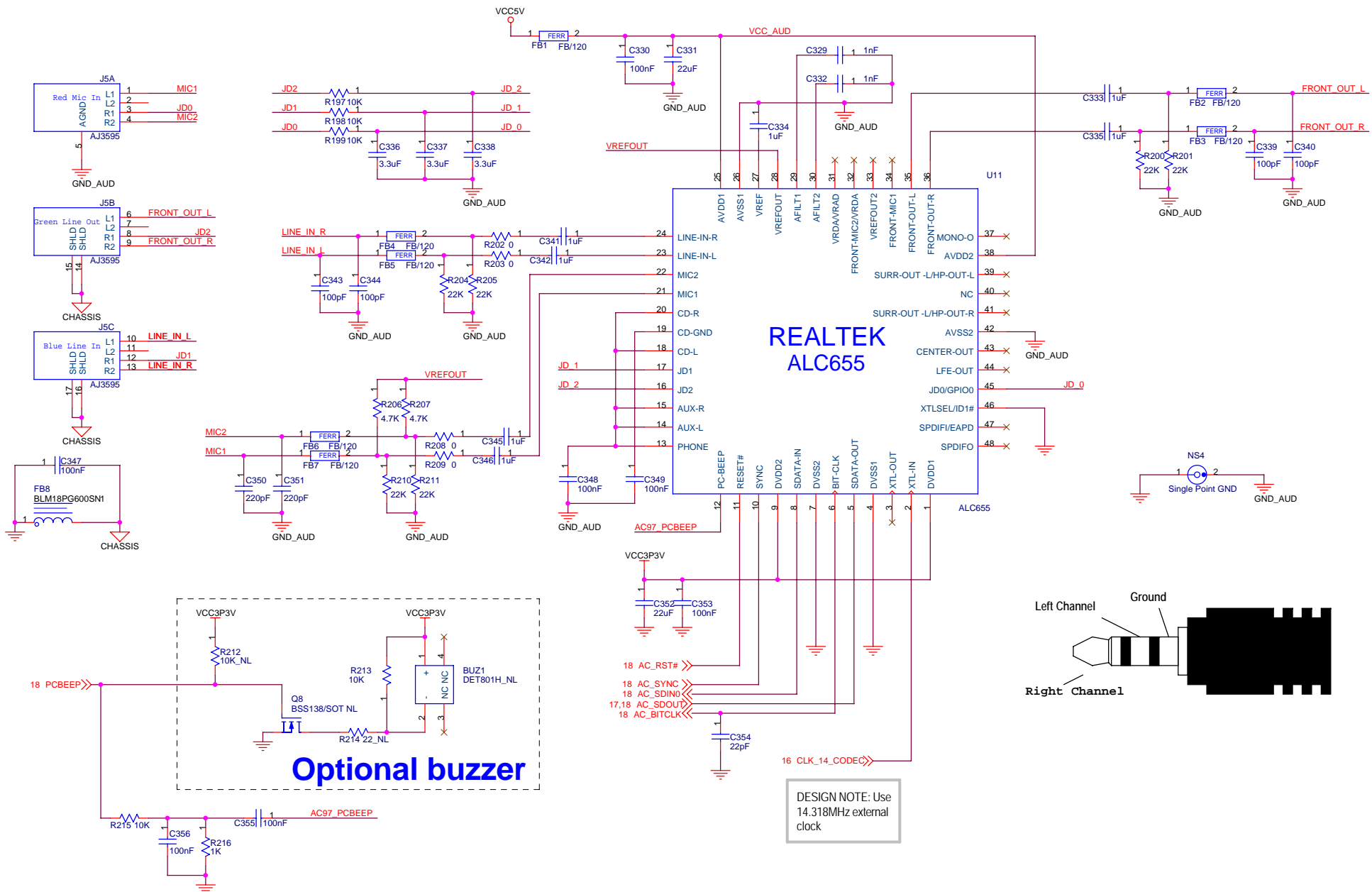
SIGNAL NAME IN ( ) IS UNIQUE TO 5787M

**Broadcom Ethernet Controller**

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Title: **AMD S1 / AMD M690T Reference Schematic**  
PID: **42504** Rev: **0.5**  
Size: Custom Date: Tuesday, March 13, 2007 Sheet: **22** of **31**

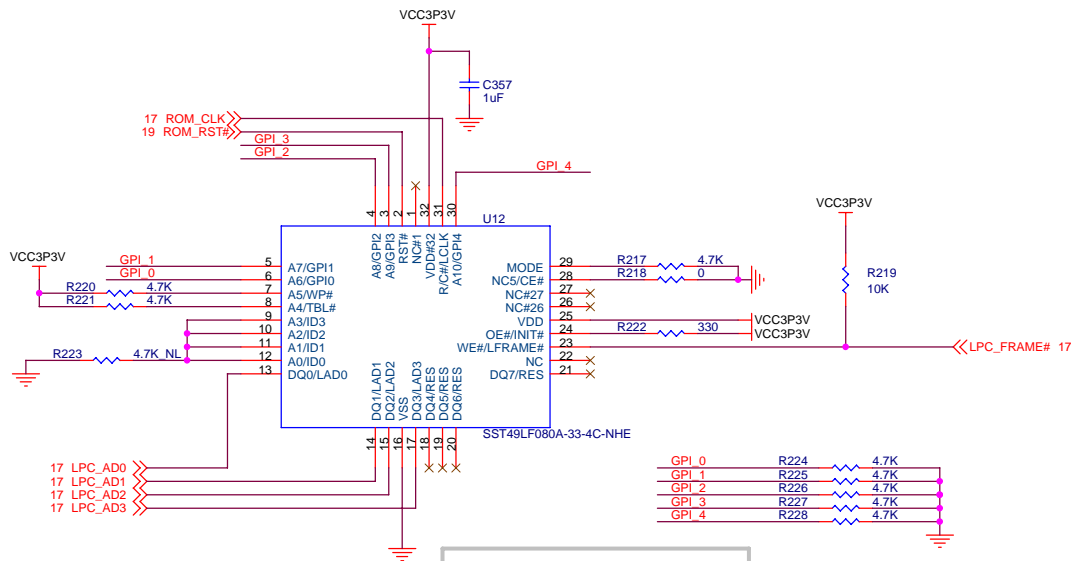


DESIGN NOTE: Use 14.318MHz external clock

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Title	AMD S1 / AMD M690T Reference Schematic	
PID	42504	Rev 0.5
Size	Custom	Date: Tuesday, March 13, 2007
		Sheet 23 of 31

Realtek Audio Codec



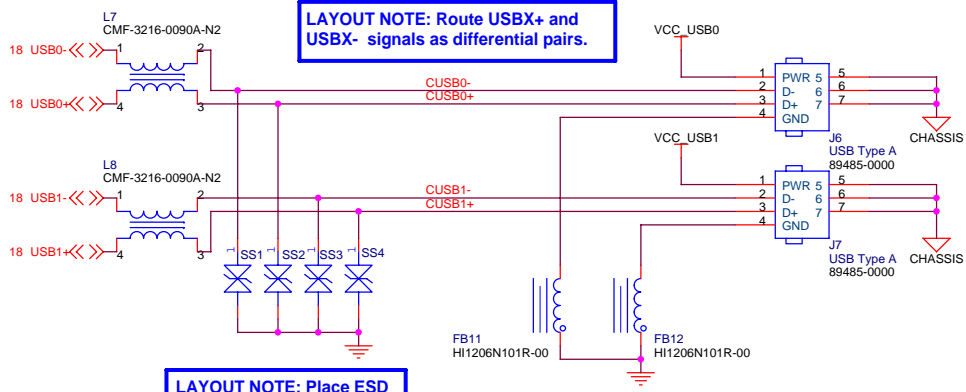
DESIGN NOTE:  
 MODE: low - LPC mode is enabled  
       high - programmer mode is enabled  
 CE#: low - device is enabled  
       high - device is in low power mode

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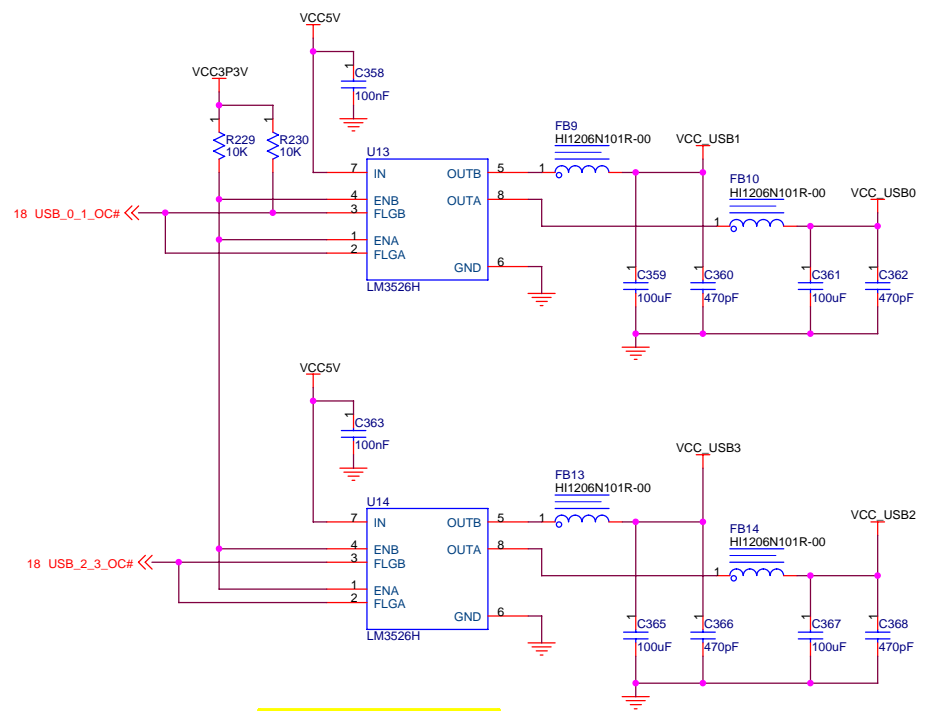
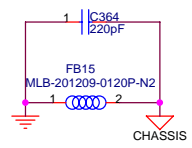
Advanced Micro Devices 1351 South Sunset St. Longmont, CO 80501		<b>AMD</b>	
Title <b>AMD S1 / AMD M690T Reference Schematic</b>			
PID <b>42504</b>	Date: <b>Tuesday, March 13, 2007</b>		Rev <b>0.5</b>
Size <b>Custom</b>	Sheet <b>24</b> of <b>31</b>		

**LPC BIOS**

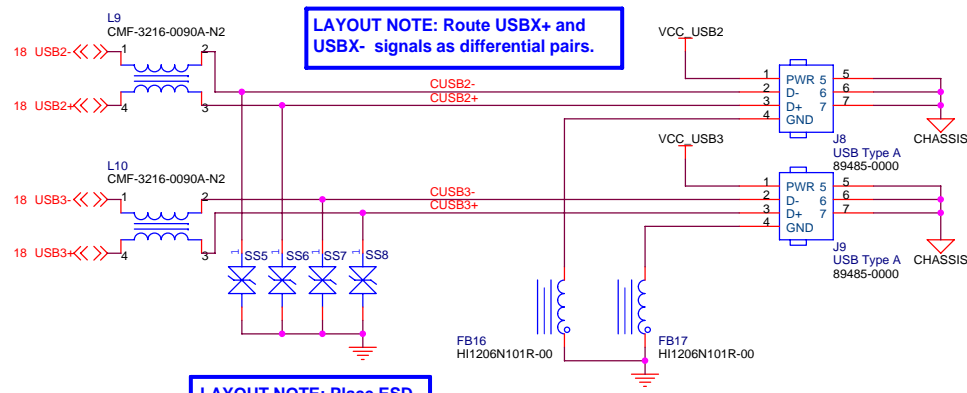




LAYOUT NOTE: Place ESD protection components as close to the USB/Ethernet connector as possible.



DESIGN NOTE: Power supply solution must be able to provide sufficient current on VCC5V to power each USB port with 500mA.



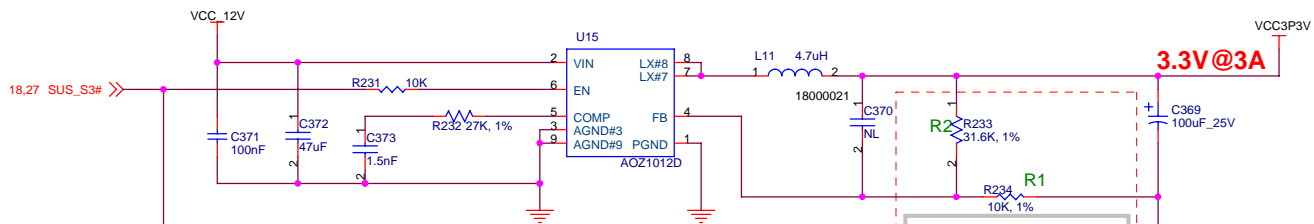
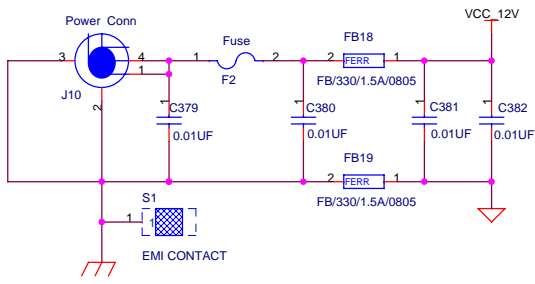
LAYOUT NOTE: Place ESD protection components as close to the USB/Ethernet connector as possible.

### USB Power and Connectors

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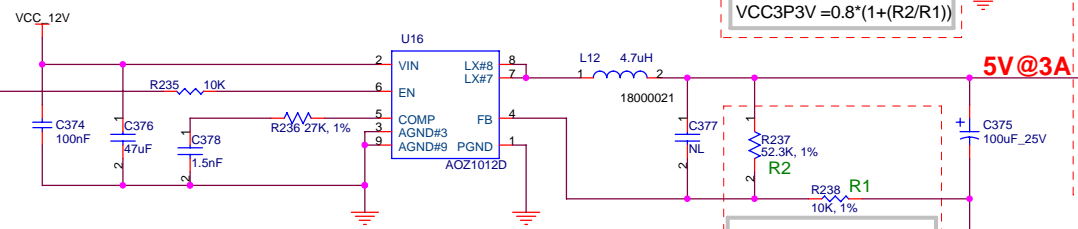
Advanced Micro Devices 1351 South Sunset St. Longmont, CO 80501		
Title	AMD S1 / AMD M690T Reference Schematic	
PID	42504	Rev 0.5
Size	Custom	Date: Tuesday, March 13, 2007
		Sheet 25 of 31

DESIGN NOTE: Generic power supply connector. Should provides +12V @ 7A for this reference design.

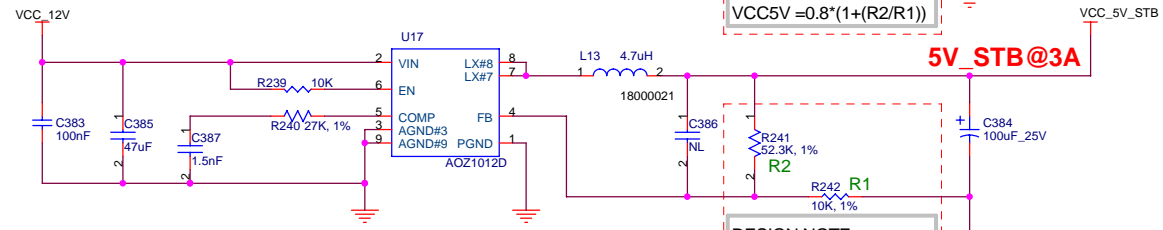


DESIGN NOTE:  
 $VCC3P3V = 0.8 * (1 + (R2/R1))$

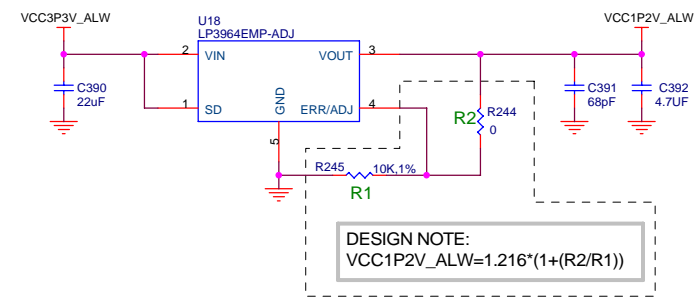
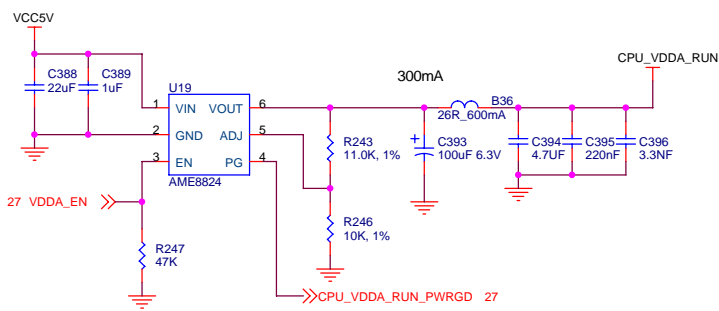
DESIGN NOTE:  
Provides for 4 ports USB. If more ports then use higher capacity supply such as the AOZ1014.



DESIGN NOTE:  
 $VCC5V = 0.8 * (1 + (R2/R1))$



DESIGN NOTE:  
 $VCC5V = 0.8 * (1 + (R2/R1))$

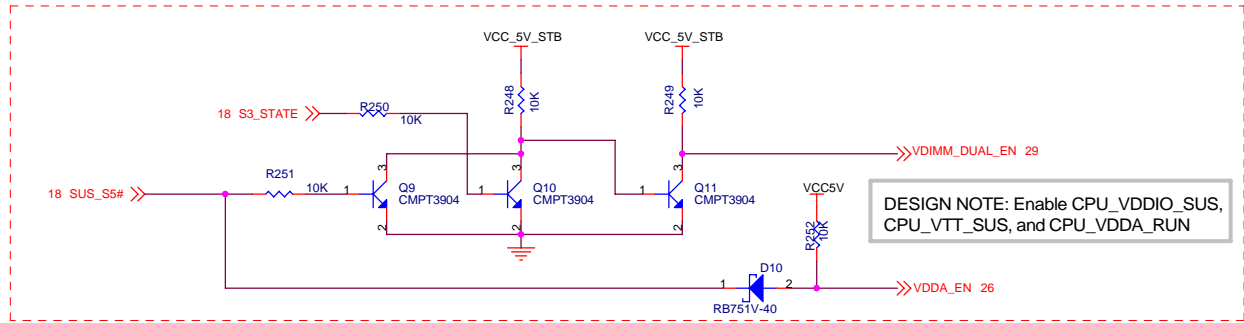


DESIGN NOTE:  
 $VCC1P2V\_ALW = 1.216 * (1 + (R2/R1))$

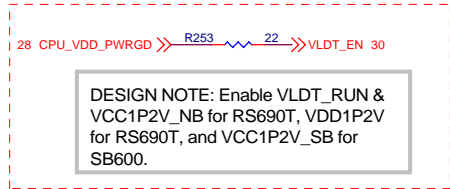
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Advanced Micro Devices 1351 South Sunset St. Longmont, CO 80501		
Title: AMD S1 / AMD M690T Reference Schematic		
PID: 42504	Rev: 0.5	
Size: Custom	Date: Tuesday, March 13, 2007	Sheet 26 of 31

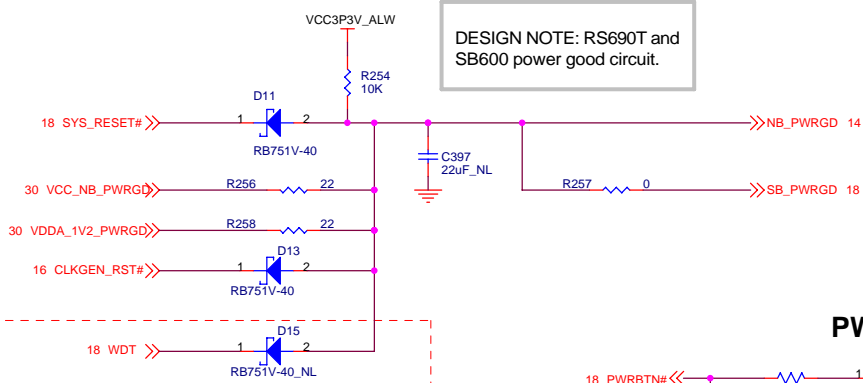
**Power Main System, SB600 PCIe™, and Other**



DESIGN NOTE: Enable CPU\_VDDIO\_SUS, CPU\_VTT\_SUS, and CPU\_VDDA\_RUN

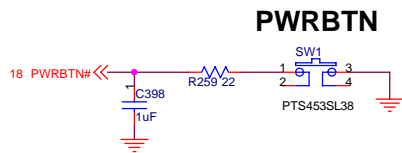
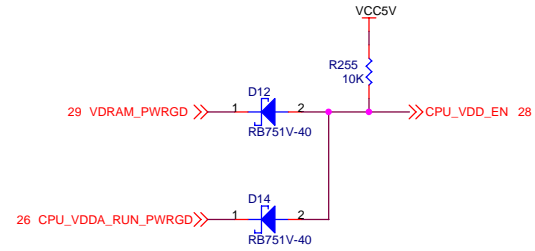


DESIGN NOTE: Enable VLDT\_RUN & VCC1P2V\_NB for RS690T, VDD1P2V for RS690T, and VCC1P2V\_SB for SB600.

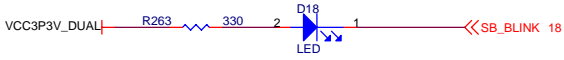
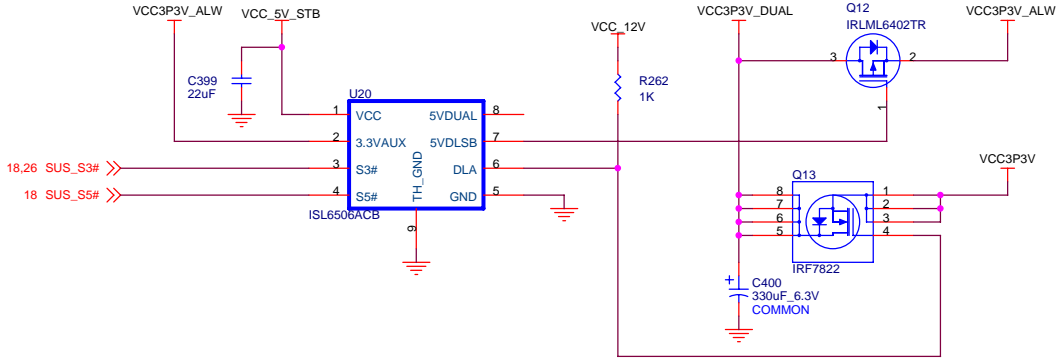
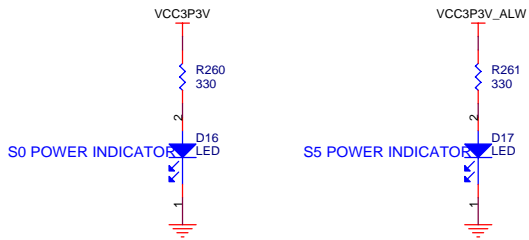


DESIGN NOTE: RS690T and SB600 power good circuit.

DESIGN NOTE: The SB600 specification indicates that the function of WDT has not been qualified as of 1-16-2007.



PWRBTN



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Title	AMD S1 / AMD M690T Reference Schematic		
PID	42504	Rev	0.5
Size	Custom	Date:	Tuesday, March 13, 2007
Sheet	27	of	31

Standby Power and Powergood

DESIGN NOTE: CPU\_VDD\_RUN=387.5mV to 1.55V @ 35A max, 37W max.

DESIGN NOTE: Offset voltage is not required for this design. If it is required contact device manufacture for details on use of the OFS and REF pins

LAYOUT NOTE: Place thermistor near MOSFET's and Inductors if temp monitoring is desired.

DESIGN NOTE: If power output and temp monitoring is desired contact device manufacture for details on proper use of the POUT, VRHOT# and THRM pins.

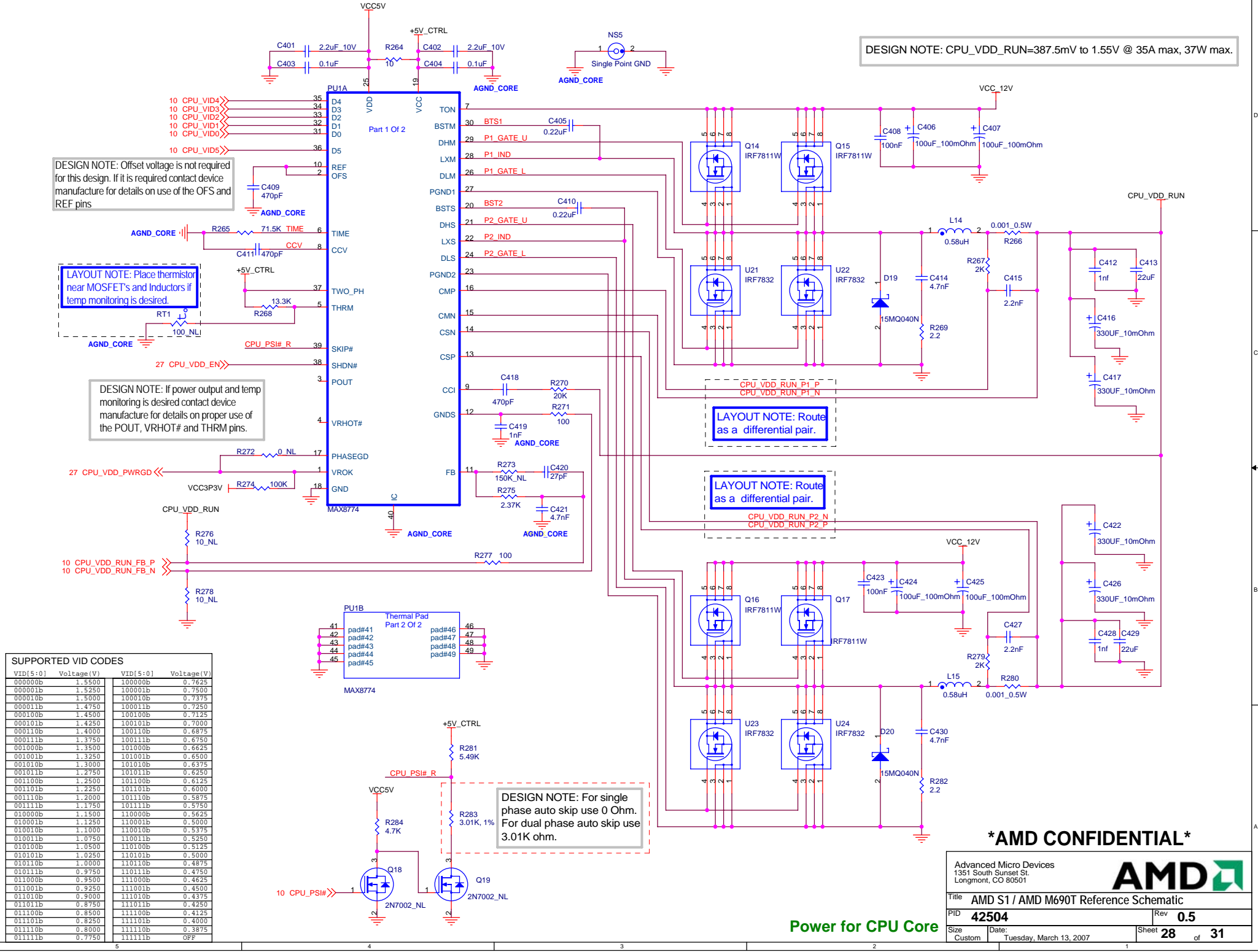
LAYOUT NOTE: Route as a differential pair.

LAYOUT NOTE: Route as a differential pair.

DESIGN NOTE: For single phase auto skip use 0 Ohm. For dual phase auto skip use 3.01K ohm.

**SUPPORTED VID CODES**

VID[5:0]	Volts(V)	VID[5:0]	Volts(V)
00000b	1.5500	10000b	0.7625
00001b	1.5250	10001b	0.7500
000010b	1.5000	100010b	0.7375
000011b	1.4750	100011b	0.7250
000100b	1.4500	100100b	0.7125
000101b	1.4250	100101b	0.7000
000110b	1.4000	100110b	0.6875
000111b	1.3750	100111b	0.6750
001000b	1.3500	101000b	0.6625
001001b	1.3250	101001b	0.6500
001010b	1.3000	101010b	0.6375
001011b	1.2750	101011b	0.6250
001100b	1.2500	101100b	0.6125
001101b	1.2250	101101b	0.6000
001110b	1.2000	101110b	0.5875
001111b	1.1750	101111b	0.5750
010000b	1.1500	110000b	0.5625
010001b	1.1250	110001b	0.5500
010010b	1.1000	110010b	0.5375
010011b	1.0750	110011b	0.5250
010100b	1.0500	110100b	0.5125
010101b	1.0250	110101b	0.5000
010110b	1.0000	110110b	0.4875
010111b	0.9750	110111b	0.4750
011000b	0.9500	111000b	0.4625
011001b	0.9250	111001b	0.4500
011010b	0.9000	111010b	0.4375
011011b	0.8750	111011b	0.4250
011100b	0.8500	111100b	0.4125
011101b	0.8250	111101b	0.4000
011110b	0.8000	111110b	0.3875
011111b	0.7750	111111b	OFF



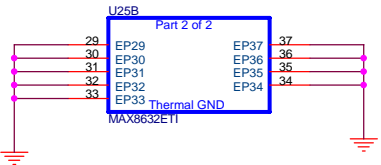
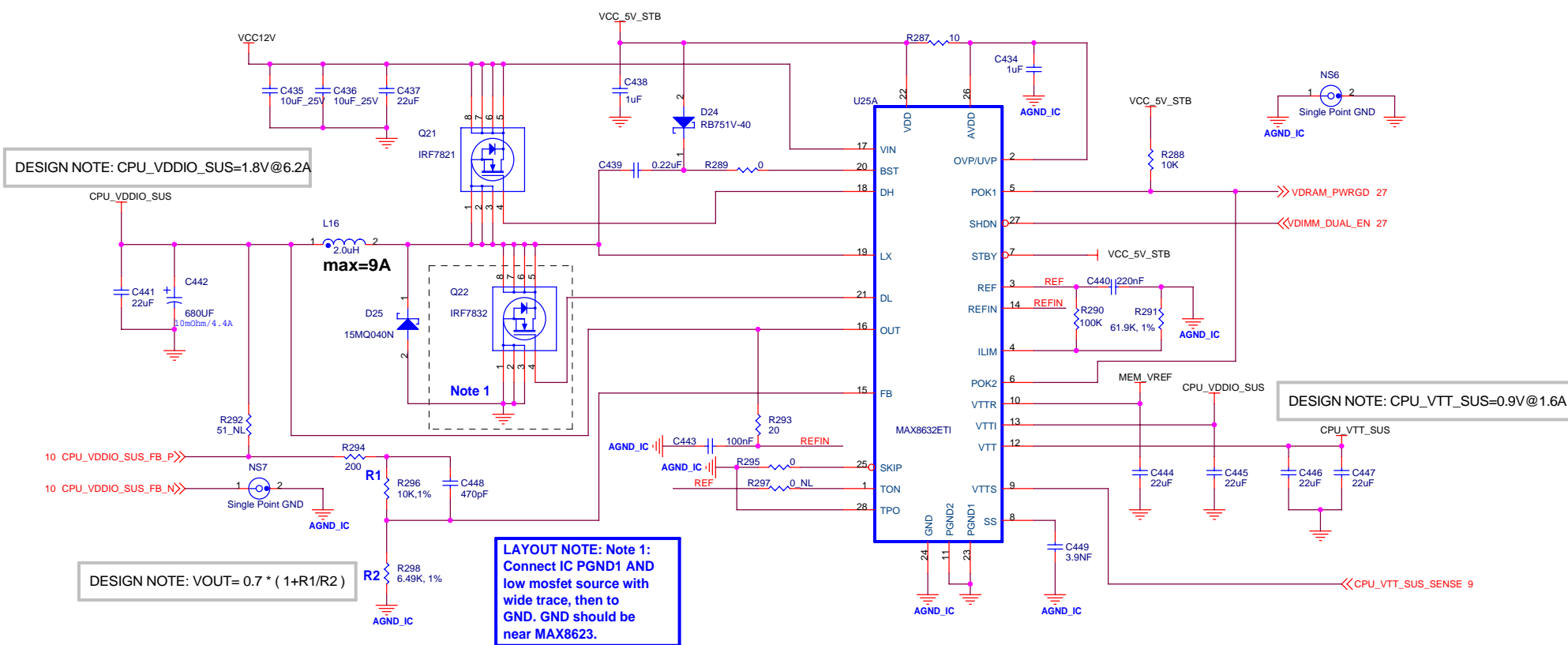
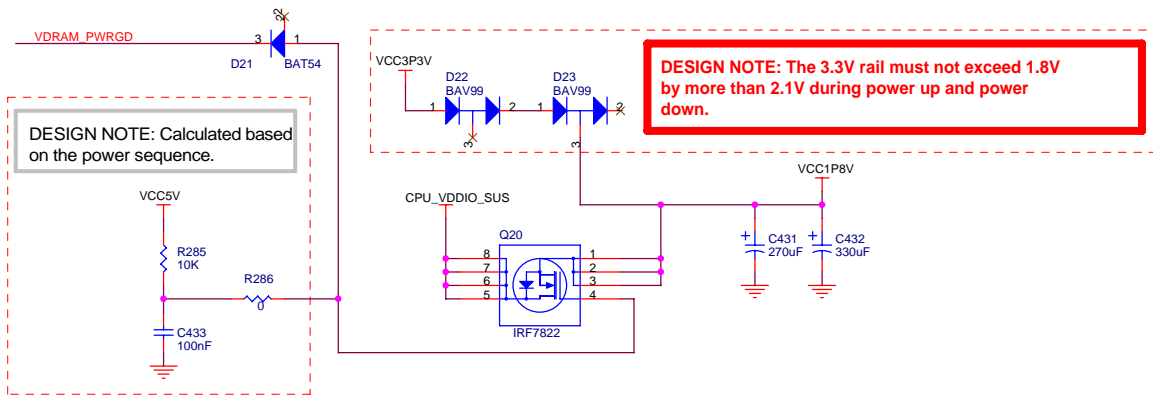
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Title		AMD S1 / AMD M690T Reference Schematic	
PID	42504	Rev	0.5
Size	Custom	Date	Tuesday, March 13, 2007
Sheet	28	of	31

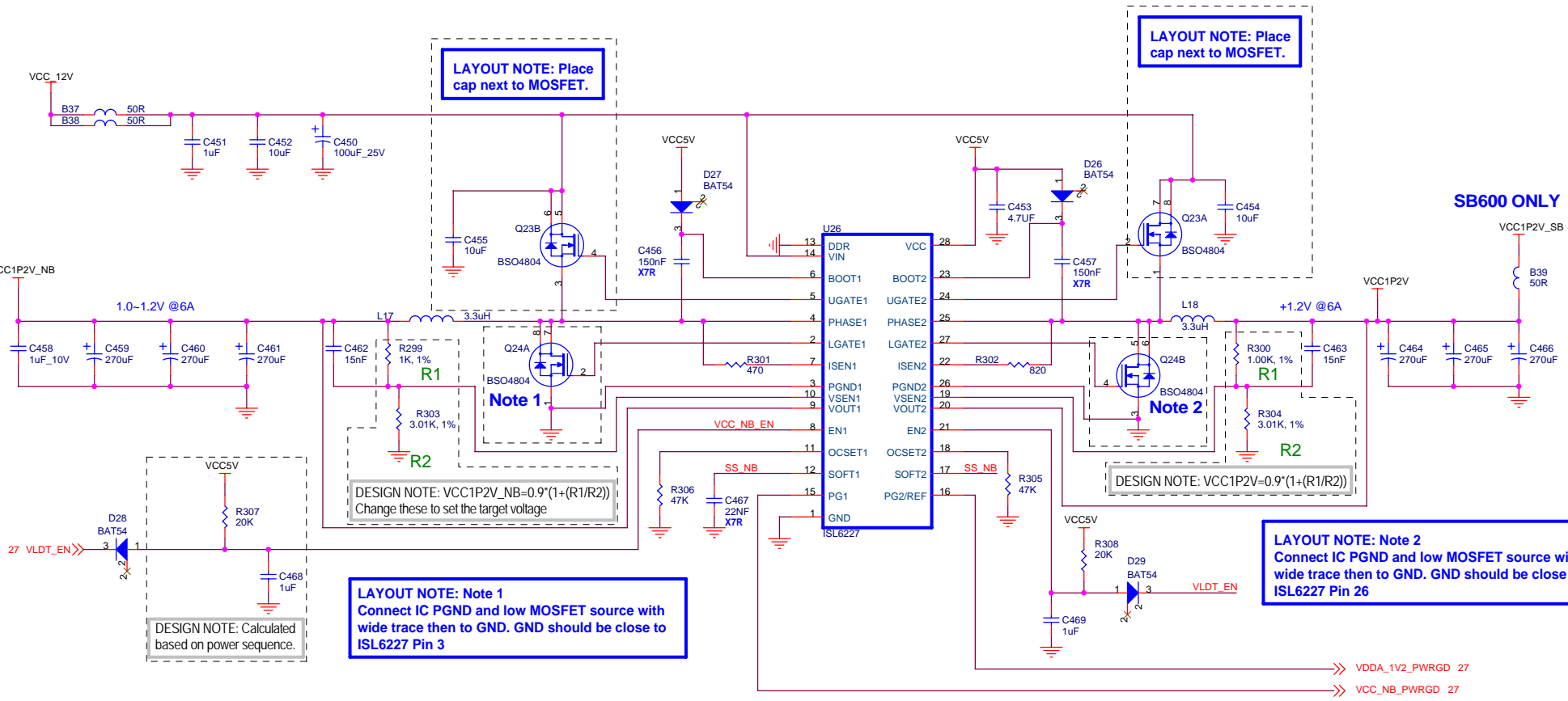
Power for CPU Core



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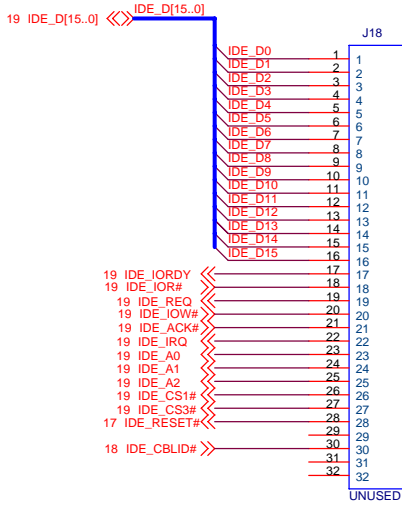
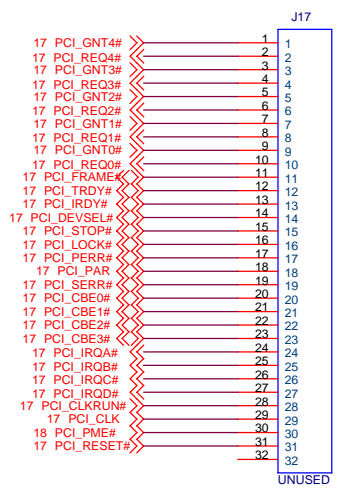
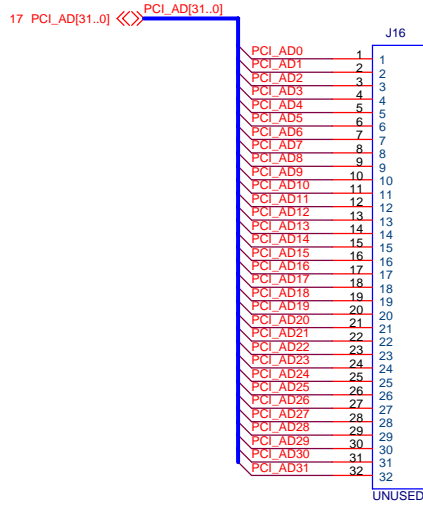
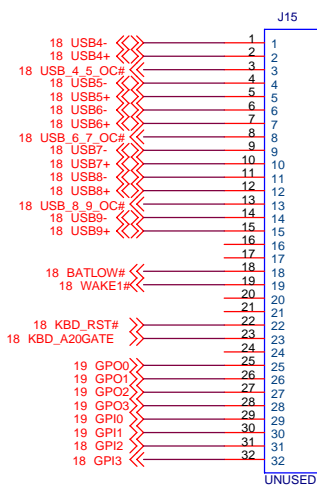
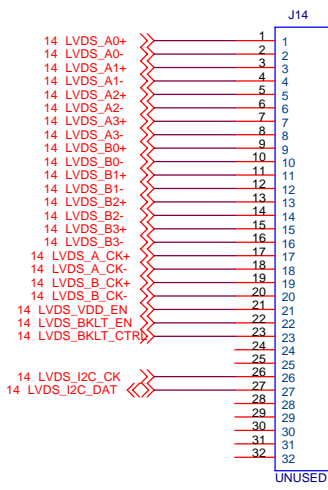
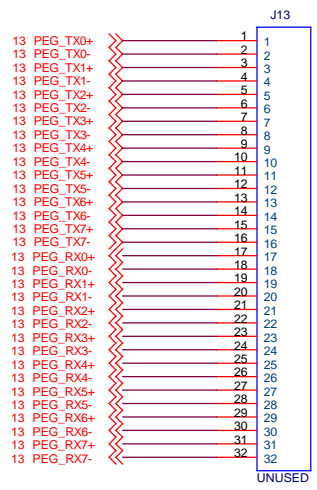
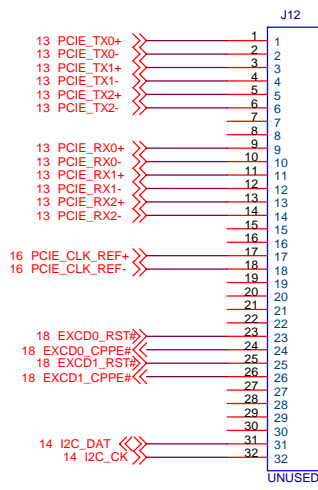
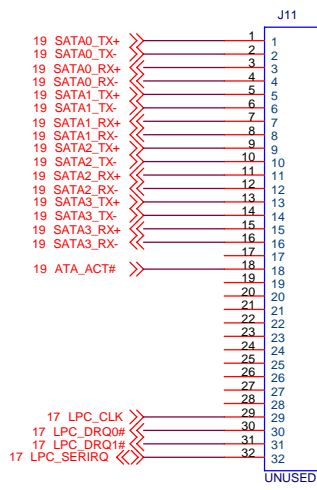
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PID	42504	Rev	0.5
Size	Custom	Date:	Tuesday, March 13, 2007
Sheet	29	of	31

**Power for DDR2 Memory and Interface**




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Size: Custom	Date: Tuesday, March 13, 2007	Sheet: <b>30</b> of <b>31</b>



DESIGN NOTE: This page has been included in this schematic to enable the design rule check tool to produce results without errors or warnings. The interfaces on this page do not have connectivity to devices or connectors. This page as well as unused interfaces on the corresponding pages should be deleted on final schematics.

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PID	42504	Rev	0.5
Size	Custom	Date:	Tuesday, March 13, 2007
Sheet	31	of	31

Unused Interfaces