AMD Geode™ LX DB800 Development Board LX-ETX-Board Schematic

NOTES:

1) THIS SCHEMATIC IS TARGETED AT AN AMD GEODE™ LX PROCESSOR AND CS5535/CS5536 COMPANION DEVICE BASED DESIGN.

IMPORTANT NOTICE:

1. THIS DOCUMENT MAY NOT REFLECT THE MOST RECENT CHANGES IN BOARD DEVELOPMENT AND DEBUG. ANY DEVELOPER INTENDING TO USE THIS SCHEMATIC AS A REFERNCE SHOULD CONTACT THEIR LOCAL FIELD APPLICATIONS ENGINEER, REGIONAL SALES OFFICE, OR PROGRAM MANAGER FOR SCHEMATIC UPDATES, DESIGN RECOMMENDATIONS AND PCB LAYOUT GUIDELINES. AMD ALSO RECOMMENDS A DESIGN REVIEW OF BOTH THE SCHEMATIC DIAGRAM AND PCB LAYOUT BEFORE CONSIDERING PRODUCTION.

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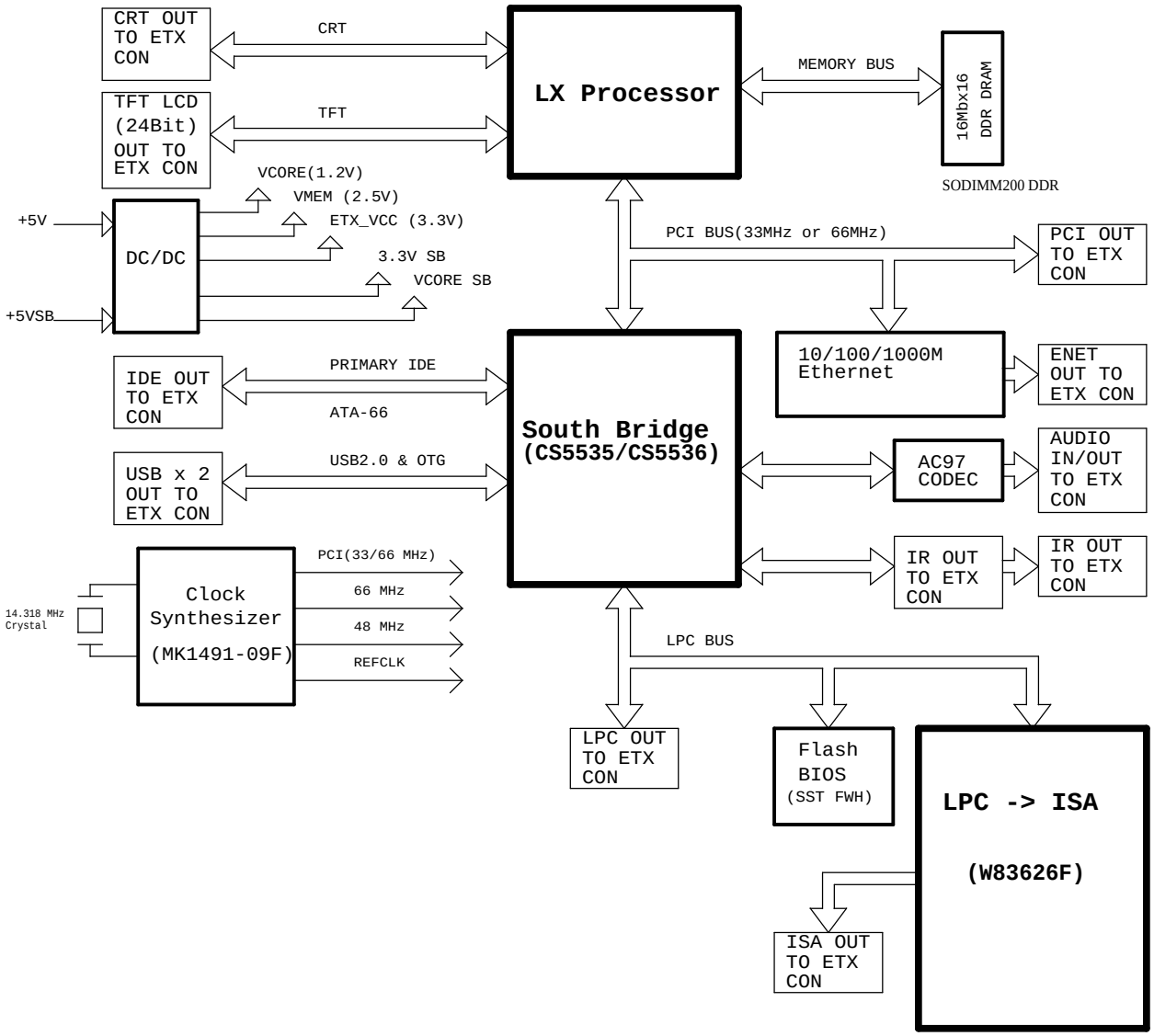

REVISIONS 7->8

1. CHANGED TITLE AND NOMENCLATURE TO USE LX PROCESSOR INSTEAD OF CASTLE OR GX3.

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PROJECT:	AMD Geode™ LX-ETX-Board Schematic
PART NUMBER:	1000370
ASSEMBLY NAME:	ETX
SCHEMATICS:	ECR

IMPORTANT NOTES ABOUT THIS SCHEMATIC

DESIGN NOTE: Example text for the design note to show the note inside the colored box.

1) DESIGN NOTES in grey are information notes.

DESIGN NOTE: Example text for the design note to show the note inside the colored box.

2) DESIGN NOTES in yellow are notes of caution.

DESIGN NOTE: Example text for the design note to show the note inside the colored box.

3) DESIGN NOTES in red are critical, and must be understood and followed.

REVISIONS 4->5

1. REMOVED ALL 4 POINT CONNECTIONS FOR CLARITY WHEN PRINTING HARD COPIES.
2. REMOVED PAGE CONTAINING ONLY POPULATION OPTIONS FOR THE CS5535/CS5536. THOSE OPTIONS ARE NOW LOCATED ON THE PAGES THEY CONCERN.
3. CHANGED ALL PAGES TO B SIZE, THIS RESULTED IN THE SPLITING UP OF SOME PAGES AND THE REORGANIZING OF OTHERS.
4. WHERE POSSIBLE REPLACED GENERAL PULLUPS/PULLDOWNS/SERIES RESISTORS WITH RPAKS TO REDUCE COMPONENT COUNT AND LABOR COSTS ASSOCIATED WITH POPULATION.

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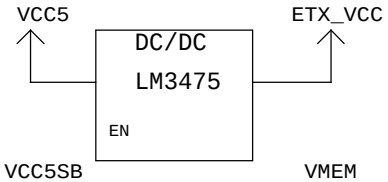

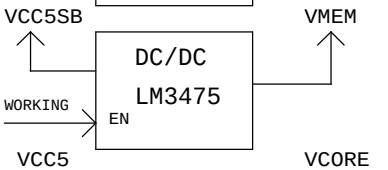

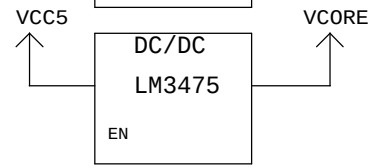

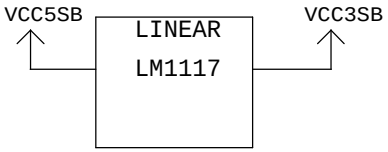

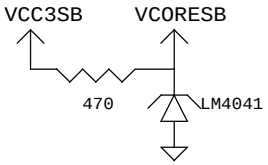

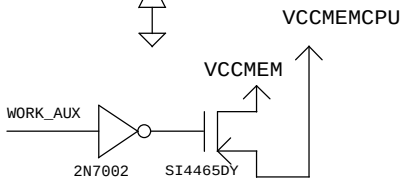

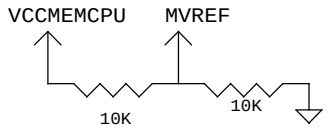

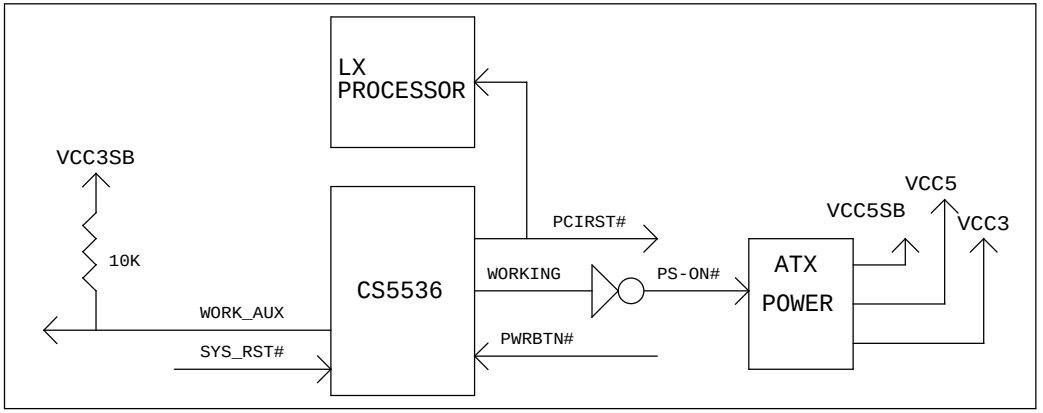

SYSTEM POWER

VCC=+5V
VCC3=+3.3V
VCC5SB=+5V

LX PROCESSOR

VCORE=+1.2V
VCCMEMCPU=+2.5V
MVREF=+1.25V
VIO=+3.3V

CS5536 POWER

VCORE=+1.2V
VCORESB=+1.2V
VIO=+3.3V

MEMORY POWER

VMEM=+2.5V
MVREF=+1.25V

SUSPEND TO RAM

@Enter S3 mode: WORK_AUX---> LOW

VCC5=0, VCORE=0, VCC3=0, VCCMEMCPU=0, MVREF=0
VCC5SB=5V, VCC3SB=3.3V, VCORESB=1.2, VCCMEM=2.5V

Power On and Reset Sequence

PWRBTN# → PS-ON# → Power ON ATX → SYS_RST# → PCIRST#

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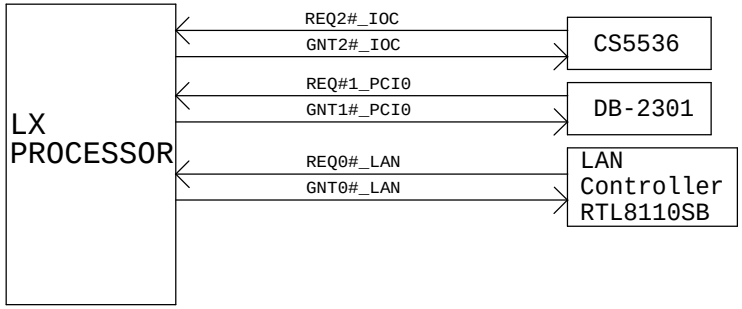
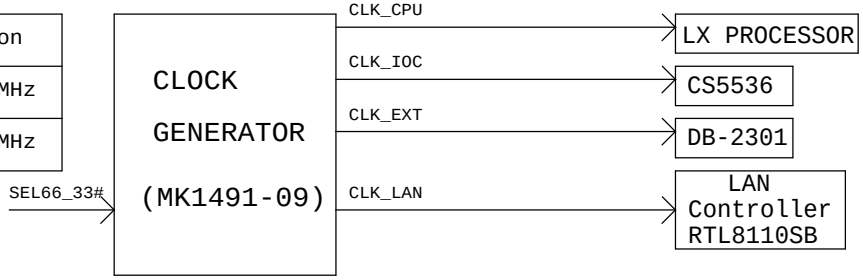
PCI MASTER SETTING

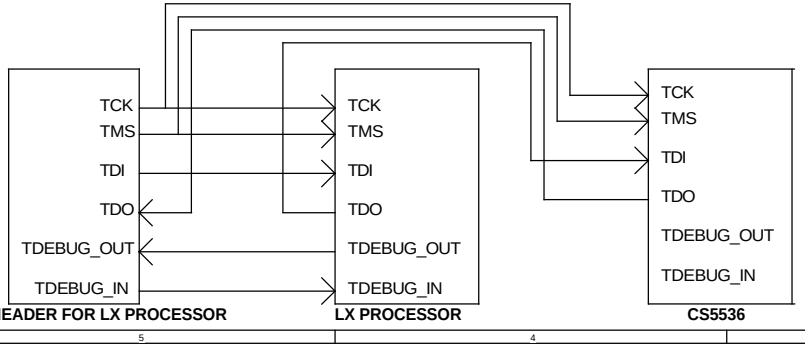


PCI CLOCK SETTING

SEL66_33#	Function
1	PCI 66 MHz
0	PCI 33 MHz



JTAG DAISY CHAIN MODE WITH CS5536



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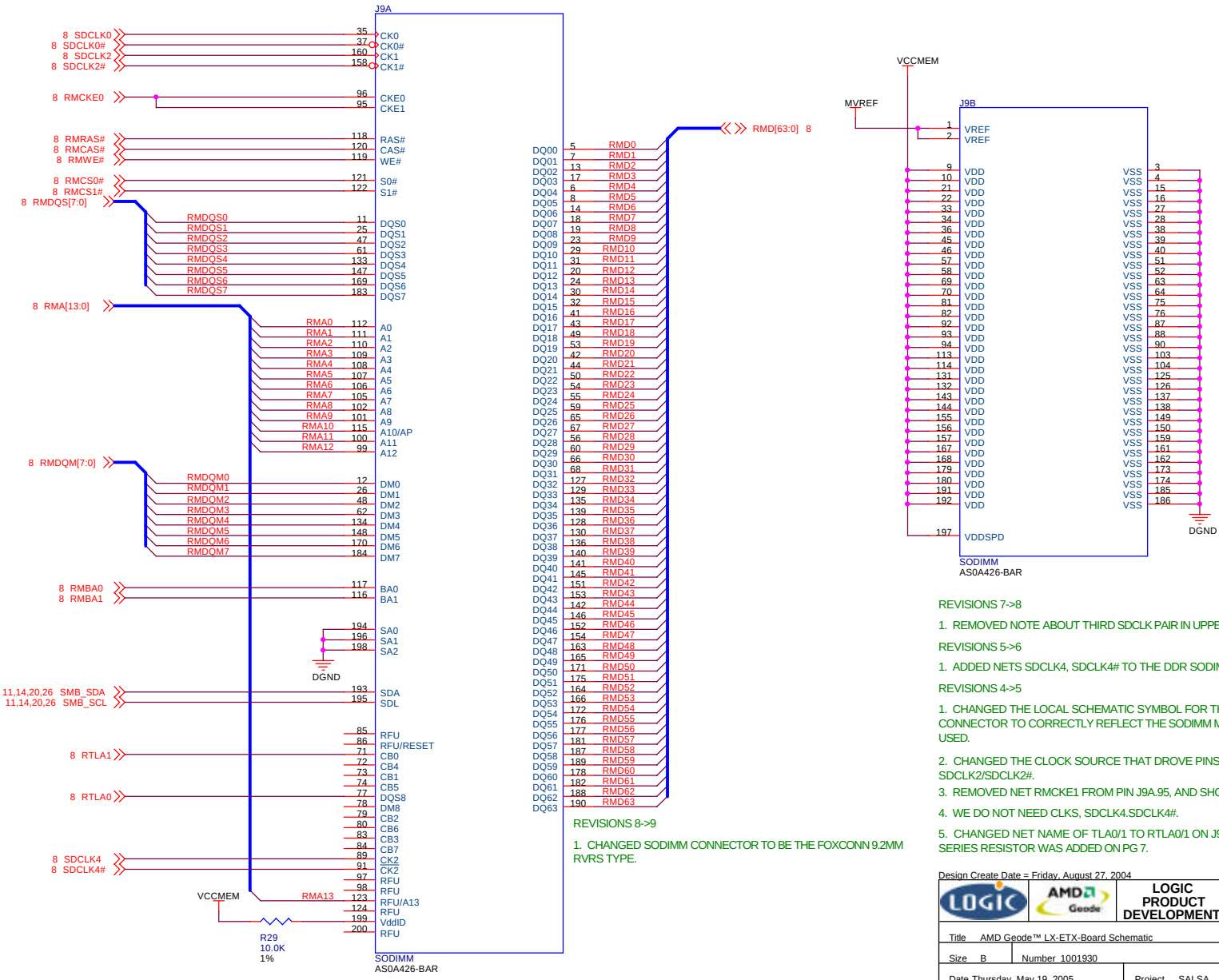
J9A
8 SDCLK0
8 SDCLK0#
8 SDCLK2
8 SDCLK2#
CK0
CK0#
CK1
CK1#
8 RMCKE0
CKE0
CKE1
8 RMRAS#
8 RMCAS#
8 RMWE#
RAS#
CAS#
WE#
8 RMCS0#
8 RMCS1#
S0#
S1#
8 RMDQS[7:0]
RMDQS0
RMDQS1
RMDQS2
RMDQS3
RMDQS4
RMDQS5
RMDQS6
RMDQS7
DQS0
DQS1
DQS2
DQS3
DQS4
DQS5
DQS6
DQS7
8 RMA[13:0]
RMA0
RMA1
RMA2
RMA3
RMA4
RMA5
RMA6
RMA7
RMA8
RMA9
RMA10
RMA11
RMA12
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10/AP
A11
A12
8 RMDQM[7:0]
RMDQM0
RMDQM1
RMDQM2
RMDQM3
RMDQM4
RMDQM5
RMDQM6
RMDQM7
DM0
DM1
DM2
DM3
DM4
DM5
DM6
DM7
8 RMBA0
8 RMBA1
BA0
BA1
SA0
SA1
SA2
DGND
11,14,20,26 SMB_SDA
11,14,20,26 SMB_SCL
SDA
SDL
RFU
RFU/RESET
8 RTLA1
CB0
CB4
CB1
CB5
8 RTLA0
DQS8
DM8
CB2
CB6
CB3
CB7
8 SDCLK4
8 SDCLK4#
CK2
CK2
RFU
RFU
VCCMEM
RMA13
RFU/A13
RFU
VddID
RFU
R29
10.0K
1%
SODIMM
AS0A426-BAR
DQ00 DQ01 DQ02 DQ03 DQ04 DQ05 DQ06 DQ07 DQ08 DQ09 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15 DQ16 DQ17 DQ18 DQ19 DQ20 DQ21 DQ22 DQ23 DQ24 DQ25 DQ26 DQ27 DQ28 DQ29 DQ30 DQ31 DQ32 DQ33 DQ34 DQ35 DQ36 DQ37 DQ38 DQ39 DQ40 DQ41 DQ42 DQ43 DQ44 DQ45 DQ46 DQ47 DQ48 DQ49 DQ50 DQ51 DQ52 DQ53 DQ54 DQ55 DQ56 DQ57 DQ58 DQ59 DQ60 DQ61 DQ62 DQ63
RMD0 RMD1 RMD2 RMD3 RMD4 RMD5 RMD6 RMD7 RMD8 RMD9 RMD10 RMD11 RMD12 RMD13 RMD14 RMD15 RMD16 RMD17 RMD18 RMD19 RMD20 RMD21 RMD22 RMD23 RMD24 RMD25 RMD26 RMD27 RMD28 RMD29 RMD30 RMD31 RMD32 RMD33 RMD34 RMD35 RMD36 RMD37 RMD38 RMD39 RMD40 RMD41 RMD42 RMD43 RMD44 RMD45 RMD46 RMD47 RMD48 RMD49 RMD50 RMD51 RMD52 RMD53 RMD54 RMD55 RMD56 RMD57 RMD58 RMD59 RMD60 RMD61 RMD62 RMD63
RMD[63:0] 8
REVISIONS 8->9
1. CHANGED SODIMM CONNECTOR TO BE THE FOXCONN 9.2MM RVRS TYPE.
VCCMEM
MVREF
J9B
VREF
VREF
VDD
VSS
VDDSPD
DGND
SODIMM
AS0A426-BAR
REVISIONS 7->8
1. REMOVED NOTE ABOUT THIRD SDCLK PAIR IN UPPER LEFTHAND CORNER.
REVISIONS 5->6
1. ADDED NETS SDCLK4, SDCLK4# TO THE DDR SODIMM-200.
REVISIONS 4->5
1. CHANGED THE LOCAL SCHEMATIC SYMBOL FOR THE DDR SDRAM CONNECTOR TO CORRECTLY REFLECT THE SODIMM MODULES THAT WILL BE USED.
2. CHANGED THE CLOCK SOURCE THAT DROVE PINS J9A.160,158 TO SDCLK2/SDCLK2#.
3. REMOVED NET RMCKE1 FROM PIN J9A.95, AND SHORTED RMCKE0 TO J9A.95.
4. WE DO NOT NEED CLKS, SDCLK4.SDCLK4#.
5. CHANGED NET NAME OF TLA0/1 TO RTLA0/1 ON J9A.71,77 BECAUSE A SERIES RESISTOR WAS ADDED ON PG 7.
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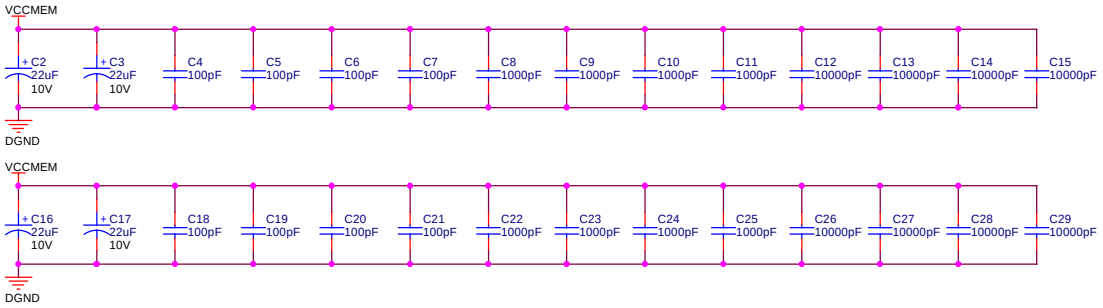
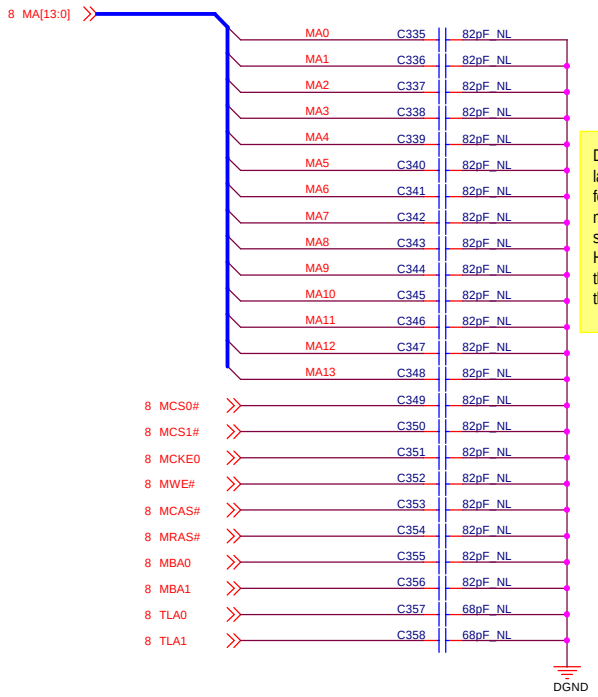
DDR SODIMM DECOUPLING CAPACITORS



DDR SODIMM WAVE SHAPING CAPACITORS



DESIGN NOTE: If the layout guidelines are followed for the DDR memory block these caps should not be necessary. However we recommend that they be included in the layout .

REVISIONS 10->11

1. CHANGED C335-C356 FROM 68pF TO 82pF.
2. ADDED DESIGN NOTE INDICATING THAT C335-C356 SHOULD NOT NEED TO BE INSTALLED.

REVISIONS 5->6

1. REMOVED C357, C358 FROM NETS TLA0 AND TLA1, NOT NEEDED.

REVISIONS 4->5

1. ADDED 24 68pF CAPS TO THE DDR ADDRESS AND CONTROL SIGNALS BASED ON TESTING INFORMATION RECEIVED FROM ANALYSIS DONE AT AMD.

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DESIGN NOTE: Testpoints designated by ref des TP_ and having the shown footprint TP_SM_040 are surface only testpoints with no via, with a 40 diameter pad.

DESIGN NOTE: BA0,BA1 MUST BE TRACE LENGTH MATCHED TO WITHIN 50MILS.

DESIGN NOTE: Swap series resistors on the DQS lines in order minimize the number of vias.

DESIGN NOTE: Swap series resistors on the address lines in order minimize the number of vias.

DESIGN NOTE: Do not swap series resistors on the DQS, DQM or Data lines with the Address or control lines.

DESIGN NOTE: Swap series resistors on the data lines in order minimize the number of vias.

DESIGN NOTE: Place data bus series resistors as close to the memory devices as possible.

DESIGN NOTE: Place DQS and DQM series resistors as close to the SODIMM connector as possible.

DESIGN NOTE: Place address and control series resistors as close to the processor as possible.

DESIGN NOTE: Use SDCLK pairs that are most convient for clean routing.

DESIGN NOTE: Test points (TPx) must not adversely affect the layout. In general they should be a surface mount pad not covered with solder mask.

U1A

LX PROCESSOR

GX3

RMD[63:0] 6

RMDQS[7:0] 6

RMDQM[7:0] 6

RMA[13:0] 6

RTLA0 6

RTLA1 6

RMBA0 6

RMBA1 6

RMCS0# 6

RMCS1# 6

RMCKE0 6

RMWE# 6

RMRAS# 6

RMCAS# 6

VCCMEM

R219 10.0K 1%

R220 10.0K 1%

Vout = 1.25

MVREF

C257 0.1uF

C1 0.1uF

DGND

REVISIONS 10->11

1. CHANGED RN1-11,13,15,17,20,23,25-28,104 FROM 22 OHMS TO 33 OHMS.

REVISIONS 6->7

1. CHANGED THE TESTPOINTS TP6,7,8,9,10,11,12 ,13,14 TO THRU-HOLE VIA'D TESTPOINTS.

REVISIONS 5->6

1. ADDED NOTE BY THE BYTE LANE ENABLES INDICATING THE MUST BE TRACE LENGTH MATCHED TO WITHIN 50MILS OF EACH OTHER.
2. CHANGED VOLTAGE SUPPLIED TO MVREF ON R219 TO VCCMEM FROM VCCMEMCPU.
3. ADDED NETS SDCLK4, SDCLK4# TO GO DIRECTLY TO THE DDR SODIMM-200.

REVISIONS 4->5

1. ADDED SERIES RESISTORS TO NETS TLA0/1. SHOWED FOOTPRINT PROPERTY ON TESTPOINTS TO INDICATE THAT THEY ARE PAD ONLY.
2. REMOVED NETS SDCLK4,SDCLK4# FROM U1A.J4,H4. ADDED NETS SDCLK2,SDCLK2# TO U1A.M28,L28.

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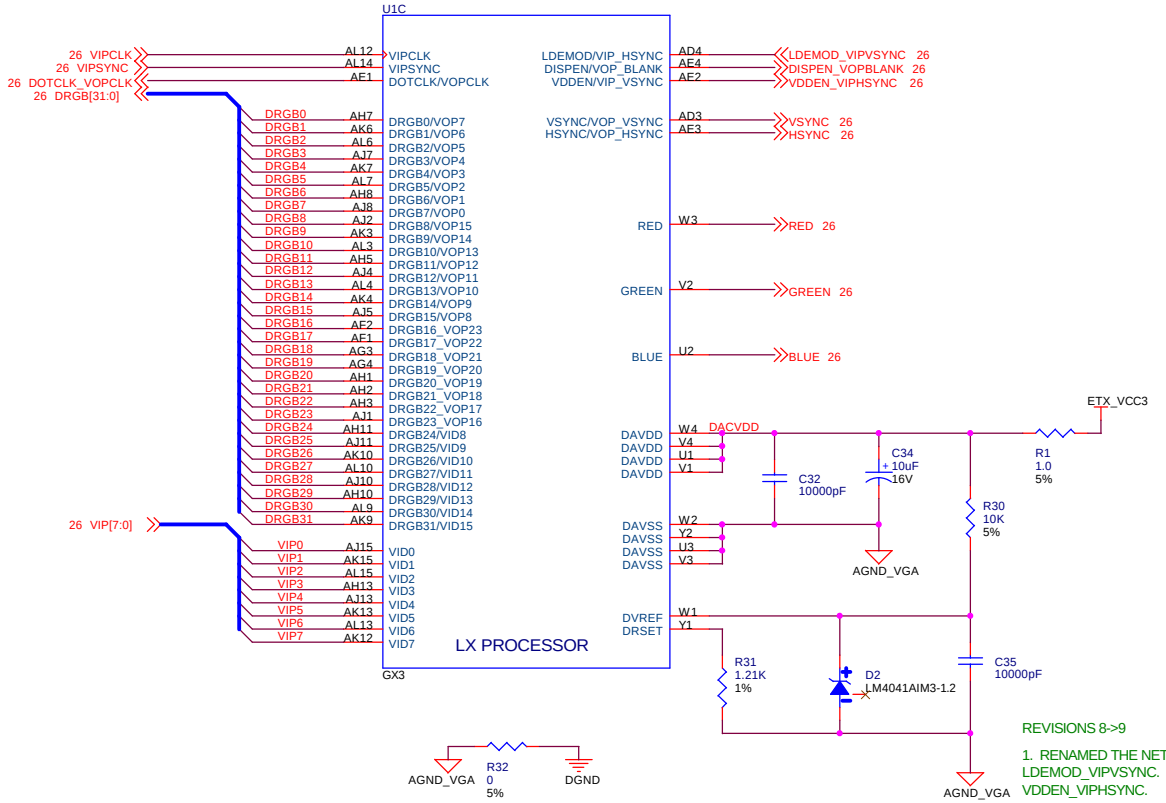

DESIGN NOTE: AGND_VGA should be an island with single point connection to the full ground plane to reduce noise content. Zero ohm resistor can be removed as long as above condition is met.

REVISIONS 8->9

1. RENAMED THE NETS: LDEMOD_VIPHSYNC WAS RENAMED TO LDEMOD_VIPVSYNC. VDDEN_VIPVSYNC WAS RENAMED TO VDDEN_VIPHSYNC.

REVISIONS 5->6

1. VERIFIED THAT THE LM4041AIM3-1.2 WILL TURN ON WITH A 10K RESISTOR IN PLACE. 4041 SPEC SAYS MIN OPERATING CURRENT IS 60uA, WITH A 10K WE SHOULD HAVE A LOAD OF 210uA.

REVISIONS 4->5

1. REMOVED C30, C31, C33 (100pF, 100pF, 10000pF) AND FB1 FROM THE DAVDD SUPPLY. REPLACED WITH 10uF AND .01uF WITH A SERIES 1OHM. ALSO REMOVED C36, (1uF) THAT HUNG OFF OF DVREF.

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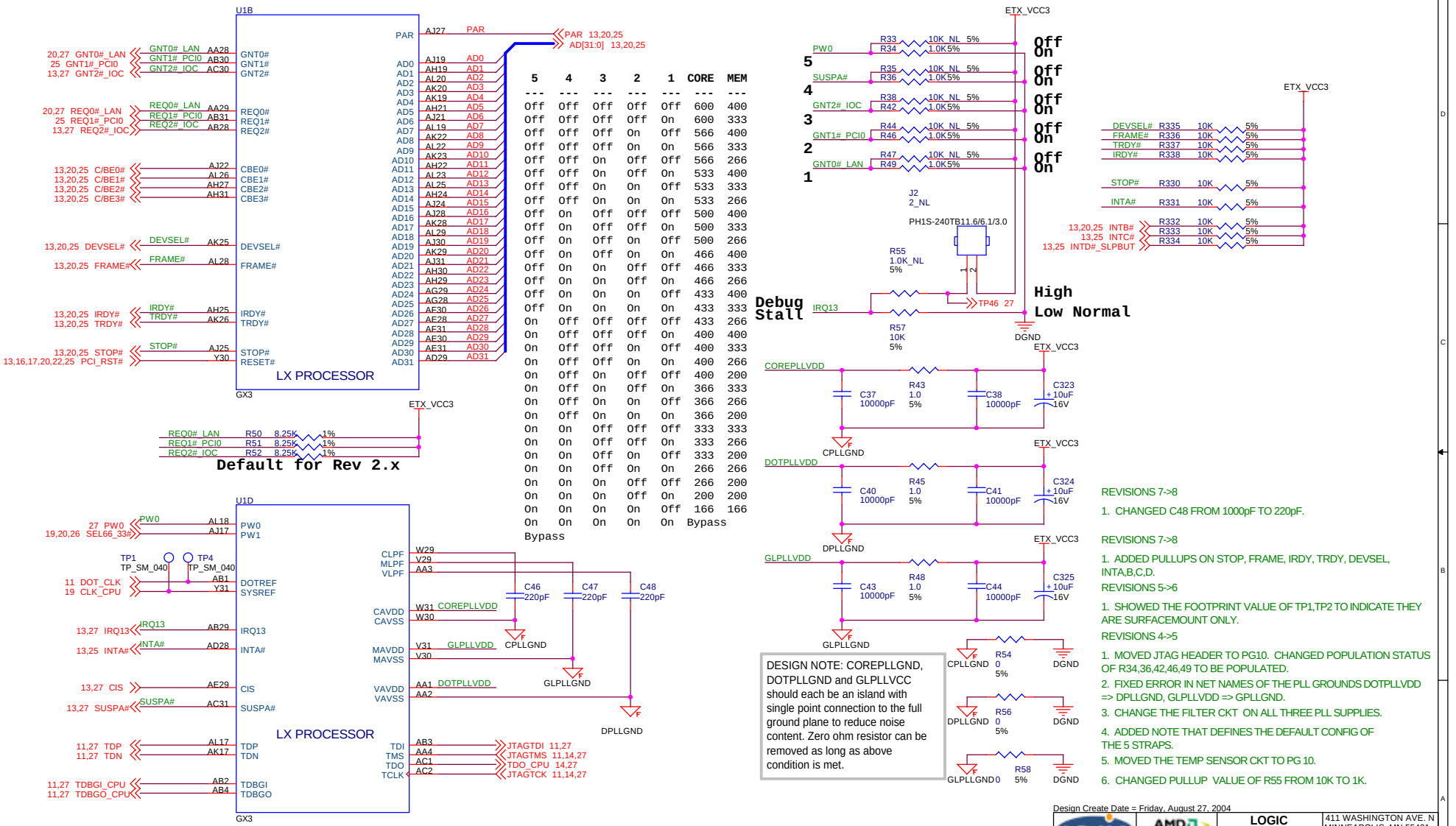
U1B
LX PROCESSOR
GX3
PAR
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
AD8
AD9
AD10
AD11
AD12
AD13
AD14
AD15
AD16
AD17
AD18
AD19
AD20
AD21
AD22
AD23
AD24
AD25
AD26
AD27
AD28
AD29
AD30
AD31
GNT0#
GNT1#
GNT2#
REQ0#
REQ1#
REQ2#
CBE0#
CBE1#
CBE2#
CBE3#
DEVSEL#
FRAME#
IRDY#
TRDY#
STOP#
RESET#
20,27 GNT0#_LAN
25 GNT1#_PCI0
13,27 GNT2#_IOC
20,27 REQ0#_LAN
25 REQ1#_PCI0
13,27 REQ2#_IOC
13,20,25 C/BE0#
13,20,25 C/BE1#
13,20,25 C/BE2#
13,20,25 C/BE3#
13,20,25 DEVSEL#
13,20,25 FRAME#
13,20,25 IRDY#
13,20,25 TRDY#
13,20,25 STOP#
13,16,17,20,22,25 PCI_RST#
PAR 13,20,25
AD[31:0] 13,20,25
ETX_VCC3
REQ0# LAN R50 8.25K 1%
REQ1# PCI0 R51 8.25K 1%
REQ2# IOC R52 8.25K 1%
Default for Rev 2.x
U1D
LX PROCESSOR
GX3
PW0
PW1
DOTREF
SYSREF
IRQ13
INTA#
CIS
SUSPA#
TDP
TDN
TDBGI
TDBGO
CLPF
MLPF
VLPF
CAVDD
CAVSS
MAVDD
MAVSS
VAVDD
VAVSS
TDI
TMS
TDO
TCLK
27 PW0
19,20,26 SEL66_33#
TP1 TP_SM_040
TP4 TP_SM_040
11 DOT_CLK
19 CLK_CPU
13,27 IRQ13
13,25 INTA#
13,27 CIS
13,27 SUSPA#
11,27 TDP
11,27 TDN
11,27 TDBGI_CPU
11,27 TDBGO_CPU
C46 220pF
C47 220pF
C48 220pF
COREPLLVDD
CPLLGND
GLPLLVDD
DOTPLLVDD
GLPLLGND
DPLLGND
JTAGTDI 11,27
JTAGTMS 11,14,27
TDO_CPU 14,27
JTAGTCK 11,14,27
5 4 3 2 1 CORE MEM
Off Off Off Off Off 600 400
Off Off Off Off On 600 333
Off Off Off On Off 566 400
Off Off Off On On 566 333
Off Off On Off Off 566 266
Off Off On Off On 533 400
Off Off On On Off 533 333
Off Off On On On 533 266
Off On Off Off Off 500 400
Off On Off Off On 500 333
Off On Off On Off 500 266
Off On Off On On 466 400
Off On On Off Off 466 333
Off On On Off On 466 266
Off On On On Off 433 400
Off On On On On 433 333
On Off Off Off Off 433 266
On Off Off Off On 400 400
On Off Off On Off 400 333
On Off Off On On 400 266
On Off On Off Off 400 200
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On Off On On Off 366 266
On Off On On On 366 200
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On On Off Off On 333 266
On On Off On Off 333 200
On On Off On On 266 266
On On On Off Off 266 200
On On On Off On 200 200
On On On On Off 166 166
On On On On On Bypass
Bypass
ETX_VCC3
PW0
SUSPA#
GNT2#_IOC
GNT1#_PCI0
GNT0#_LAN
R33 10K_NL 5%
R34 1.0K5%
R35 10K_NL 5%
R36 1.0K5%
R38 10K_NL 5%
R42 1.0K5%
R44 10K_NL 5%
R46 1.0K5%
R47 10K_NL 5%
R49 1.0K5%
5 Off On
4 Off On
3 Off On
2 Off On
1 Off On
J2
2_NL
PH1S-240TB11.6/6.1/3.0
R55 1.0K_NL 5%
Debug Stall
IRQ13
TP46 27
R57 10K 5%
High
Low Normal
DGND
DEVSEL# R335 10K 5%
FRAME# R336 10K 5%
TRDY# R337 10K 5%
IRDY# R338 10K 5%
STOP# R330 10K 5%
INTA# R331 10K 5%
13,20,25 INTB# R332 10K 5%
13,25 INTC# R333 10K 5%
13,25 INTD#_SLPBUT R334 10K 5%
COREPLLVDD
C37 10000pF
R43 1.0 5%
C38 10000pF
C323 10uF 16V
DOTPLLVDD
C40 10000pF
R45 1.0 5%
C41 10000pF
C324 10uF 16V
GLPLLVDD
C43 10000pF
R48 1.0 5%
C44 10000pF
C325 10uF 16V
R54 0 5%
R56 0 5%
R58 0 5%
DESIGN NOTE: COREPLLGND, DOTPLLGND and GLPLLVCC should each be an island with single point connection to the full ground plane to reduce noise content. Zero ohm resistor can be removed as long as above condition is met.
REVISIONS 7->8
1. CHANGED C48 FROM 1000pF TO 220pF.
REVISIONS 7->8
1. ADDED PULLUPS ON STOP, FRAME, IRDY, TRDY, DEVSEL, INTA,B,C,D.
REVISIONS 5->6
1. SHOWED THE FOOTPRINT VALUE OF TP1,TP2 TO INDICATE THEY ARE SURFACEMOUNT ONLY.
REVISIONS 4->5
1. MOVED JTAG HEADER TO PG10. CHANGED POPULATION STATUS OF R34,36,42,46,49 TO BE POPULATED.
2. FIXED ERROR IN NET NAMES OF THE PLL GROUNDS DOTPLLVDD => DPLLGND, GLPLLVDD => GPLLGND.
3. CHANGE THE FILTER CKT ON ALL THREE PLL SUPPLIES.
4. ADDED NOTE THAT DEFINES THE DEFAULT CONFIG OF THE 5 STRAPS.
5. MOVED THE TEMP SENSOR CKT TO PG 10.
6. CHANGED PULLUP VALUE OF R55 FROM 10K TO 1K.
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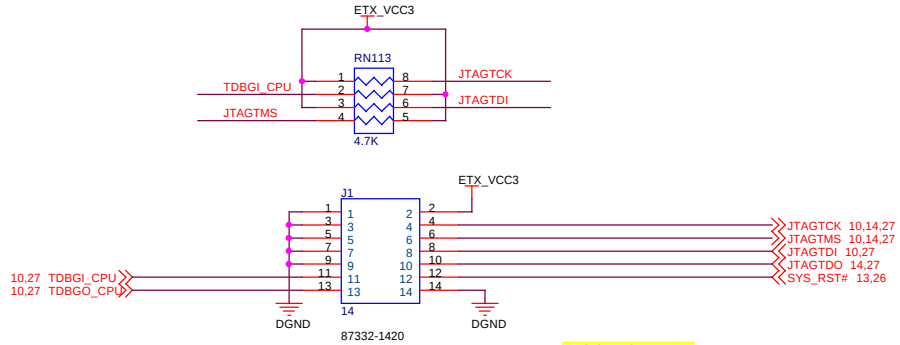
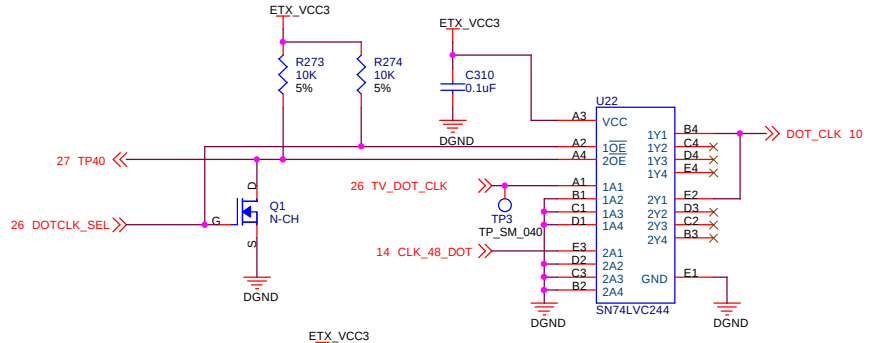
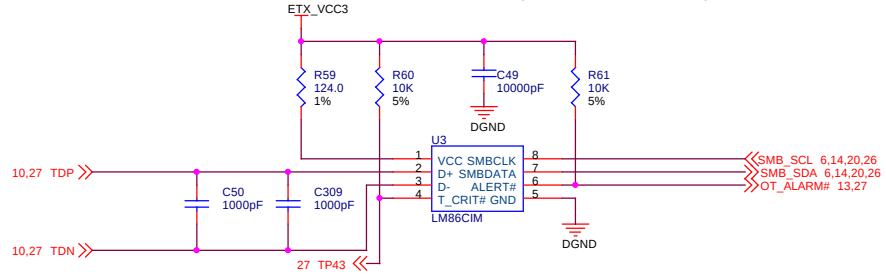


JTAG HEADER

DESIGN NOTE: ADD "JTAG HEADER" TO SILKSCREEN





ACCESS.BUS ADDRESS=98 FOR LM86

TEMPERATURE SENSOR

REVISIONS 9->10

1. REMOVED TP42

REVISIONS 8->9

1. REMOVED OFF PAGE CONNECTOR TP10, CONFLICTED WITH TDP ON U3

REVISIONS 5->6

1. CHANGED NET FOCUS_DOT_CLK NAME TO TV_DOT_CLK.
2. REMOVED R62 (WAS BTWN TDP AND U3.2), NOT NEEDED WAS PREVIOUSLY USED FOR DEBUG.

REVISIONS 4->5

1. ADDED THIS PAGE, AND MOVED, JTAG, TEMP SENSE AND DOT CLK CKT TO IT.

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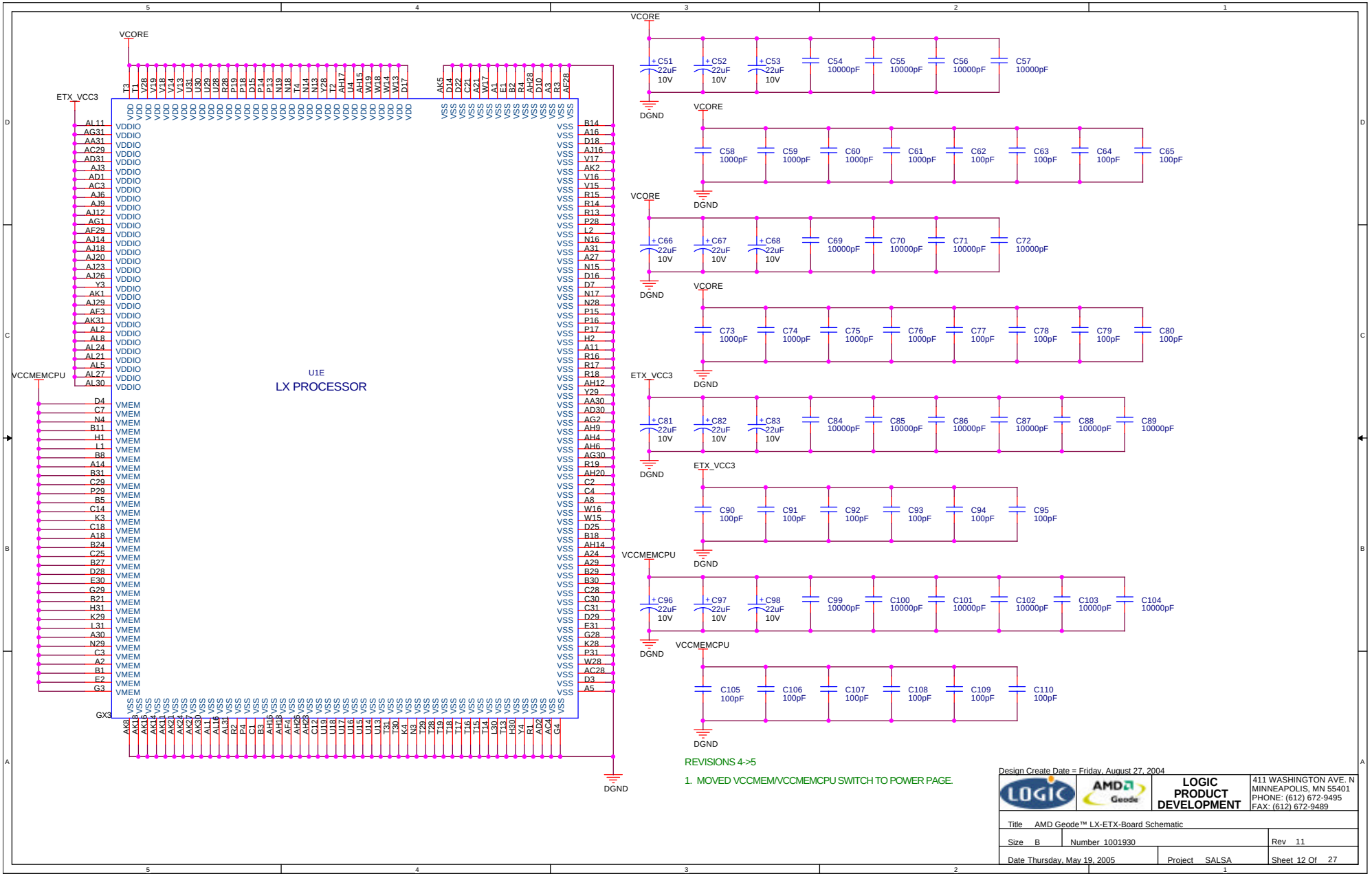

REVISIONS 4->5

1. MOVED VCCMEM/VCCMEMCPU SWITCH TO POWER PAGE.

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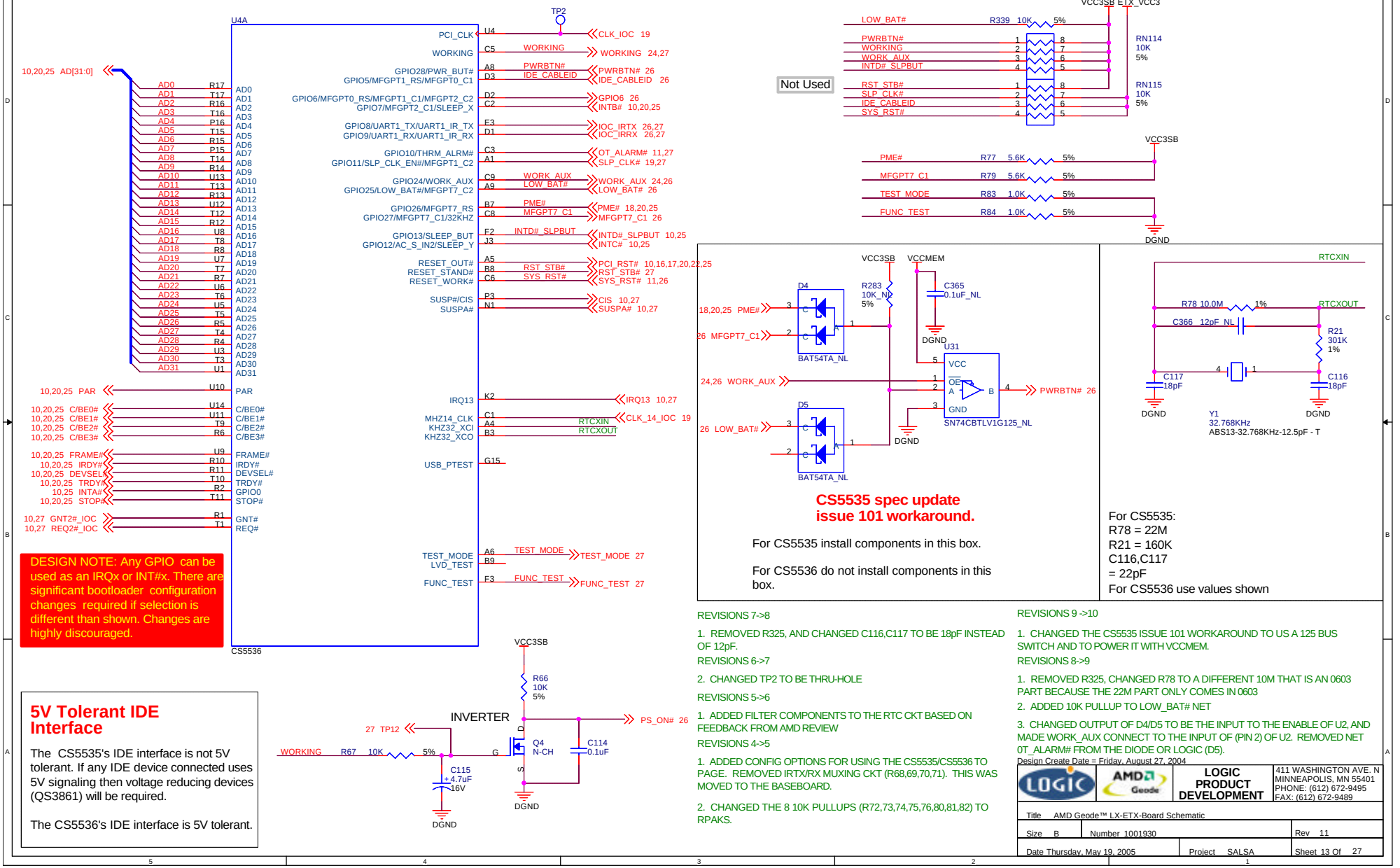

REVISIONS 7->8

1. REMOVED R325, AND CHANGED C116,C117 TO BE 18pF INSTEAD OF 12pF.

REVISIONS 6->7

2. CHANGED TP2 TO BE THRU-HOLE

REVISIONS 5->6

1. ADDED FILTER COMPONENTS TO THE RTC CKT BASED ON FEEDBACK FROM AMD REVIEW

REVISIONS 4->5

1. ADDED CONFIG OPTIONS FOR USING THE CS5535/CS5536 TO PAGE. REMOVED IRTX/RX MUXING CKT (R68,69,70,71). THIS WAS MOVED TO THE BASEBOARD.

2. CHANGED THE 8 10K PULLUPS (R72,73,74,75,76,80,81,82) TO RPAKS.

REVISIONS 9 ->10

1. CHANGED THE CS5535 ISSUE 101 WORKAROUND TO US A 125 BUS SWITCH AND TO POWER IT WITH VCCMEM.

REVISIONS 8->9

1. REMOVED R325, CHANGED R78 TO A DIFFERENT 10M THAT IS AN 0603 PART BECAUSE THE 22M PART ONLY COMES IN 0603

2. ADDED 10K PULLUP TO LOW_BAT# NET

3. CHANGED OUTPUT OF D4/D5 TO BE THE INPUT TO THE ENABLE OF U2, AND MADE WORK_AUX CONNECT TO THE INPUT OF (PIN 2) OF U2. REMOVED NET 0T_ALARM# FROM THE DIODE OR LOGIC (D5).

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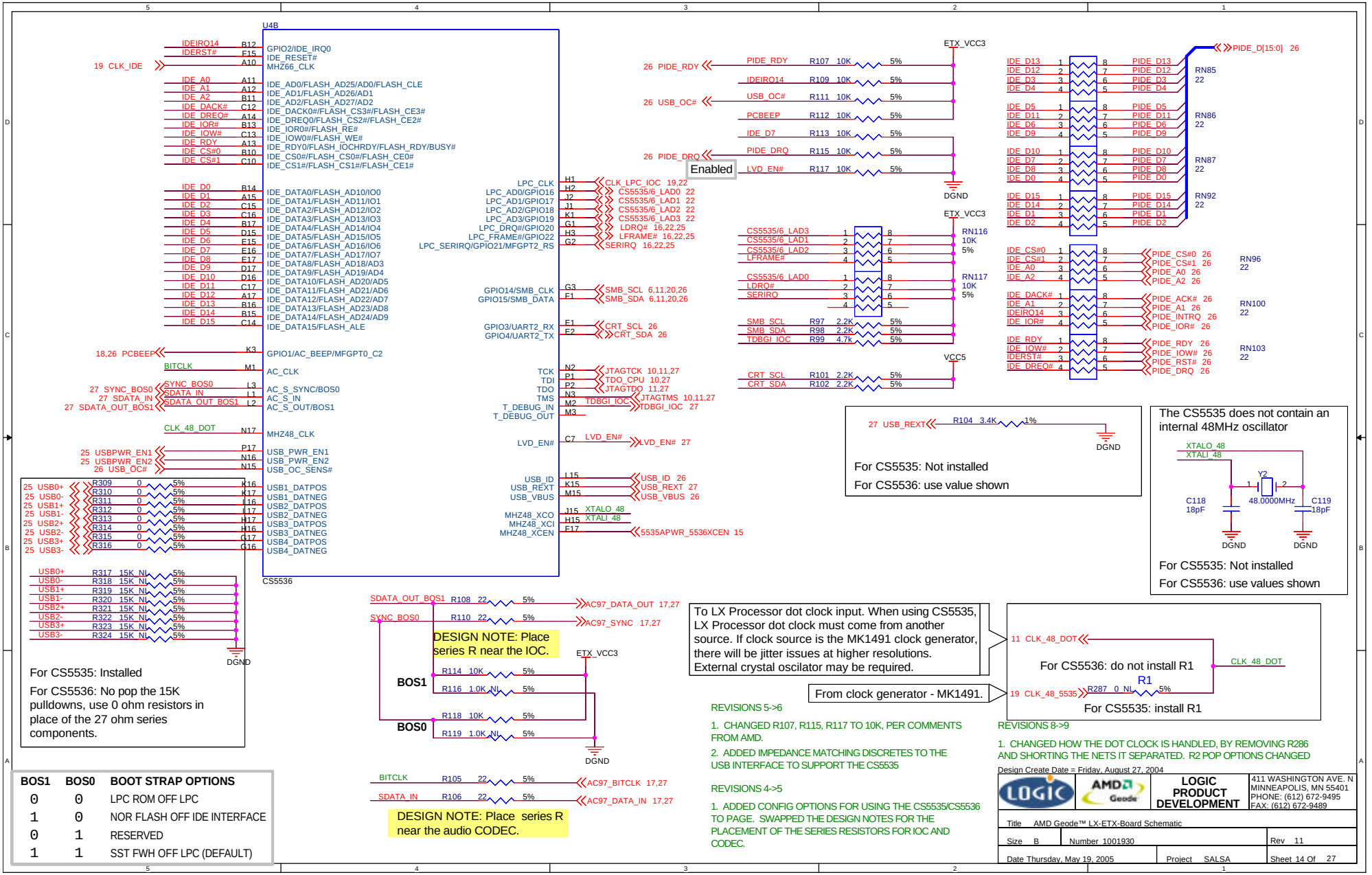
U4B
CS5536
GPIO2/IDE_IRQ0
IDE_RESET#
MHZ66_CLK
IDE_AD0/FLASH_AD25/AD0/FLASH_CLE
IDE_AD1/FLASH_AD26/AD1
IDE_AD2/FLASH_AD27/AD2
IDE_DACK0#/FLASH_CS3#/FLASH_CE3#
IDE_DREQ0/FLASH_CS2#/FLASH_CE2#
IDE_IOR0#/FLASH_RE#
IDE_IOW0#/FLASH_WE#
IDE_RDY0/FLASH_IOCHRDY/FLASH_RDY/BUSY#
IDE_CS0#/FLASH_CS0#/FLASH_CE0#
IDE_CS1#/FLASH_CS1#/FLASH_CE1#
IDE_DATA0/FLASH_AD10/IO0
IDE_DATA1/FLASH_AD11/IO1
IDE_DATA2/FLASH_AD12/IO2
IDE_DATA3/FLASH_AD13/IO3
IDE_DATA4/FLASH_AD14/IO4
IDE_DATA5/FLASH_AD15/IO5
IDE_DATA6/FLASH_AD16/IO6
IDE_DATA7/FLASH_AD17/IO7
IDE_DATA8/FLASH_AD18/AD3
IDE_DATA9/FLASH_AD19/AD4
IDE_DATA10/FLASH_AD20/AD5
IDE_DATA11/FLASH_AD21/AD6
IDE_DATA12/FLASH_AD22/AD7
IDE_DATA13/FLASH_AD23/AD8
IDE_DATA14/FLASH_AD24/AD9
IDE_DATA15/FLASH_ALE
GPIO1/AC_BEEP/MFGPT0_C2
AC_CLK
AC_S_SYNC/BOS0
AC_S_IN
AC_S_OUT/BOS1
MHZ48_CLK
USB_PWR_EN1
USB_PWR_EN2
USB_OC_SENS#
USB1_DATPOS
USB1_DATNEG
USB2_DATPOS
USB2_DATNEG
USB3_DATPOS
USB3_DATNEG
USB4_DATPOS
USB4_DATNEG
LPC_CLK
LPC_AD0/GPIO16
LPC_AD1/GPIO17
LPC_AD2/GPIO18
LPC_AD3/GPIO19
LPC_DRQ#/GPIO20
LPC_FRAME#/GPIO22
LPC_SERIRQ/GPIO21/MFGPT2_RS
GPIO14/SMB_CLK
GPIO15/SMB_DATA
GPIO3/UART2_RX
GPIO4/UART2_TX
TCK
TDI
TDO
TMS
T_DEBUG_IN
T_DEBUG_OUT
LVD_EN#
USB_ID
USB_REXT
USB_VBUS
MHZ48_XCO
MHZ48_XCI
MHZ48_XCEN
ETX_VCC3
DGND
VCC5
Enabled
For CS5535: Installed
For CS5536: No pop the 15K pulldowns, use 0 ohm resistors in place of the 27 ohm series components.
BOS1 BOS0 BOOT STRAP OPTIONS
0 0 LPC ROM OFF LPC
1 0 NOR FLASH OFF IDE INTERFACE
0 1 RESERVED
1 1 SST FWH OFF LPC (DEFAULT)
DESIGN NOTE: Place series R near the IOC.
DESIGN NOTE: Place series R near the audio CODEC.
For CS5535: Not installed
For CS5536: use value shown
The CS5535 does not contain an internal 48MHz oscillator
48.0000MHz
For CS5535: Not installed
For CS5536: use values shown
To LX Processor dot clock input. When using CS5535, LX Processor dot clock must come from another source. If clock source is the MK1491 clock generator, there will be jitter issues at higher resolutions. External crystal oscilator may be required.
From clock generator - MK1491.
For CS5536: do not install R1
For CS5535: install R1
REVISIONS 5->6
1. CHANGED R107, R115, R117 TO 10K, PER COMMENTS FROM AMD.
2. ADDED IMPEDANCE MATCHING DISCRETES TO THE USB INTERFACE TO SUPPORT THE CS5535
REVISIONS 4->5
1. ADDED CONFIG OPTIONS FOR USING THE CS5535/CS5536 TO PAGE. SWAPPED THE DESIGN NOTES FOR THE PLACEMENT OF THE SERIES RESISTORS FOR IOC AND CODEC.
REVISIONS 8->9
1. CHANGED HOW THE DOT CLOCK IS HANDLED, BY REMOVING R286 AND SHORTING THE NETS IT SEPARATED. R2 POP OPTIONS CHANGED
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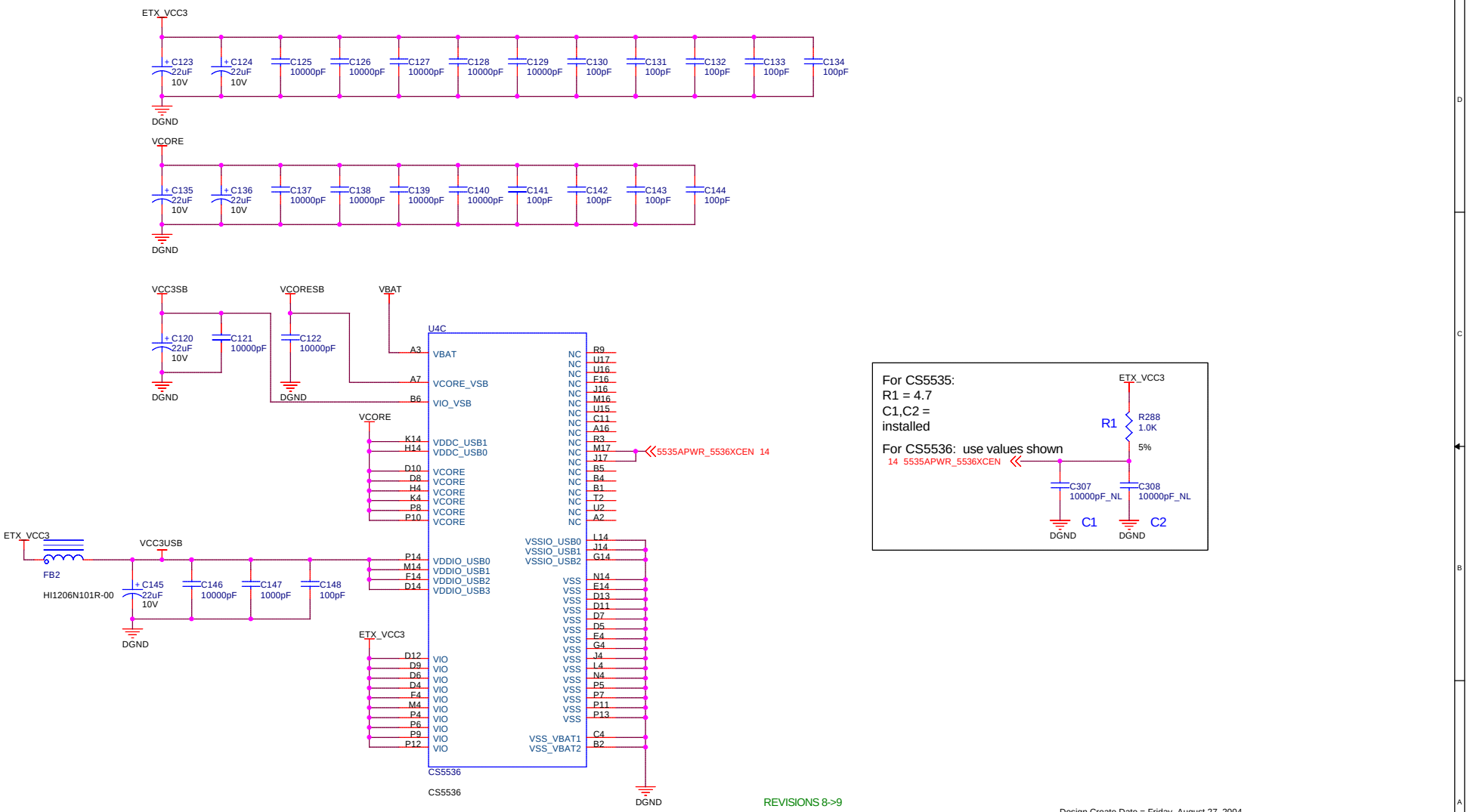

REVISIONS 8->9

1. CHANGED NOTE FOR CS5535 POP OPTIONS FOR R1 TO 4.7 OHM

REVISIONS 5->6

1. REMOVED SEPARATE CORE SUPPLY FOR THE CS5535, CHANGED NETS ON U4C K14 DOWN TO P10 TO VCORE, CHANGED NET ON C135.1 TO VCORE

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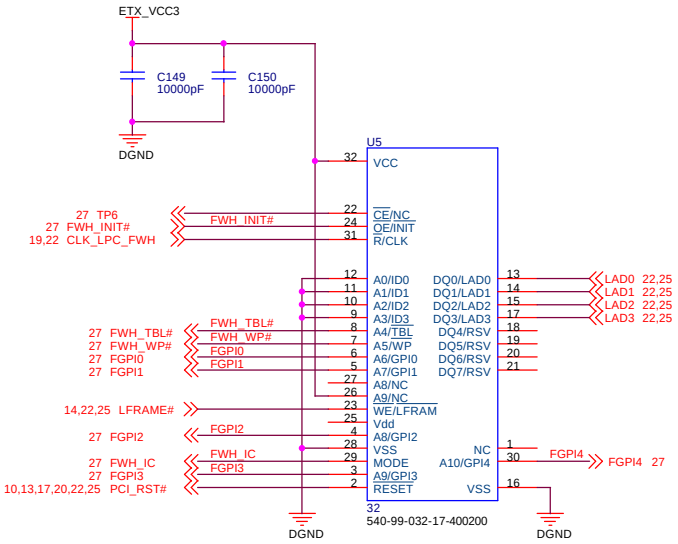
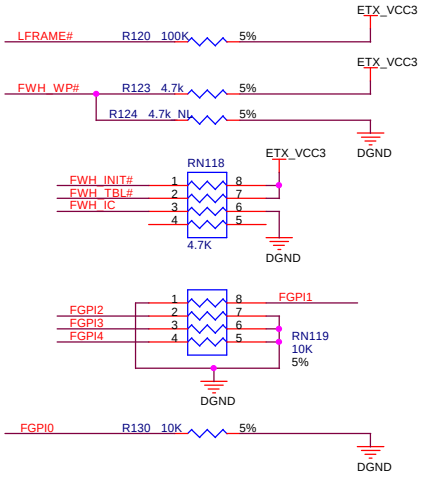
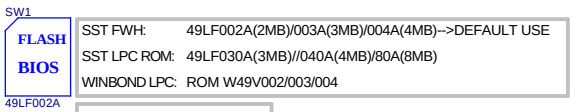




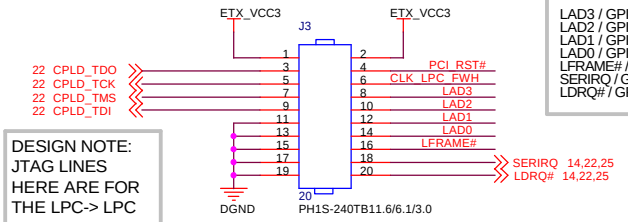


SST FWH: 49LF002A(2MB)/003A(3MB)/004A(4MB)-->DEFAULT USE

SST LPC ROM: 49LF030A(3MB)//040A(4MB)/80A(8MB)

WINBOND LPC: ROM W49V002/003/004

DESIGN NOTE: 49LF002A/03A/04A is end of life at SST



DESIGN NOTE: JTAG LINES HERE ARE FOR THE LPC-> LPC BRIDGE CPLD.

LAD3 / GPIO19
LAD2 / GPIO18
LAD1 / GPIO17
LAD0 / GPIO16
LFRAME# / GPIO22
SERIRQ / GPIO21
LDRQ# / GPIO20

DESIGN NOTE: GPIO's are the alternate function supported on the LPC Bus.

REVISIONS 9->10

1. CHANGED THE NET NAMES OF THE CPLD JTAG SIGNALS

REVISIONS 8->9

1. FIXED A HANGING NET THAT CAUSED U5.16 TO BE UNCONNECTED

REVISIONS 4->5

1. CHANGED SYMBOL OF THE PLCC CONNECTOR TO REFLECT THE FWH/LPC ROM THAT WILL BE PLUGGED INTO IT. CHANGE THE DESIGN NOT ABOUT GPIOS TO REFLECT THE CORRECT GPIOS.

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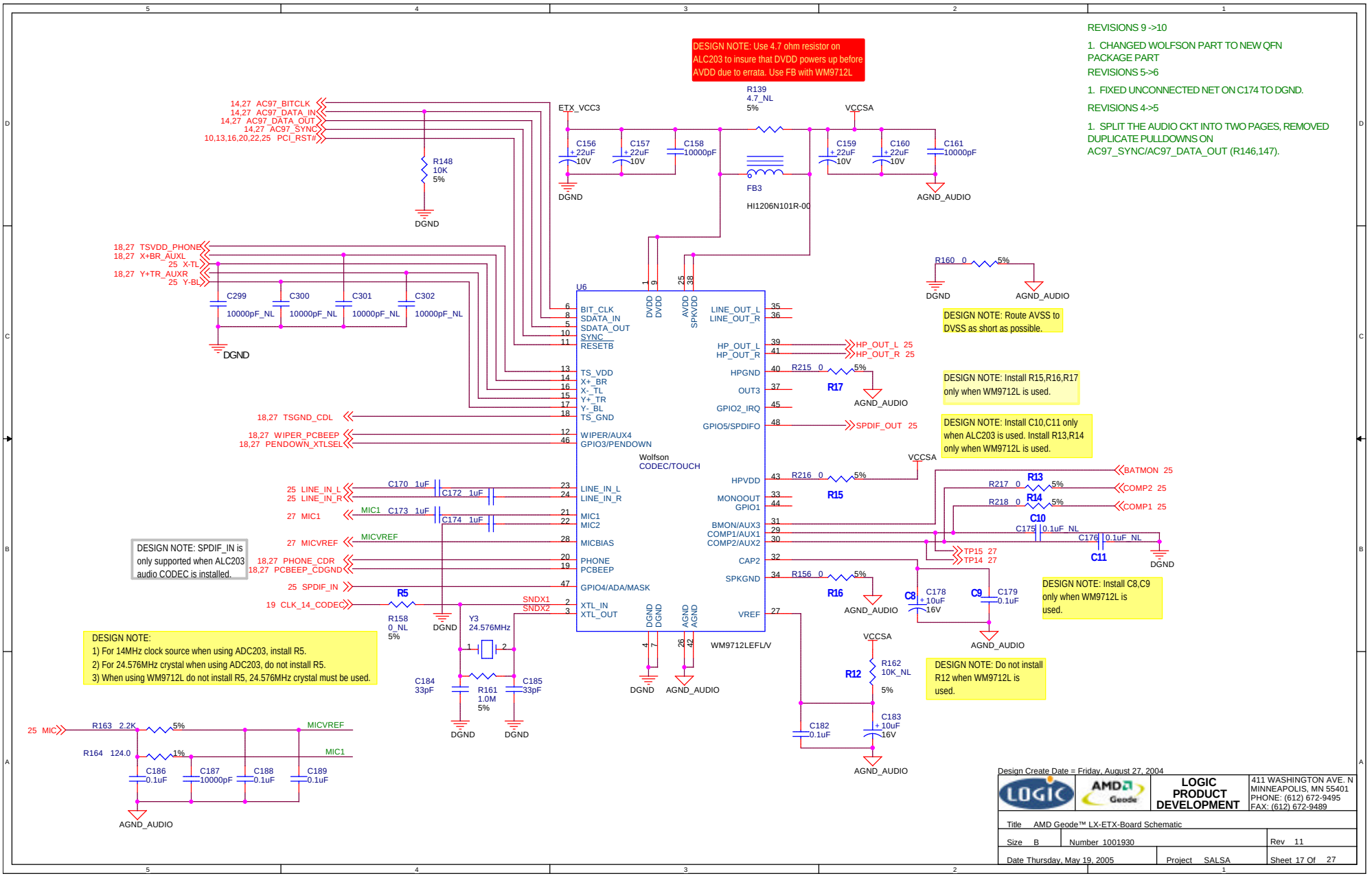
DESIGN NOTE: Use 4.7 ohm resistor on ALC203 to insure that DVDD powers up before AVDD due to errata. Use FB with WM9712L
REVISIONS 9 ->10
1. CHANGED WOLFSON PART TO NEW QFN PACKAGE PART
REVISIONS 5->6
1. FIXED UNCONNECTED NET ON C174 TO DGND.
REVISIONS 4->5
1. SPLIT THE AUDIO CKT INTO TWO PAGES, REMOVED DUPLICATE PULLDOWNS ON AC97_SYNC/AC97_DATA_OUT (R146,147).
U6
Wolfson CODEC/TOUCH
WM9712LEFL/V
DESIGN NOTE: Route AVSS to DVSS as short as possible.
DESIGN NOTE: Install R15,R16,R17 only when WM9712L is used.
DESIGN NOTE: Install C10,C11 only when ALC203 is used. Install R13,R14 only when WM9712L is used.
DESIGN NOTE: Install C8,C9 only when WM9712L is used.
DESIGN NOTE: Do not install R12 when WM9712L is used.
DESIGN NOTE: SPDIF_IN is only supported when ALC203 audio CODEC is installed.
DESIGN NOTE:
1) For 14MHz clock source when using ADC203, install R5.
2) For 24.576MHz crystal when using ADC203, do not install R5.
3) When using WM9712L do not install R5, 24.576MHz crystal must be used.
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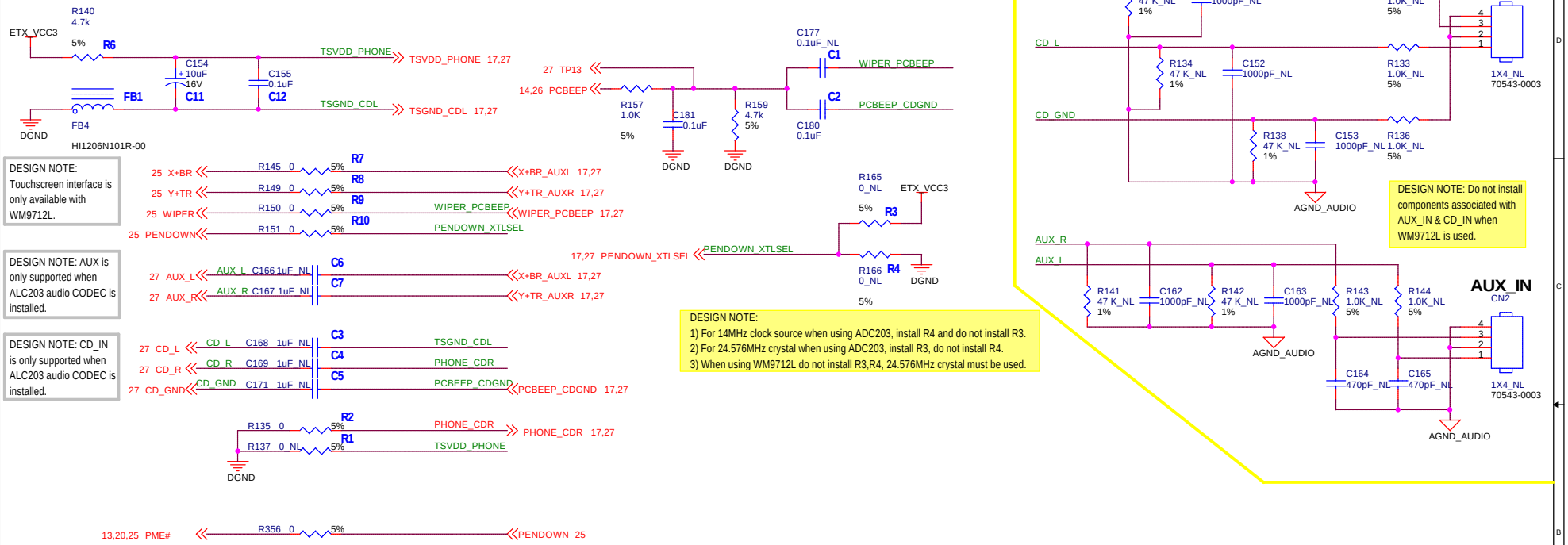
ADC203		WM9712L	
INSTALLED	NOT INSTALLED	INSTALLED	NOT INSTALLED
C1,C3,C4,C5 C6,C7,R1	C2,R2,R6,R7 R8,FB1,R9,R10 C11,C12	C2,R2,R6,R7 R8,FB1,R9,R10 C11,C12	C1,C3,C4,C5 C6,C7,R1



REVISIONS 8 ->9

1. ADDED 0 OHM BETWEEN PENDOWN AND PME# TO CONNECT PME# TO PENDOWN TO WAKE ON TOUCH. THE ZERO OHM WAS USED TO MAINTAIN CONSISTANCY WITH NET NAMES.

REVISIONS 4->5

1. SPLIT THE AUDIO CKT INTO TWO PAGES.

2. REMOVED NOTE IN THE CONNECTORS SECTION THAT REGARDED SLIGHT DIFFERENCES IN THE VALUES OF THE DISCRETES USED. THIS WAS FOR INFO ONLY DURING THE PROCESS OF INITIAL DESIGN.

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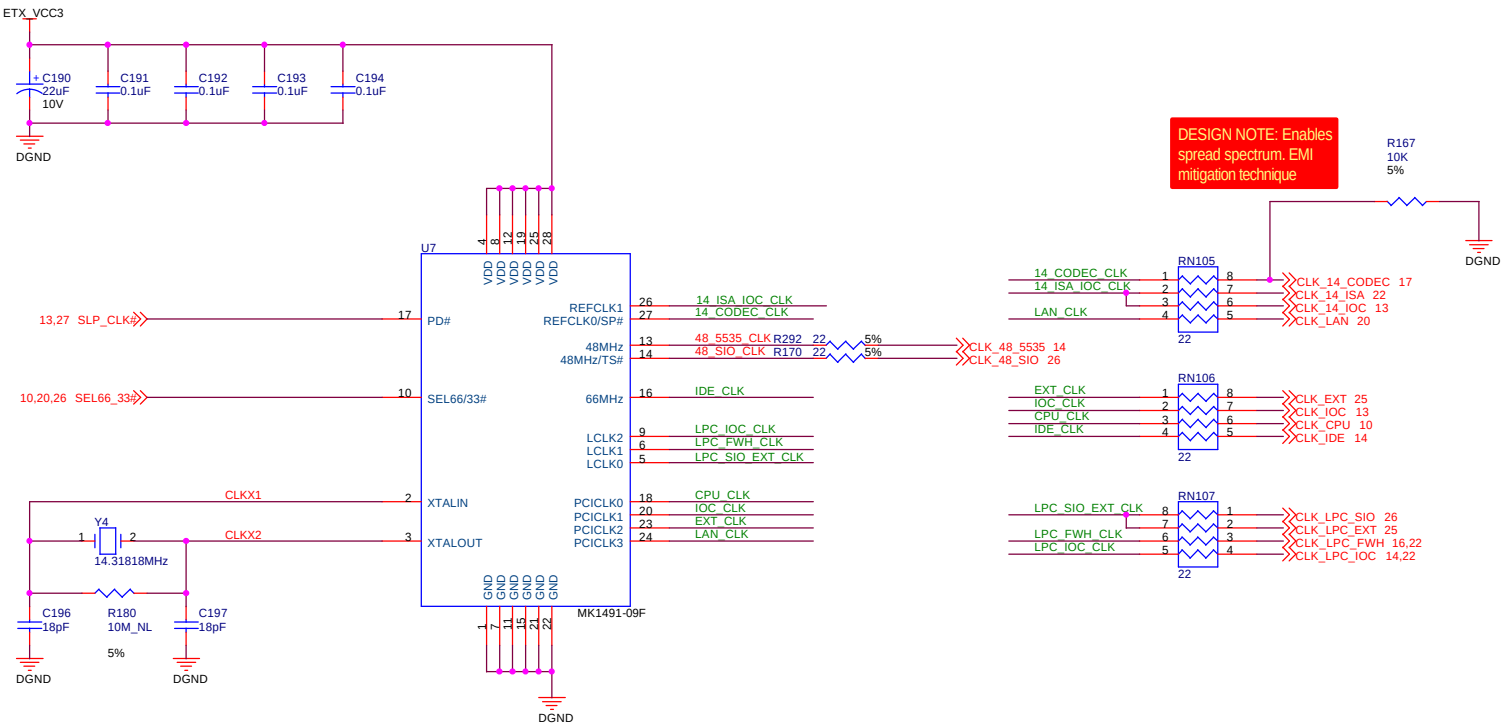

REVISIONS 4->5

1. CHANGED ALL SERIES 22OHM RESISTOR TO RPAKS, REMOVED FERRITE BEAD AND CHANGED VALUE OF DECOUPLING CAPS TO .1uF FROM .01uF.

REVISIONS 8->9

1. removed the alias VCLK and its offpage connector from the CLOCK Gen page and the testpoint page

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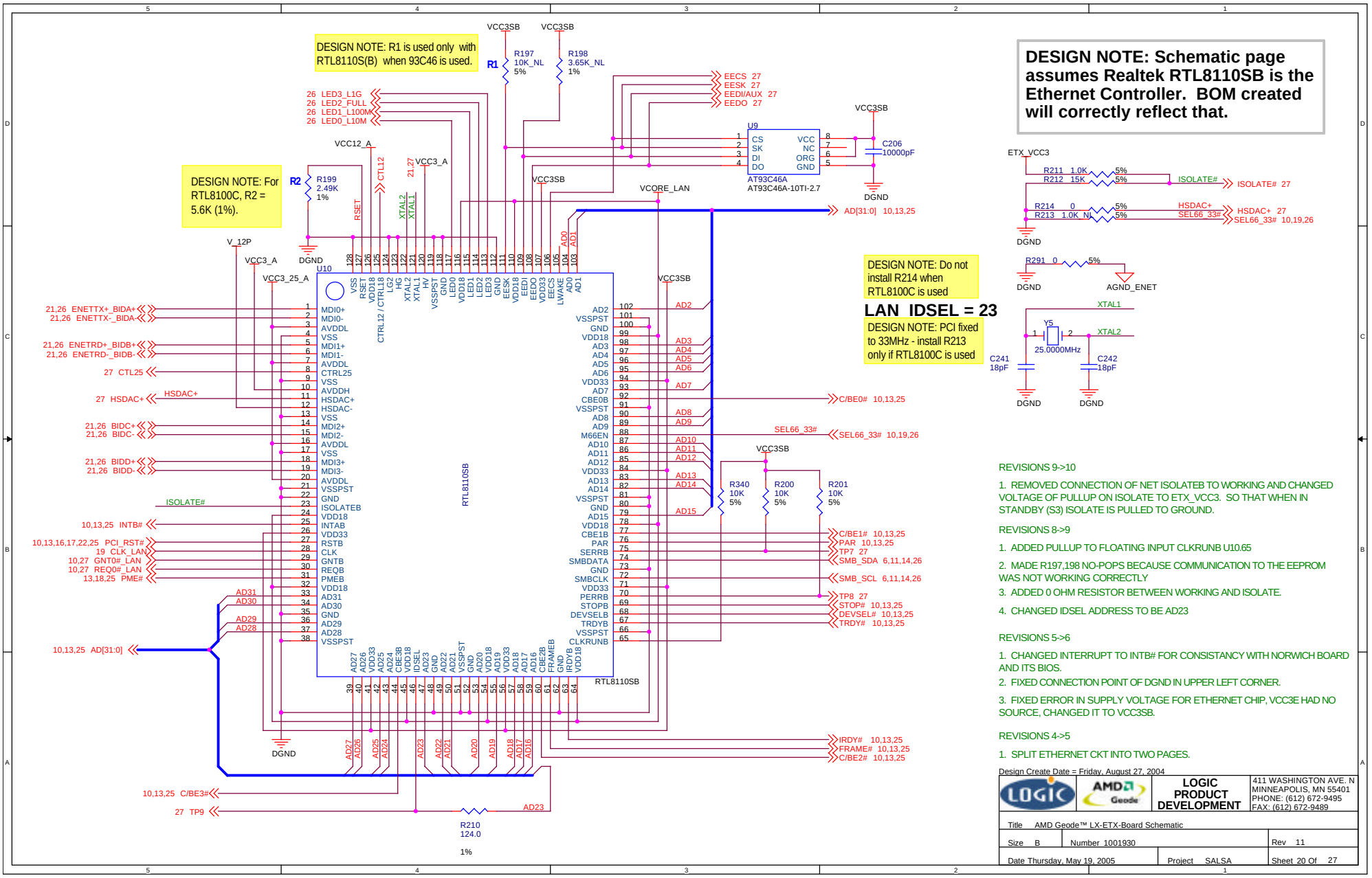

REVISIONS 9->10

1. REMOVED CONNECTION OF NET ISOLATEB TO WORKING AND CHANGED VOLTAGE OF PULLUP ON ISOLATE TO ETX_VCC3. SO THAT WHEN IN STANDBY (S3) ISOLATE IS PULLED TO GROUND.

REVISIONS 8->9

1. ADDED PULLUP TO FLOATING INPUT CLKRUNB U10.65
2. MADE R197,198 NO-POPS BECAUSE COMMUNICATION TO THE EEPROM WAS NOT WORKING CORRECTLY
3. ADDED 0 OHM RESISTOR BETWEEN WORKING AND ISOLATE.
4. CHANGED IDSEL ADDRESS TO BE AD23

REVISIONS 5->6

1. CHANGED INTERRUPT TO INTB# FOR CONSISTANCY WITH NORWICH BOARD AND ITS BIOS.
2. FIXED CONNECTION POINT OF DGND IN UPPER LEFT CORNER.
3. FIXED ERROR IN SUPPLY VOLTAGE FOR ETHERNET CHIP, VCC3E HAD NO SOURCE, CHANGED IT TO VCC3SB.

REVISIONS 4->5

1. SPLIT ETHERNET CKT INTO TWO PAGES.

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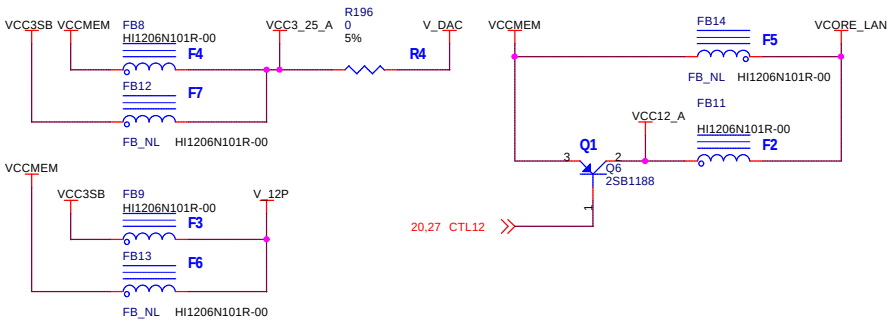
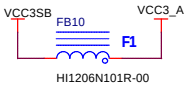
RTL8110SB		RTL8100C	
INSTALLED	NOT INSTALLED	INSTALLED	NOT INSTALLED
F1,F2,F3,F4 Q1,R4	F5,F6,F7	F5,F6,F7	F1,F2,F3,F4 Q1,R4

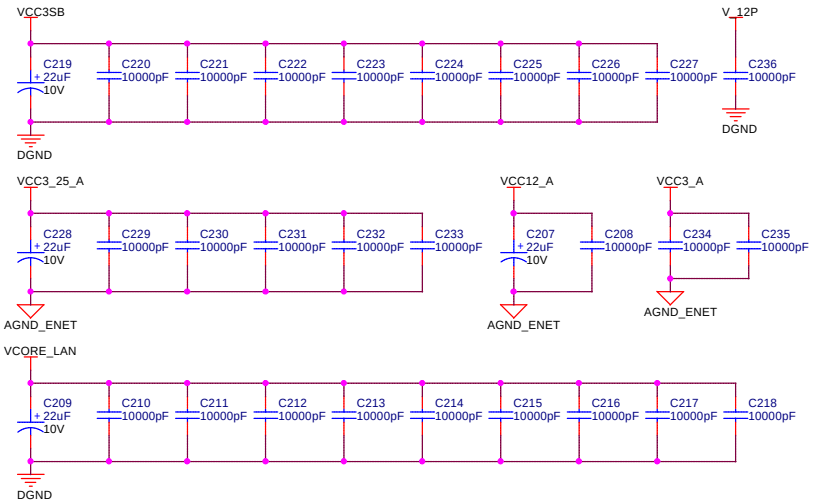
DESIGN NOTE: Schematic page assumes Realtek RTL8110SB is the Ethernet Controller. BOM created will correctly reflect that.

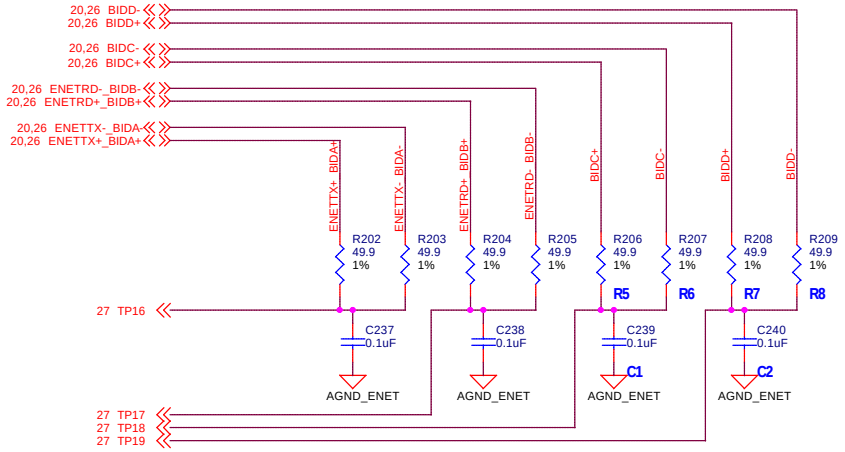
EDITOR NOTE: Need a voltage sequenceing diagram for the entire system.

DESIGN NOTE: VCC12 and VCC12_A could be supplied from VCORESB or VCORE. If VCORESB is used, the VCORESB supply must be beefed up.









DESIGN NOTE: For RTL8100C application, remove R5, R6, R7, R8, C1, C2.

REVISIONS 5->6

1. FIXED ERROR IN SUPPLY VOLTAGE FOR ETHERNET CHIP, VCC3E HAD NO SOURCE, CHANGED IT TO VCC3SB. FIXED ERROR IN THE DESIGNATORS FOR THE POPULATION OPTION F1-7 WERE ASSIGNED INCORRECTLY.

REVISIONS 4->5

1. SPLIT ETHERNET CKT INTO TWO PAGES. FIXED DISCONNECTED NET ENETRD-_DIDB- => R205.

Design Create Date = Friday, August 27, 2004

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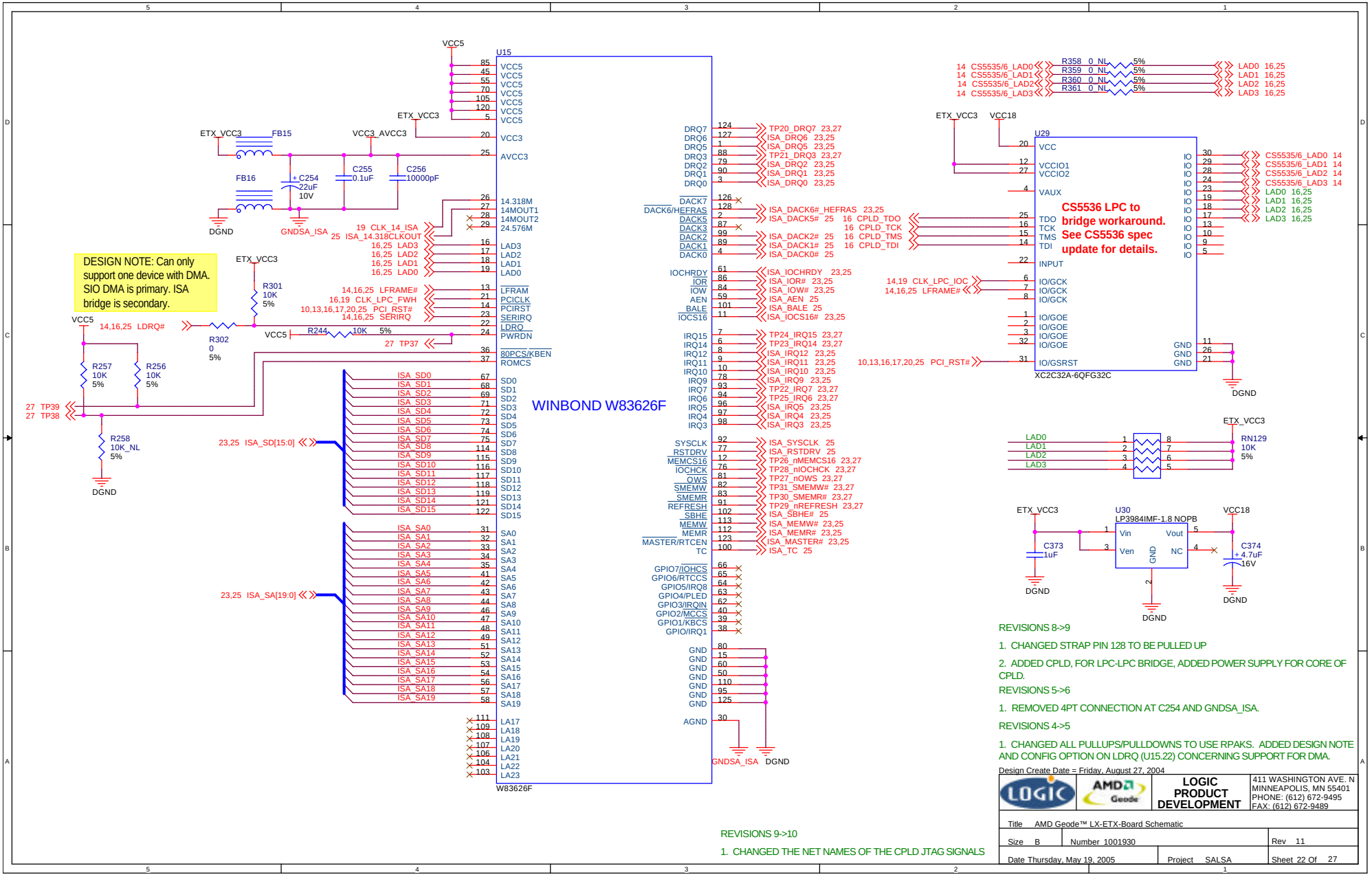
Title	AMD Geode™ LX-ETX-Board Schematic		
Size B	Number 1001930		Rev 11
Date Thursday, May 19, 2005		Project SALSA	Sheet 21 Of 27


U15
WINBOND W83626F
W83626F
DESIGN NOTE: Can only support one device with DMA. SIO DMA is primary. ISA bridge is secondary.
U29
XC2C32A-6QFG32C
CS5536 LPC to bridge workaround. See CS5536 spec update for details.
U30
LP3984IMF-1.8 NOPB
REVISIONS 8->9
1. CHANGED STRAP PIN 128 TO BE PULLED UP
2. ADDED CPLD, FOR LPC-LPC BRIDGE, ADDED POWER SUPPLY FOR CORE OF CPLD.
REVISIONS 5->6
1. REMOVED 4PT CONNECTION AT C254 AND GNDSA_ISA.
REVISIONS 4->5
1. CHANGED ALL PULLUPS/PULLDOWNS TO USE RPAKS. ADDED DESIGN NOTE AND CONFIG OPTION ON LDRQ (U15.22) CONCERNING SUPPORT FOR DMA.
REVISIONS 9->10
1. CHANGED THE NET NAMES OF THE CPLD JTAG SIGNALS
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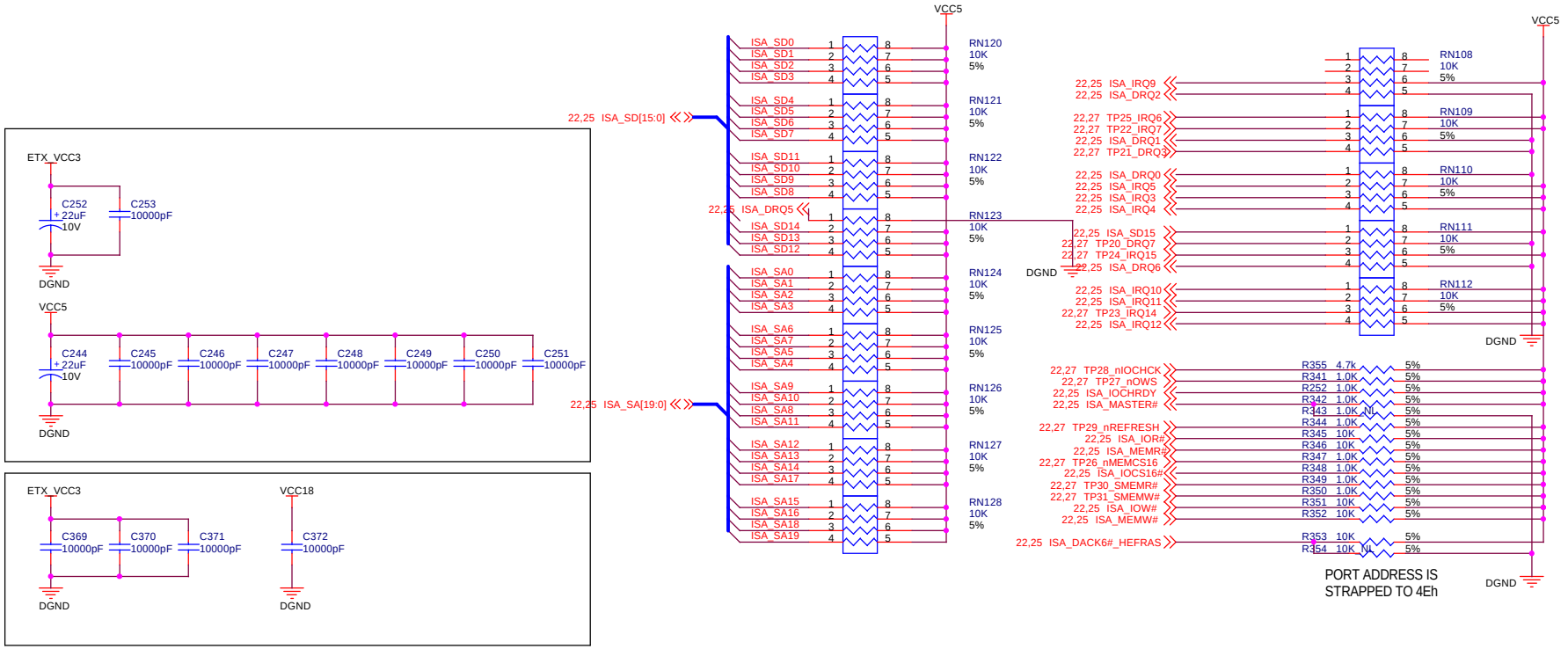

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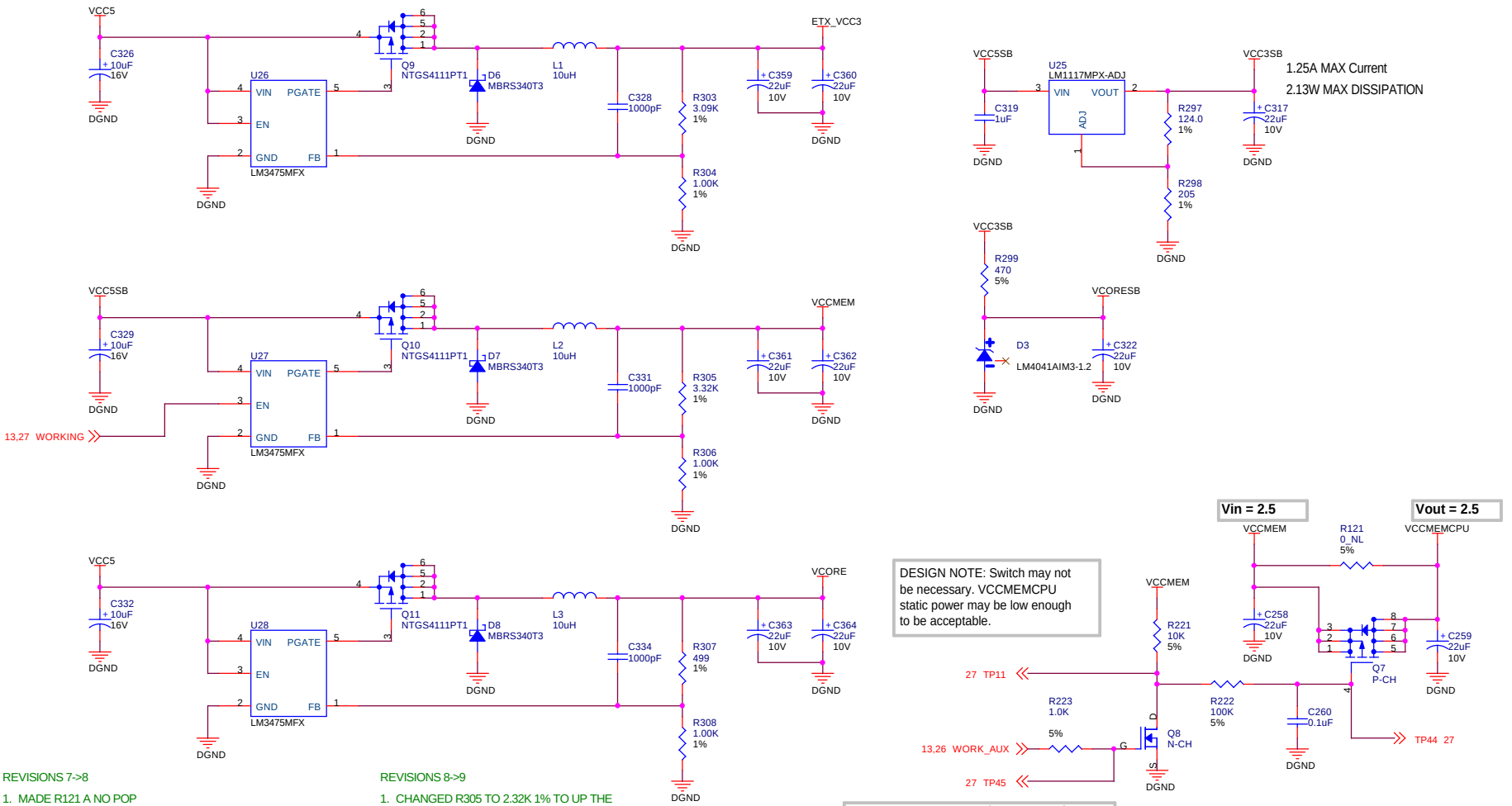

DESIGN NOTE: Switch may not be necessary. VCCMEMCPU static power may be low enough to be acceptable.

DESIGN NOTE: GPIO24/WORK_AUX is an open drain output, which requires a pullup resistor to achieve a high state. At initial standby power application the GPIO24/WORK_AUX pin defaults to GPIO24 and the GPIO24 defaults as an input. This default combination will leave the pin in a high state due to the pullup which is normally connected to VCC3SB and may not the desired behavior.

REVISIONS 7->8

1. MADE R121 A NO POP

REVISIONS 5->6

1. CHANGED R300 TO A 1206 1/4W PACKAGE
2. CHANGED R305 FROM 2.15K TO 2.26K TO ADJ THE VCCMEM VOLTAGE TO 2.6V

REVISIONS 4->5

1. THIS PAGE IS COMPLETELY REDESIGNED TO USE SWITCHERS INSTEAD OF A SHUNT/FET LINEAR SOLUTION.
2. ADDEDD VCCMEM/VCCMEMCPU SWITCH TO THIS PAGE, ADDED 0 OHM BETWEEN VCCMEM/VCCMEMCPU. FIXED TEXT ON INPUT TO SAY Vin = 2.5V.

REVISIONS 8->9

1. CHANGED R305 TO 2.32K 1% TO UP THE VCCMEM VOLTAGE TO 2.6V

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Title	AMD Geode™ LX-ETX-Board Schematic		
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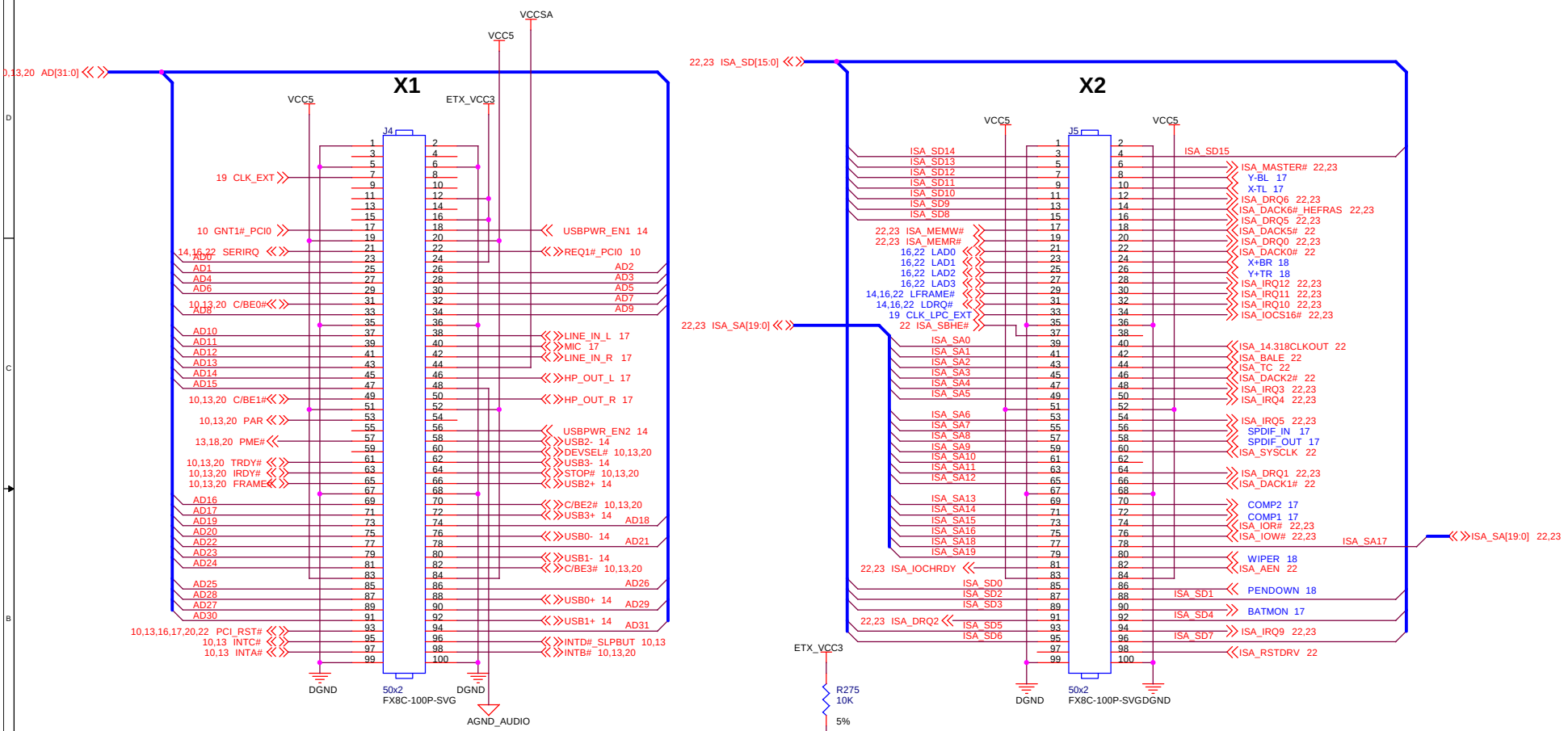

DESIGN NOTE: Touchscreen support when using Wolfson WM9712L.

DESIGN NOTE: Battery moniter support when using Wolfson WM9712L.

REVISIONS 5->6

1. REMOVED DUPLICATE NET SEL66_33# FROM J4.55

REVISIONS 4->5

1. FIXED PAGE SIZE ISSUE.

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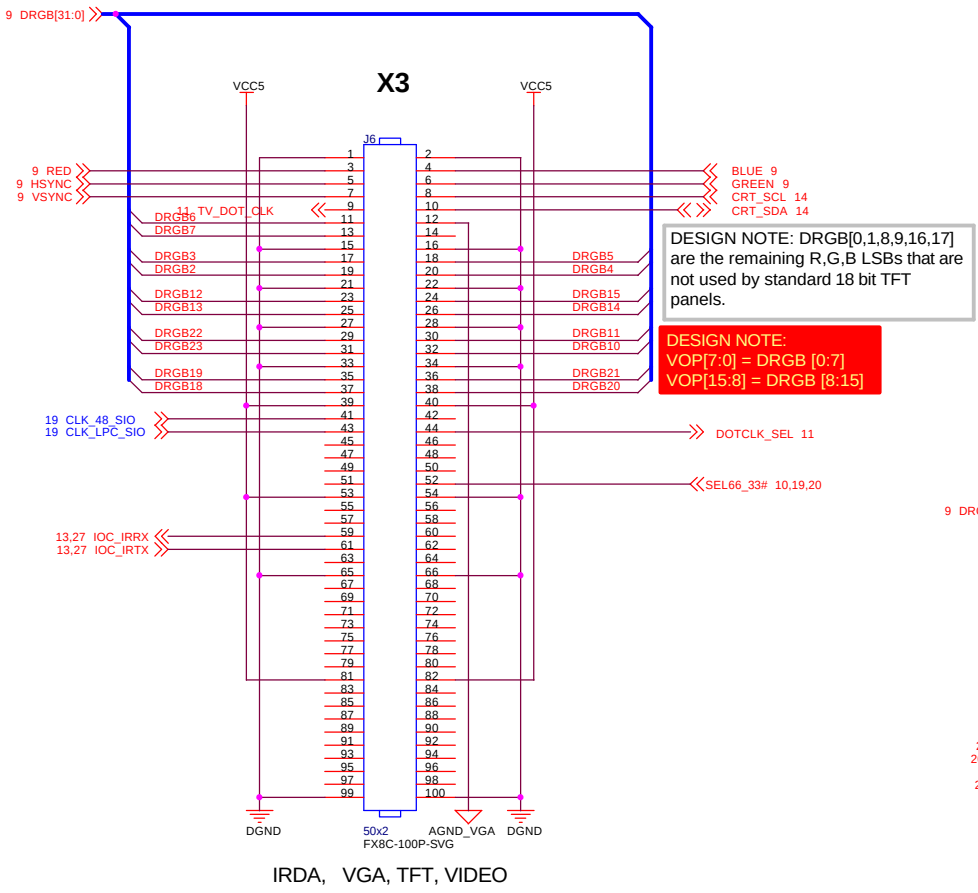
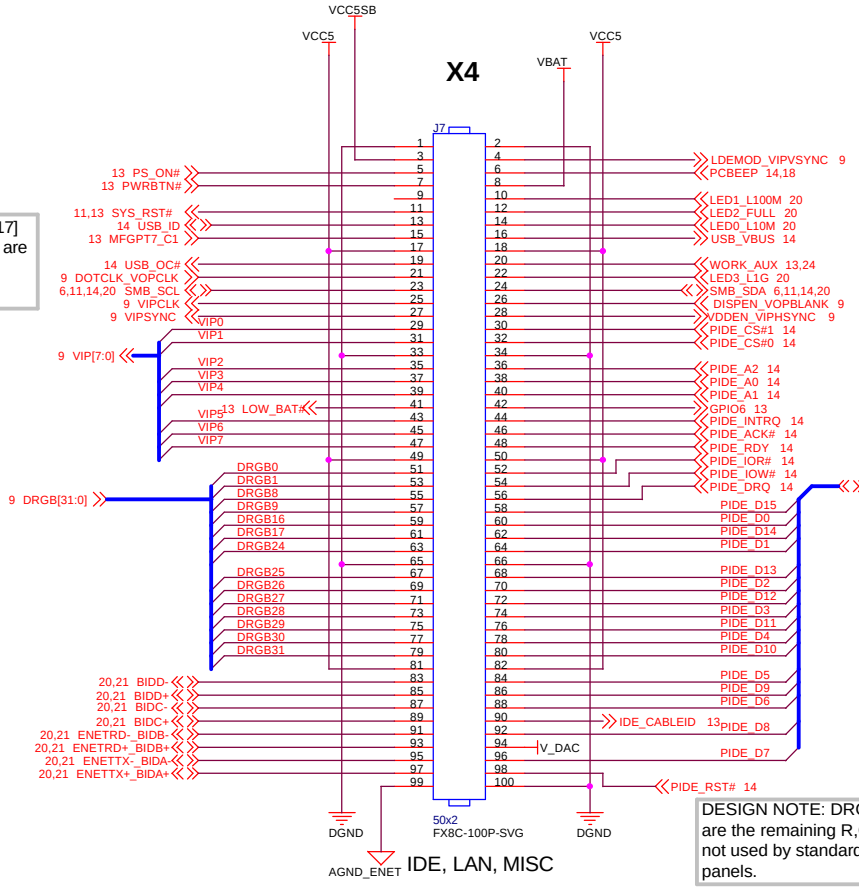


IRDA, VGA, TFT, VIDEO

DESIGN NOTE: DRGB[0,1,8,9,16,17] are the remaining R,G,B LSBs that are not used by standard 18 bit TFT panels.

DESIGN NOTE:
VOP[7:0] = DRGB [0:7]
VOP[15:8] = DRGB [8:15]



IDE, LAN, MISC

DESIGN NOTE: DRGB[0,1,8,9,16,17] are the remaining R,G,B LSBs that are not used by standard 18 bit TFT panels.

DESIGN NOTE: VOP[23..0] is pin multiplexed on DRGB[0..23] from the GX3. VOP0 is on DRGB23 and so on.

DESIGN NOTE: VIP[8..15] is pin multiplexed on DRGB[24..31] from the GX3

REVISIONS 8->9

1. RENAMED THE NETS: LDEMOD_VIPHSYNC WAS RENAMED TO LDEMOD_VIPVSYNC. VDDEN_VIPVSYNC WAS RENAMED TO VDDEN_VIPHSYNC.

REVISIONS 5->6

1. CHANGED NET FOCUS_DOT_CLK NAME TO TV_DOT_CLK.

REVISIONS 4->5

1. REMOVED NETS SIO_IRTX/SIO_IRRX MOVED MUXING TO THE BASEBOARD. CHANGED NET NAME OF IRTX/IRRX TO IOC_IRTX/IOC_IRRX.

2. ADDED NET FOCUS_DOT_CLK TO THE MIX J6.9. FIXED UNCONNECTED NET DRGB28 TO THE BUS.

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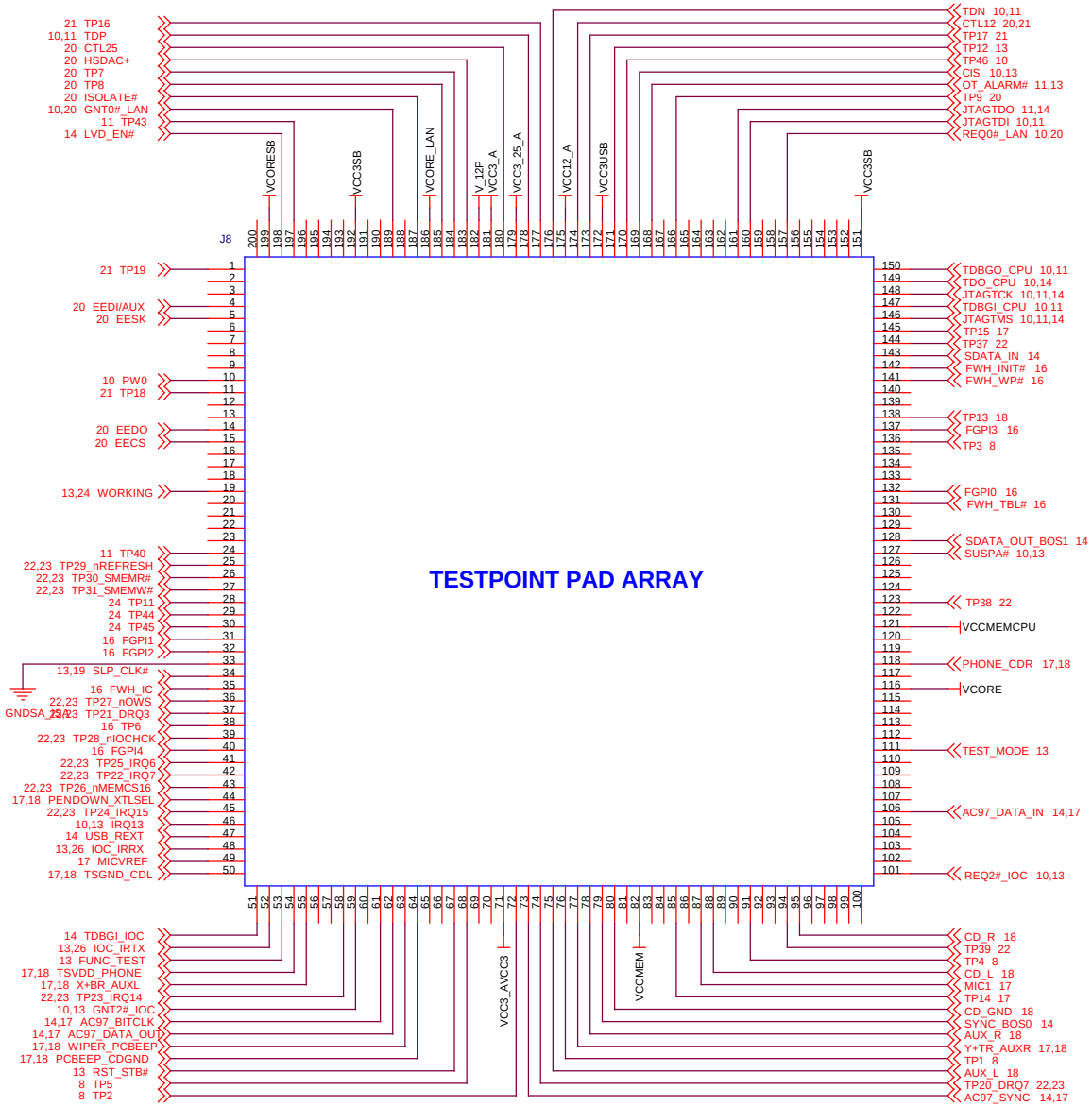

REVISIONS 9->10

1. REMOVED TP42

REVISIONS 4->5

1. CHANGED LOCAL SYMBOL FOR TESTPOINT ARRAY SUCH THAT THE PAGE SIZE COULD BE CHANGED TO SIZE B.

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Title AMD Geode™ LX-ETX-Board Schematic			
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Reference Designator to Schematic Cross List

Format: REFDES PAGE:X.Y VALUE

C

C1	8:4.A	0.1UF
C2	7:4.D	22UF
C3	7:4.D	22UF
C4	7:4.D	100PF
C5	7:4.D	100PF
C6	7:4.D	100PF
C7	7:3.D	100PF
C8	7:3.D	1000PF
C9	7:3.D	1000PF
C10	7:3.D	1000PF
C11	7:3.D	1000PF
C12	7:2.D	10000PF
C13	7:2.D	10000PF
C14	7:2.D	10000PF
C15	7:2.D	10000PF
C16	7:4.D	22UF
C17	7:4.D	22UF
C18	7:4.D	100PF
C19	7:4.D	100PF
C20	7:4.D	100PF
C21	7:3.D	100PF
C22	7:3.D	1000PF
C23	7:3.D	1000PF
C24	7:3.D	1000PF
C25	7:3.D	1000PF
C26	7:2.D	10000PF
C27	7:2.D	10000PF
C28	7:2.D	10000PF
C29	7:2.D	10000PF
C32	9:2.C	10000PF
C34	9:2.C	10UF
C35	9:2.B	10000PF
C37	10:3.C	10000PF
C38	10:2.C	10000PF
C40	10:3.B	10000PF
C41	10:2.B	10000PF
C43	10:3.B	10000PF
C44	10:2.B	10000PF
C46	10:4.B	220PF
C47	10:4.B	220PF
C48	10:3.B	220PF
C49	11:3.B	10000PF
C50	11:4.A	1000PF
C51	12:3.D	22UF
C52	12:3.D	22UF
C53	12:3.D	22UF
C54	12:3.D	10000PF
C55	12:2.D	10000PF
C56	12:2.D	10000PF
C57	12:2.D	10000PF
C58	12:3.D	1000PF
C59	12:3.D	1000PF
C60	12:2.D	1000PF
C61	12:2.D	1000PF
C62	12:2.D	100PF
C63	12:2.D	100PF
C64	12:2.D	100PF
C65	12:1.D	100PF
C66	12:3.C	22UF
C67	12:3.C	22UF
C68	12:3.C	22UF
C69	12:3.C	10000PF
C70	12:2.C	10000PF
C71	12:2.C	10000PF
C72	12:2.C	10000PF
C73	12:3.C	1000PF
C74	12:3.C	1000PF
C75	12:2.C	1000PF
C76	12:2.C	1000PF
C77	12:2.C	100PF
C78	12:2.C	100PF
C79	12:2.C	100PF
C80	12:1.C	100PF
C81	12:3.C	22UF
C82	12:3.C	22UF
C83	12:3.C	22UF
C84	12:3.C	10000PF
C85	12:2.C	10000PF
C86	12:2.C	10000PF
C87	12:2.C	10000PF
C88	12:2.C	10000PF
C89	12:1.C	10000PF
C90	12:3.B	100PF
C91	12:3.B	100PF
C92	12:2.B	100PF
C93	12:2.B	100PF
C94	12:2.B	100PF
C95	12:2.B	100PF
C96	12:3.B	22UF
C97	12:3.B	22UF
C98	12:3.B	22UF
C99	12:3.B	10000PF
C100	12:2.B	10000PF
C101	12:2.B	10000PF
C102	12:2.B	10000PF
C103	12:2.B	10000PF
C104	12:1.B	10000PF
C105	12:3.A	100PF
C106	12:3.A	100PF
C107	12:2.A	100PF
C108	12:2.A	100PF
C109	12:2.A	100PF
C110	12:2.A	100PF
C114	13:3.A	0.1UF
C115	13:4.A	4.7UF
C116	13:1.C	18PF
C117	13:1.C	18PF
C118	14:1.B	18PF
C119	14:1.B	18PF
C120	15:5.C	22UF
C121	15:5.C	10000PF
C122	15:4.C	10000PF
C123	15:5.D	22UF
C124	15:5.D	22UF
C125	15:4.D	10000PF
C126	15:4.D	10000PF
C127	15:4.D	10000PF
C128	15:4.D	10000PF
C129	15:4.D	10000PF
C130	15:4.D	100PF
C131	15:3.D	100PF
C132	15:3.D	100PF
C133	15:3.D	100PF
C134	15:3.D	100PF
C135	15:5.D	22UF
C136	15:5.D	22UF
C137	15:4.D	10000PF
C138	15:4.D	10000PF
C139	15:4.D	10000PF
C140	15:4.D	10000PF
C141	15:4.D	100PF
C142	15:4.D	100PF
C143	15:3.D	100PF
C144	15:3.D	100PF
C145	15:5.B	22UF
C146	15:5.B	10000PF
C147	15:5.B	1000PF
C148	15:4.B	100PF
C149	16:4.D	10000PF
C150	16:4.D	10000PF
C151	18:2.D	1000PF
C152	18:2.D	1000PF
C153	18:1.D	1000PF
C154	18:5.D	10UF
C155	18:5.D	0.1UF
C156	17:3.D	22UF
C157	17:3.D	22UF
C158	17:3.D	10000PF
C159	17:2.D	22UF
C160	17:2.D	22UF
C161	17:2.D	10000PF
C162	18:2.C	1000PF
C163	18:1.C	1000PF
C164	18:1.C	470PF
C165	18:1.C	470PF
C166	18:4.C	1UF
C167	18:4.C	1UF
C168	18:4.C	1UF
C169	18:4.C	1UF
C170	17:4.B	1UF
C171	18:4.C	1UF
C172	17:4.B	1UF
C173	17:4.B	1UF
C174	17:4.B	1UF
C175	17:2.B	0.1UF
C176	17:1.B	0.1UF
C177	18:3.D	0.1UF
C178	17:2.B	10UF
C179	17:2.B	0.1UF
C180	18:3.D	0.1UF
C181	18:3.D	0.1UF
C182	17:3.A	0.1UF
C183	17:2.A	10UF
C184	17:4.A	33PF
C185	17:4.A	33PF
C186	17:5.A	0.1UF
C187	17:5.A	10000PF
C188	17:5.A	0.1UF
C189	17:4.A	0.1UF
C190	19:5.D	22UF
C191	19:5.D	0.1UF
C192	19:4.D	0.1UF
C193	19:4.D	0.1UF
C194	19:4.D	0.1UF
C196	19:5.B	18PF
C197	19:4.B	18PF
C206	20:2.D	10000PF
C207	21:4.B	22UF
C208	21:4.B	10000PF
C209	21:5.A	22UF
C210	21:5.A	10000PF
C211	21:5.A	10000PF
C212	21:5.A	10000PF
C213	21:5.A	10000PF
C214	21:4.A	10000PF
C215	21:4.A	10000PF
C216	21:4.A	10000PF
C217	21:4.A	10000PF
C218	21:4.A	10000PF
C219	21:5.B	22UF
C220	21:5.B	10000PF
C221	21:5.B	10000PF
C222	21:5.B	10000PF
C223	21:5.B	10000PF
C224	21:4.B	10000PF
C225	21:4.B	10000PF
C226	21:4.B	10000PF
C227	21:4.B	10000PF
C228	21:5.B	22UF
C229	21:5.B	10000PF
C230	21:5.B	10000PF
C231	21:5.B	10000PF
C232	21:5.B	10000PF
C233	21:4.B	10000PF
C234	21:4.B	10000PF
C235	21:4.B	10000PF
C236	21:4.B	10000PF
C237	21:2.B	0.1UF
C238	21:2.B	0.1UF
C239	21:2.B	0.1UF
C240	21:1.B	0.1UF
C241	20:2.C	18PF
C242	20:2.C	18PF
C244	23:5.C	22UF
C245	23:5.C	10000PF
C246	23:5.C	10000PF
C247	23:5.C	10000PF
C248	23:5.C	10000PF
C249	23:4.C	10000PF
C250	23:4.C	10000PF
C251	23:4.C	10000PF
C252	23:5.C	22UF
C253	23:5.C	10000PF
C254	22:4.D	22UF
C255	22:4.D	0.1UF
C256	22:4.D	10000PF
C257	8:1.B	0.1UF
C258	24:2.B	22UF
C259	24:1.B	22UF
C260	24:2.B	0.1UF
C299	17:5.C	10000PF
C300	17:4.C	10000PF
C301	17:4.C	10000PF
C302	17:4.C	10000PF
C307	15:2.B	10000PF
C308	15:2.B	10000PF
C309	11:4.A	1000PF
C310	11:4.C	0.1UF
C317	24:2.D	22UF
C319	24:2.D	1UF
C322	24:2.C	22UF
C323	10:2.C	10UF
C324	10:2.B	10UF
C325	10:2.B	10UF
C326	24:5.D	10UF
C328	24:4.D	1000PF
C329	24:5.C	10UF
C331	24:4.C	1000PF
C332	24:5.B	10UF
C334	24:4.B	1000PF
C335	7:3.C	68PF
C336	7:3.C	68PF
C337	7:3.C	68PF
C338	7:3.C	68PF
C339	7:3.C	68PF
C340	7:3.C	68PF
C341	7:3.B	68PF
C342	7:3.B	68PF
C343	7:3.B	68PF
C344	7:3.B	68PF
C345	7:3.B	68PF
C346	7:3.B	68PF
C347	7:3.B	68PF
C348	7:3.B	68PF
C349	7:3.B	68PF
C350	7:3.B	68PF
C351	7:3.B	68PF
C352	7:3.B	68PF
C353	7:3.A	68PF
C354	7:3.A	68PF
C355	7:3.A	68PF
C356	7:3.A	68PF
C357	7:3.A	68PF
C358	7:3.A	68PF
C359	24:3.D	22UF
C360	24:3.D	22UF
C361	24:3.C	22UF
C362	24:3.C	22UF
C363	24:3.B	22UF
C364	24:3.B	22UF
C365	13:2.C	0.1UF
C366	13:1.C	12pF
C369	23:5.B	10000PF
C370	23:5.B	10000PF
C371	23:5.B	10000PF
C372	23:5.B	10000PF
C373	22:2.B	1UF
C374	22:1.B	4.7UF

CN

CN1	18:1.D	1X4
CN2	18:1.C	1X4

D

D2	9:2.B	SHUNT VOLTA‡
D3	24:2.C	SHUNT VOLTA‡
D4	13:3.C	BAT54TA
D5	13:3.C	BAT54TA
D6	24:4.D	MBRS340T3
D7	24:4.C	MBRS340T3
D8	24:4.B	MBRS340T3

FB

FB2	15:5.B	FB
FB3	17:3.D	FB
FB4	18:5.D	FB
FB8	21:5.D	FB
FB9	21:5.C	FB
FB10	21:5.C	FB
FB11	21:4.D	FB
FB12	21:5.D	FB
FB13	21:5.C	FB
FB14	21:4.D	FB
FB15	22:5.D	FERRITE BEAD
FB16	22:5.D	FERRITE BEAD

J

J1	11:4.D	14
J2	10:2.C	2
J3	16:2.B	20
J4	25:4.D	50X2
J5	25:2.D	50X2
J6	26:5.D	50X2
J7	26:2.D	50X2
J8	27:5.D	HEADER 100X‡
J9A	6:4.D	SODIMM
J9B	6:2.D	SODIMM

L

L1	24:4.D	10UH
L2	24:4.C	10UH
L3	24:4.B	10UH

Q

Q1	11:4.B	N-CH
Q4	13:4.A	N-CH
Q6	21:4.D	2SB1188
Q7	24:1.B	P-CH
Q8	24:2.B	N-CH
Q9	24:4.D	NTGS4111PT1
Q10	24:4.C	NTGS4111PT1
Q11	24:4.B	NTGS4111PT1

R

R1	9:2.C	1.0
R21	13:1.C	301K
R29	6:4.A	10.0K
R30	9:2.C	10K
R31	9:3.B	1.21K
R32	9:3.B	0
R33	10:2.D	10K
R34	10:2.D	1.0K
R35	10:2.D	10K
R36	10:2.D	1.0K
R38	10:2.D	10K
R42	10:2.D	1.0K
R43	10:2.C	1.0
R44	10:2.D	10K
R45	10:2.B	1.0
R46	10:2.D	1.0K
R47	10:2.D	10K
R48	10:2.B	1.0
R49	10:2.D	1.0K
R50	10:4.C	8.25K
R51	10:4.C	8.25K
R52	10:4.C	8.25K
R54	10:2.B	0
R55	10:2.C	1.0K
R56	10:2.A	0
R57	10:2.C	10K
R58	10:2.A	0
R59	11:4.B	124.0
R60	11:4.B	10K
R61	11:3.B	10K
R66	13:4.A	10K
R67	13:4.A	10K
R77	13:2.D	5.6K
R78	13:1.C	10.0M
R79	13:2.D	5.6K
R83	13:2.D	1.0K
R84	13:2.C	1.0K
R97	14:2.C	2.2K
R98	14:2.C	2.2K
R99	14:2.C	4.7K
R101	14:2.C	2.2K
R102	14:2.C	2.2K
R104	14:2.C	3.4K
R105	14:4.A	22
R106	14:4.A	22
R107	14:2.D	10K
R108	14:4.B	22
R109	14:2.D	10K
R110	14:4.B	22
R111	14:2.D	10K
R112	14:2.D	10K
R113	14:2.D	10K
R114	14:4.A	10K
R115	14:2.D	10K
R116	14:4.A	1.0K
R117	14:2.D	10K
R118	14:4.A	10K
R119	14:4.A	1.0K
R120	16:2.D	100K
R121	24:1.B	0
R123	16:2.D	4.7K
R124	16:2.D	4.7K
R130	16:2.C	10K
R131	18:1.D	1.0K
R132	18:2.D	47 K
R133	18:1.D	1.0K
R134	18:2.D	47 K
R135	18:5.B	0
R136	18:1.D	1.0K
R137	18:5.B	0
R138	18:2.D	47 K
R139	17:3.D	4.7
R140	18:5.D	4.7K
R141	18:2.C	47 K
R142	18:2.C	47 K
R143	18:1.C	1.0K
R144	18:1.C	1.0K
R145	18:5.C	0
R148	17:4.D	10K
R149	18:5.C	0
R150	18:5.C	0
R151	18:5.C	0
R156	17:2.B	0
R157	18:4.D	1.0K
R158	17:4.B	0
R159	18:3.D	4.7K
R160	17:2.C	0
R161	17:4.A	1.0M
R162	17:2.A	10K
R163	17:5.A	2.2K
R164	17:5.A	124.0
R165	18:3.C	0
R166	18:3.C	0
R167	19:1.C	10K
R170	19:3.C	22
R180	19:5.B	10M
R196	21:5.D	0
R197	20:4.D	10K
R198	20:4.D	3.65K
R199	20:4.D	2.49K
R200	20:3.B	10K
R201	20:3.B	10K
R202	21:2.B	49.9
R203	21:2.B	49.9
R204	21:2.B	49.9
R205	21:2.B	49.9
R206	21:2.B	49.9
R207	21:1.B	49.9
R208	21:1.B	49.9
R209	21:1.B	49.9
R210	20:4.A	124.0
R211	20:2.D	1.0K
R212	20:2.D	15K
R213	20:2.D	1.0K
R214	20:2.D	0
R215	17:2.C	0
R216	17:2.B	0
R217	17:2.B	0
R218	17:2.B	0
R219	8:1.B	10.0K
R220	8:1.B	10.0K
R221	24:2.B	10K
R222	24:2.B	100K
R223	24:2.B	1.0K
R244	22:4.C	10K
R252	23:2.B	1.0K
R256	22:5.C	10K
R257	22:5.C	10K
R258	22:5.C	10K
R273	11:4.C	10K

Format: REFDES PAGE:X.Y VALUE

R274	11:4.C	10K
R275	25:3.B	10K
R283	13:2.C	10K
R287	14:1.A	0
R288	15:2.C	1.0K
R291	20:2.C	0
R292	19:3.C	22
R297	24:2.D	124.0
R298	24:2.D	205
R299	24:2.C	470
R301	22:5.C	10K
R302	22:5.C	0
R303	24:3.D	3.09K
R304	24:3.D	1.00K
R305	24:3.C	3.32K
R306	24:3.C	1.00K
R307	24:3.B	499
R308	24:3.B	1.00K
R309	14:5.B	0
R310	14:5.B	0
R311	14:5.B	0
R312	14:5.B	0
R313	14:5.B	0
R314	14:5.B	0
R315	14:5.B	0
R316	14:5.B	0
R317	14:5.B	15K
R318	14:5.B	15K
R319	14:5.B	15K
R320	14:5.B	15K
R321	14:5.B	15K
R322	14:5.B	15K
R323	14:5.B	15K
R324	14:5.B	15K
R330	10:1.D	10K
R331	10:1.D	10K
R332	10:1.D	10K
R333	10:1.C	10K
R334	10:1.C	10K
R335	10:1.D	10K
R336	10:1.D	10K
R337	10:1.D	10K
R338	10:1.D	10K
R339	13:2.D	10K
R340	20:3.B	10K
R341	23:2.C	1.0K
R342	23:2.B	1.0K
R343	23:2.B	1.0K
R344	23:2.B	1.0K
R345	23:2.B	10K
R346	23:2.B	10K
R347	23:2.B	1.0K
R348	23:2.B	1.0K
R349	23:2.B	1.0K
R350	23:2.B	1.0K
R351	23:2.B	10K
R352	23:2.B	10K
R353	23:2.B	10K
R354	23:2.B	10K
R355	23:2.C	4.7K
R356	18:5.B	0
R358	22:1.D	0
R359	22:1.D	0
R360	22:1.D	0
R361	22:1.D	0

RN

RN1	8:3.D	22
RN2	8:2.D	22
RN3	8:3.D	22
RN4	8:2.D	22
RN5	8:3.D	22
RN6	8:2.D	22
RN7	8:3.D	22
RN8	8:2.D	22
RN9	8:3.D	22
RN10	8:3.C	22
RN11	8:3.C	22
RN12	8:2.C	22
RN13	8:3.C	22
RN14	8:2.C	22
RN15	8:3.C	22
RN16	8:2.C	22
RN17	8:3.B	22
RN18	8:2.C	22
RN20	8:3.B	22
RN22	8:2.B	22
RN23	8:3.B	22
RN24	8:2.B	22
RN25	8:3.B	22
RN26	8:3.B	22
RN27	8:3.A	22
RN28	8:3.A	22
RN85	14:2.D	22
RN86	14:2.D	22
RN87	14:2.D	22
RN92	14:2.D	22
RN96	14:2.C	22
RN100	14:2.C	22
RN103	14:2.C	22
RN104	8:2.B	22
RN105	19:2.C	22
RN106	19:2.C	22
RN107	19:2.B	22
RN108	23:2.D	10K
RN109	23:2.C	10K
RN110	23:2.C	10K
RN111	23:2.C	10K
RN112	23:2.C	10K
RN113	11:4.D	4.7K
RN114	13:2.D	10K
RN115	13:2.D	10K
RN116	14:2.C	10K
RN117	14:2.C	10K
RN118	16:2.C	4.7K
RN119	16:2.C	10K
RN120	23:3.D	10K
RN121	23:3.D	10K
RN122	23:3.C	10K
RN123	23:3.C	10K
RN124	23:3.C	10K
RN125	23:3.C	10K
RN126	23:3.B	10K
RN127	23:3.B	10K
RN128	23:3.B	10K
RN129	22:1.C	10K

SW

SW1	16:4.B	49LF002A

TP

TP1	10:5.B	T_POINT
TP2	13:4.D	T_POINT
TP3	11:3.B	T_POINT
TP4	10:5.B	T_POINT
TP6	8:4.D	T_POINT
TP7	8:4.C	T_POINT
TP8	8:5.C	T_POINT
TP9	8:5.C	T_POINT
TP10	8:5.C	T_POINT
TP11	8:5.C	T_POINT
TP12	8:4.B	T_POINT
TP13	8:4.A	T_POINT
TP14	8:5.C	T_POINT
TP15	8:5.B	T_POINT

U

U1A	8:5.D	GX3
U1B	10:5.D	GX3
U1C	9:3.D	GX3
U1D	10:5.B	GX3
U1E	12:5.D	GX3
U3	11:4.A	LM86CIM
U4A	13:5.D	CS5536
U4B	14:5.D	CS5536
U4C	15:4.C	CS5536
U5	16:4.D	32
U6	17:3.C	CODEC/TOUCH
U7	19:4.C	MK1491-09F
U9	20:3.D	AT93C46A
U10	20:4.C	RTL8110SB
U15	22:4.D	W83626F
U22	11:3.C	SN74LVC244
U25	24:2.D	LM1117MPX-A‡
U26	24:5.D	LM3475
U27	24:5.C	LM3475
U28	24:5.B	LM3475
U29	22:2.D	XC2C32A-6QF‡
U30	22:1.B	LP3984IMF-1‡
U31	13:2.C	SN74CBTLV1G‡

Y

Y1	13:1.C	32.768KHz
Y2	14:1.B	48.0000MHZ
Y3	17:4.B	24.576MHz
Y4	19:5.B	14.31818MHz